Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

DAC1653D/DAC1658D

Dual 16-bit DAC: 10 Gbps JESD204B interface: x2, x4 and x8 interpolating

Datasheet
Revision 2.41

1. General description

DAC1653D and DAC1658D are high-speed, high-performance 16-bit dual channel Digital-to-Analog Converters (DACs). The devices provide sample rates up to 2 Gsps with selectable ×2, ×4 and ×8 interpolation filters optimized for multi-carrier and broadband wireless transmitters.

When both devices are referred to in this data sheet, the following convention will be used: DAC165xD.

The DAC165xD integrates a JEDEC JESD204B compatible high-speed serial input data interface running up to 10 Gbps allowing dual channel input sampling at up to 1 Gsps over four differential lanes. It offers numerous advantages over traditional parallel digital interfaces:

- Easier Printed-Circuit Board (PCB) layout
- Lower radiated noise
- Lower pin count
- Self-synchronous link
- Skew compensation
- Deterministic latency
- Multiple Device Synchronization (MDS); JESD204B subclass 1 compatible
- Harmonic clocking support
- Assured FPGA interoperability

There are two versions of the DAC165xD:

- Low common-mode output voltage (part identification DAC1653D)
- High common-mode output voltage (part identification DAC1658D)

An optional on-chip digital modulator converts the complex I/Q pattern from baseband to IF. The mixer frequency is set by writing to the Serial Peripheral Interface (SPI) control registers associated with the on-chip 40-bit Numerically Controlled Oscillator (NCO). This accurately places the IF carrier in the frequency domain. The 13-bit phase adjustment feature, the 12-bit digital gain and the 16-bit digital offset enable full control of the analog output signals.

The DAC165xD is fully compatible with device subclass 1 of the JEDEC JESD204B standard, guaranteeing deterministic and repeatable interface latency using the differential SYSREF signal. The device also supports harmonic clocking to reduce system-level clock synthesis and distribution challenges.

Multiple Device Synchronization (MDS) enables multiple DAC channels to be sample synchronous and phase coherent to within one DAC clock period. MDS is ideal for LTE and LTE-A MIMO transceiver applications.

The DAC165xD includes a ×2, ×4 or ×8 divider to achieve the best possible noise performance at the analog outputs, allowing harmonic clocking through the system. The internal regulator adjusts the full-scale output current between 10 mA and 30 mA.

The device is available in a VFQFP-N 56 package (8 mm × 8 mm).

2. Features and benefits

- Dual channel 16-bit resolution
- 2.0 GSps maximum output update rate
- JEDEC JESD204B device subclass I compatible: SYSREF based deterministic and repeatable interface latency
- Multiple device synchronization enables multiple DAC channels to be sample synchronous and phase coherent to within one DAC clock period
- 1, 2 or 4 configurable JESD204B serial input lanes running up to 10 Gbps with embedded termination and programmable equalization gain (CTLE)
- 1 Gsps maximum baseband input data rate
- SPI interface (3-wire or 4-wire mode) for control setting and status monitoring
- Differential scalable output current from 10 mA to 30 mA
- Embedded NCO with 40-bit programmable frequency and 16-bit phase adjustment
- Embedded complex (IQ) digital modulator
- 1.2 V and 3.3 V power supplies (for DAC1653D series, the 3.3V supply voltage can be lowered to 2.7V for lower power consumption)
- Flexible SPI power supply (1.8 V or 1.2 V) ensuring compatibility with on-board SPI bus
- Flexible differential SYNC signals power supply (1.8 V or 1.2 V) ensuring compatibility with on-board devices
- Embedded Temperature Sensor
- Configurable IOs pins for monitoring, interrupt
- XBERT features (PRBS31, 23, 15, 7, JTSPAT, STLTP)
- $SFDR_{RBW}$ = 88 dBc typical (f_s = 1.50 Gsps; interpolation ×2; bandwidth = 250 MHz; f_{out} = 150 MHz)
- NSD = −167 dBc/Hz typical (f_o = 70 MHz)
- IMD3 = 85 dBc typical (f_s = 1.50 Gsps; interpolation ×2; f_{o1} = 152 MHz; f_{o2} = 155.1 MHz)
- Four carriers ACLR = 76 dB typical (f_s = 1.50 Gsps; f_{NCO} = 350 MHz)
- RF enable/disable pin and RF automatic mute
- Clock divider by 2, 4, 6 and 8 available at the input of the clock path
- Group delay compensation
- Analog offset control (10-bit auxiliary DACs)
- Power-down mode controls
- On-chip 0.7 V reference
- Industrial temperature range −40 °C to +85 °C
- Low (DAC1653D) or high (DAC1658D) common-mode output voltage
- VFQFP-N 56 package (8 mm × 8 mm)
- Embedded Power On Reset
- Lane swapping and polarity swapping
- Signal Power Detector, IQ-Range detector, Level detectors with Auto-Mute feature

3. Applications

- Wireless infrastructure radio base station transceivers, including: LTE-A, LTE, MC-GSM, W-CDMA, TD-SCDMA
- LMDS/MMDS, point-to-point microwave backhaul
- Direct Digital Synthesis (DDS) instruments
- High-definition video broadcast production equipment
- Automated Test Equipment (ATE)

4. ORDERING INFORMATION

Table 1. Ordering information

Type number	Package			
	Name	Description	Shipping Packaging	Version
DAC1653D2G0NLGA8	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tape & Reel	PSC-4110
DAC1653D1G5NLGA8	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tape & Reel	PSC-4110
DAC1653D1G0NLGA8	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tape & Reel	PSC-4110
DAC1658D2G0NLGA8	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tape & Reel	PSC-4110
DAC1658D1G5NLGA8	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tape & Reel	PSC-4110
DAC1658D1G0NLGA8	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tape & Reel	PSC-4110
DAC1653D2G0NLGA	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tray	PSC-4110
DAC1653D1G5NLGA	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tray	PSC-4110
DAC1653D1G0NLGA	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tray	PSC-4110
DAC1658D2G0NLGA	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tray	PSC-4110
DAC1658D1G5NLGA	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tray	PSC-4110
DAC1658D1G0NLGA	VFQFP-N 56	VFQFP-N 8.0 × 8.0 × 0.85 mm; no lead	Tray	PSC-4110

5. BLOCK DIAGRAM

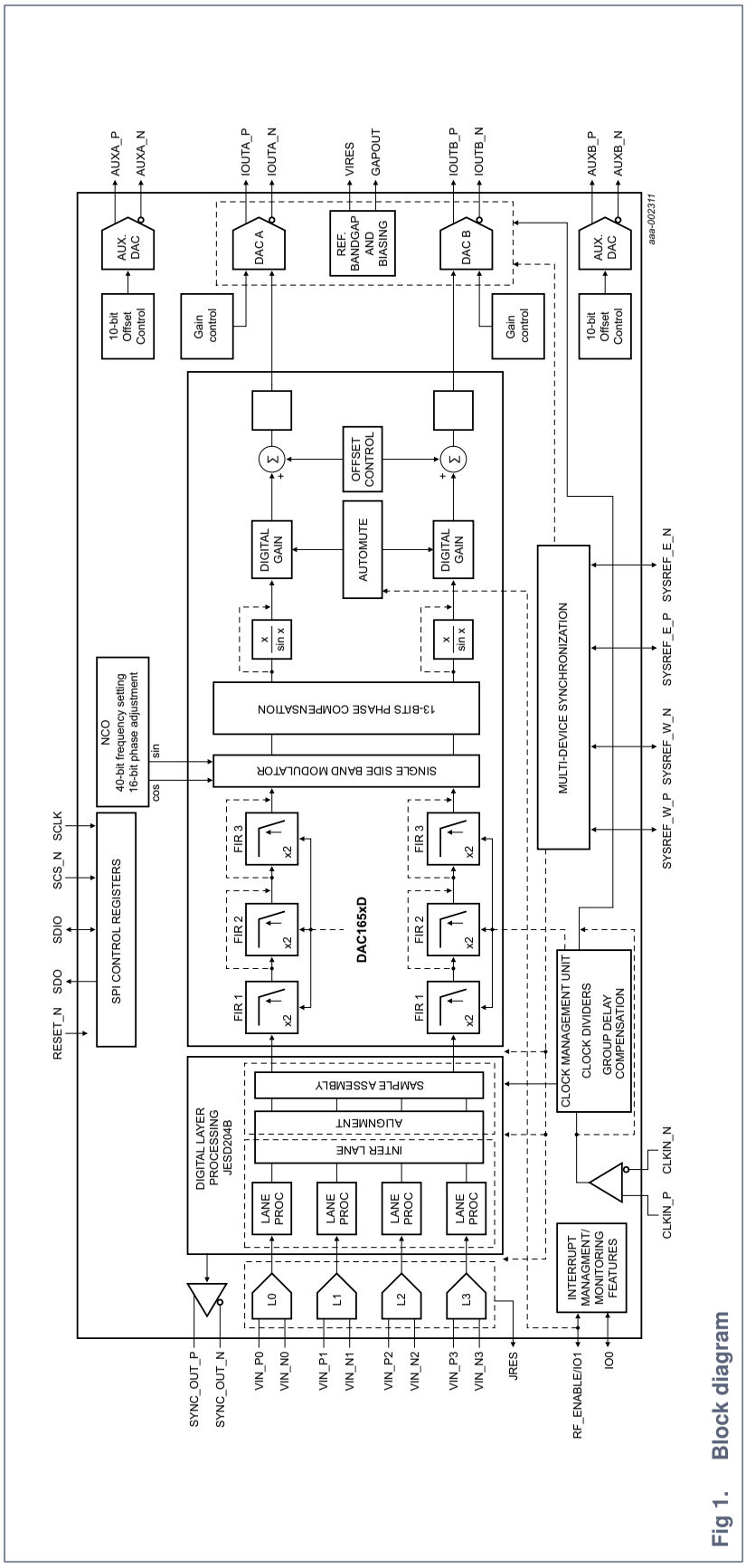

Fig 1. Block diagram

6. PINNING INFORMATION

6.1 Pinning

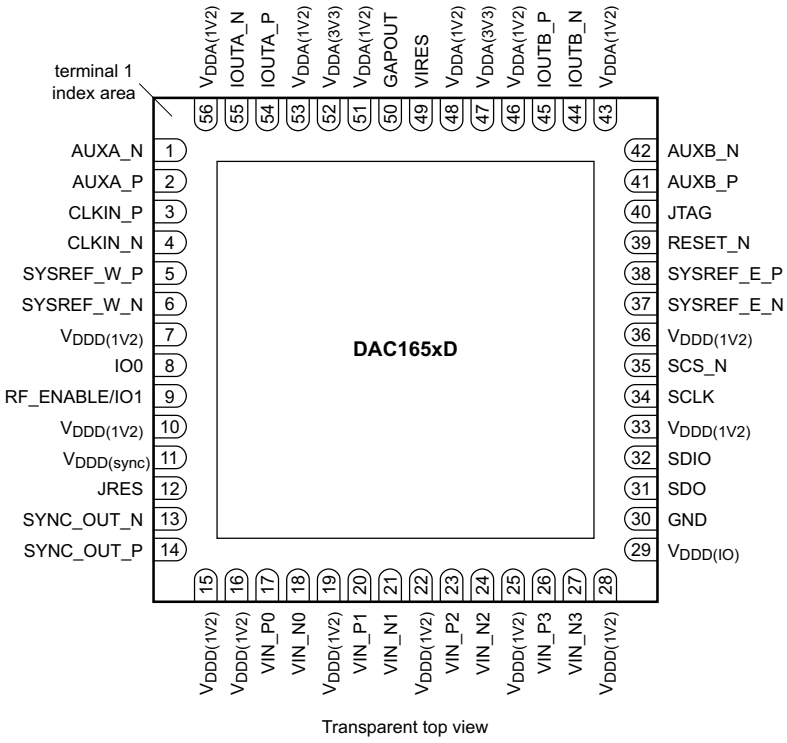

Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
AUXA_N	1	O	complementary auxiliary DAC A output current
AUXA_P	2	O	auxiliary DAC A output current
CLKIN_P	3	I	DAC clock positive input
CLKIN_N	4	I	DAC clock negative input
SYSREF_W_P	5	I/O	multiple device synchronization positive signal, west side (if not used, keep it floating)
SYSREF_W_N	6	I/O	multiple device synchronization negative signal, west side (if not used, keep it floating)
$V_{DDD(1V2)}$	7	P	1.2 V digital power supply
IO0	8	I/O	IO port bit 0
RF_ENABLE/IO1	9	I/O	IO port bit 1 or RF enable pin (see Section automute)
$V_{DDD(1V2)}$	10	P	1.2 V digital power supply
$V_{DDD(sync)}$	11	P	flexible power supply for SYNC differential signals (1.2 V to 1.8 V; see Section 11.2.1.1)
JRES	12	I/O	calibration resistor (6.98 kΩ 1%) for serial lanes termination
SYNC_OUT_N	13	O	synchronization request to transmitter, complementary output

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
SYNC_OUT_P	14	O	synchronization request to transmitter
$V_{DDD(1V2)}$	15	P	1.2 V digital power supply for JESD204B interface
$V_{DDD(1V2)}$	16	P	1.2 V digital power supply for JESD204B Lane 0
VIN_P0	17	I[2]	serial interface lane 0 positive input (AC coupling recommended)
VIN_N0	18	I[2]	serial interface lane 0 negative input (AC coupling recommended)
$V_{DDD(1V2)}$	19	P	1.2 V digital power supply for JESD204B Lane 0 and Lane 1
VIN_P1	20	I[2]	lane 1 serial interface positive input (AC coupling recommended)
VIN_N1	21	I[2]	serial interface lane 1 negative input (AC coupling recommended)
$V_{DDD(1V2)}$	22	P	1.2 V digital power supply for JESD204B Lane 1 and Lane 2
VIN_P2	23	I[2]	serial interface lane 2 positive input (AC coupling recommended)
VIN_N2	24	I[2]	serial interface lane 2 negative input (AC coupling recommended)
$V_{DDD(1V2)}$	25	P	1.2 V digital power supply for JESD204B Lane 2 and Lane 3
VIN_P3	26	I[2]	serial interface lane 3 positive input (AC coupling recommended)
VIN_N3	27	I[2]	serial interface lane 3 negative input (AC coupling recommended)
$V_{DDD(1V2)}$	28	P	1.2 V digital power supply for JESD204B Lane 3
$V_{DDD(IO)}$	29	P	flexible power supply for SPI IOs and IO0/IO1 signals (1.2 V to 1.8 V; see Section 11.2.1)
GND	30	G	connect to ground
SDO	31	O	SPI data output
SDIO	32	I/O	SPI data input/output
$V_{DDD(1V2)}$	33	P	1.2 V digital power supply
SCLK	34	I	SPI clock
SCS_N	35	I	SPI chip select (active LOW)
$V_{DDD(1V2)}$	36	P	1.2 V digital power supply
SYSREF_E_N	37	I/O	multiple device synchronization negative signal, east side (if unused, leave it floating)
SYSREF_E_P	38	I/O	multiple device synchronization positive signal, east side (if unused, leave it floating)
RESET_N	39	I	general reset (active LOW)
JTAG	40	G	JTAG connection (connect to ground)
AUXB_P	41	O	auxiliary DAC B output current
AUXB_N	42	O	complementary auxiliary DAC B output current
$V_{DDA(1V2)}$	43	P	1.2 V analog power supply
IOUTB_N	44	O	complementary DAC B output current
IOUTB_P	45	O	DAC B output current
$V_{DDA(1V2)}$	46	P	1.2 V analog power supply
$V_{DDA(3V3)}$	47	P	DAC1658D: 3.3 V analog power supply
			DAC1653D: 2.5 V to 3.3 V analog power supply
$V_{DDA(1V2)}$	48	P	1.2 V analog power supply
VIRES	49	I/O	DAC biasing resistor (562 Ω 1%)
GAPOUT	50	I/O	band gap input/output voltage
$V_{DDA(1V2)}$	51	P	1.2 V analog power supply
$V_{DDA(3V3)}$	52	P	DAC1658D: 3.3 V analog power supply
			DAC1653D: 2.5 V to 3.3 V analog power supply

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
$V_{DDA(1V2)}$	53	P	1.2 V analog power supply
IOUTA_P	54	O	DAC A output current
IOUTA_N	55	O	complementary DAC A output current
$V_{DDA(1V2)}$	56	P	1.2 V analog power supply

[1] P: power supply; G: ground; I: input; O: output.

[2] JESD204B input lanes can be swapped between P and N using dedicated registers. The order of lanes can be updated logically (see Section 11.8.5.3).

7. LIMITING VALUES

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDA(3V3)}$	analog supply voltage		–0.5	+4.6	V
$V_{DDD(1V2)}$	digital supply voltage		–0.5	+1.5	V
$V_{DDA(1V2)}$	analog supply voltage		–0.5	+1.5	V
V_I	input voltage	pins VIN_Px; VIN_Nx, VIRES, GAPOUT; referenced to 1V2	–0.5	+1.5	V
	input voltage for clocks and SYSREF pins	pins CLK_P,CLK_N, SYSREF_W_P; SYSREF_W_N, SYSREF_E_P;SYSREF_E_N;	–0.5	1.95	V
V_O	output voltage	pins IOUTA_P; IOUTA_N; IOUTB_P; IOUTB_N; AUXA_P; AUXA_N; AUXB_P and AUXB_N; referenced to GND	–0.5	+4.6	V
$V_{DDD(IO)}$	I/O digital supply voltage	pins SDO; SDIO; SCLK; SCS_N; RESET_N; JTAG; IO0; RF_ENABLE/IO1	–0.5	2.1	V
$V_{DDD(sync)}$	digital supply voltage for differential output buffers	pins SYNC_OUT_P; SYNC_OUT_N,	–0.5	2.1	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		–40	+125	°C

8. THERMAL CHARACTERISTICS

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
JEDEC 4L board					
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	23.6	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	13.7	K/W
$R_{th(j-b)}$	thermal resistance from junction to bottom case		[1]	0.9	K/W
JEDEC compliance board with additional layers count					
$R_{th(j-a)}$	thermal resistance from junction to ambient	6 layers	[2]	17.5	K/W
		8 layers	[2]	17.4	K/W
		12 layers	[2]	15.5	K/W

[1] In compliance with JEDEC test board; in free air with 64 thermal vias, class 5

[2] In free air with 64 thermal vias, class 5

9. STATIC CHARACTERISTICS

9.1 Common characteristics

The DAC165xD requires supplies of both 3.3 V and 1.2 V or 1.3 V for DAC sample rate above 1.8 Gsps. The 1.2 V supply has separate digital and analog power supply pins. The SPI power supply is flexible. It can be set from1.2 V to1.8 V (see Section 11.2.1.1).

Table 5. Common characteristics

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 $V_{pp,diff}$; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Voltages							
$V_{DDA(3V3)}$	analog supply voltage	DAC1658D: high common mode output	C	3.15	3.3	3.45	V
		DAC1653D: low common mode output	C	2.7[2]	3.3	3.45	V
$V_{DDD(1V2)}$	digital supply voltage		C	1.14[3]	1.2	1.26	V
$V_{DDA(1V2)}$	analog supply voltage		C	1.14	1.2	1.26	V
$V_{DDD(IO)}$	I/O digital supply voltage		C	1.14	1.2	1.9	V
$V_{DDD(sync)}$	digital supply voltage for differential SYNC output buffers		C	1.14	1.2	1.9	V
Clock inputs (pins CLKIN_P, CLKIN_N)							
$V_{i(cm)}$	common-mode input voltage. Internal self-biased. AC-coupling recommended		D	-	800	-	mV
$V_{i(diff)}$	differential Peak-to-Peak voltage		D	400	1000	2000	mV
f_{in}	Input frequency compliance range	direct clocking	D			2000	MHz
		harmonic clocking (using clock divider)	D			3000	MHz
$R_{i(diff)}$	differential input resistor		D	-	100	-	Ω
C_i	input capacitance		D	-	2	-	pF
Digital inputs/outputs (SYSREF_W_P/SYSREF_W_N, SYSREF_E_P/SYSREF_E_N)							
$V_{i(cm)}$	common-mode input voltage	$V_{DDD(IO)}$=1.8V	D	800	1200	1400	mV
		$V_{DDD(IO)}$=1.2V	D	800	950	1100	mV
$V_{i(diff)}$	differential Peak-to-Peak voltage		D	400	800	1000	mV
$R_{i(diff)}$	differential input resistor (could be disconnected see Table 102)		D	-	100	-	Ω
C_i	input capacitance		D	-	0.7	-	pF
Digital inputs (pins SDO, SDIO, SCLK, SCS_N, RESET_N)							
V_{IL}	LOW-level input voltage		C	GND	-	$0.3V_{DDD(IO)}$	V
V_{IH}	HIGH-level input voltage		C	$0.7V_{DDD(IO)}$	-	$V_{DDD(IO)}$	V

Table 5. Common characteristics *…continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 $V_{pp,diff}$; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Digital inputs (VIN_Px/VIN_Nx) compliant with the LV-OIF-11G-SR; CML format							
V_{cm}	common-mode voltage	AC coupling is mandatory	D	0.580	-	1.126	V
$V_{pp-diff}$	differential peak-to-peak voltage	below 8 Gbps	D	80	-	-	mV
		above 8 Gbps	D	110	-	-	mV
Z_{diff}	differential impedance	controlled by SPI register	D	71	100	190	Ω
Hi-Z_{diff}	tri-state observed impendance		D	-	64	-	kΩ
DR	data rate		D	2	-	10	Gbps
Digital outputs (pins SYNC_OUT_P and SYNC_OUT_N)							
V_{cm}	common-mode voltage	controlled by SPI register			-		
		$V_{DDD(sync)}$ = 1.8 V	D	1.0	-	1.7	V
		$V_{DDD(sync)}$ = 1.2 V	I	0.4	-	1.1	V
$V_{O(diff)(swing)}$	swing differential output voltage		I	100	-	1200	mV
Digital outputs (pins SDO, SDIO)							
V_{OL}	LOW-level output voltage		I	-	-	$0.3V_{DDD(IO)}$	V
V_{OH}	HIGH-level output voltage		I	$0.7V_{DDD(IO)}$	-	-	V
Reference voltage output (pin GAPOUT)							
$V_{O(ref)}$	reference output voltage	T_{amb} = 25 °C	I	-	0.70	-	V
Analog auxiliary outputs (pins AUXA_P, AUXA_N, AUXB_P and AUXB_N)							
$I_{O(fs)}$	full-scale output current	normal resolution	I	-	2.3	-	mA
		high resolution	D	-	40	-	µA
$N_{DAC(aux)mono}$	auxiliary DAC monotonicity	guaranteed	D	-	10	-	bits
DAC output timing							
f_s	sampling rate	DAC165xD2G0	C	-[4]	-	2000	Msps
		DAC165xD1G5	C	-[4]	-	1500	Msps
		DAC165xD1G0	C	-[4]	-	1000	Msps
t_s	settling time	t_o = ±0.5LSB	D	-	20	-	ns

[1] D = guaranteed by design; C = guaranteed by characterization; I = industrially tested.

[2] Lower power supply value could be used but the overall DAC performances will be degraded.

[3] For frequencies higher than 1.7Gsps and when using all digital features (NCO, inv sin(x)/x, phase correction, ..) the minimum value is 1.165V

[4] Minimum value is linked to the JESD204B link configuration and lane rate

9.2 Specific characteristics

Table 6. Currents characteristics

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	DAC165xD			Unit
				Min	Typ	Max	
Currents							
$I_{DDA(3V3)}$ [2]	analog supply current	DAC1658D High Common Mode: all use cases	I	-	64	68	mA
		DAC1653D Low Common Mode: all use cases	I	-	114	122	mA
$I_{DDD(IO)}$ [2]	digital supply current for IO pins	depends on SPI IO0/IO1 activity	I	-	0.5	1	mA
$I_{DDD(sync)}$ [2]	digital supply current for SYNC pins	all use cases	I	-	5	7	mA
$I_{DDD(1V2)}$	digital supply current	NCO off;×2 interpolation; MDS off; invsinc off, phase correction off					
		f_s = 983.04 Msps	C	-	250	285	mA
		f_s = 1474.56 Msps	C	-	330	365	mA
		f_s = 1966.80 Msps	C	-	400	445	mA
$I_{DDA(1V2)}$ [2]	analog supply current	$V_{DDA(1V2)}$ = 1.2 V	I	-	203	220	mA

[1] D = guaranteed by design; C = guaranteed by characterization; I = industrially tested.

[2] Power supply independent of the DAC sampling frequency.

Table 7. Specific characteristics

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff; unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658D: High common-mode			DAC1653D: Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
Power										
P_{tot}	total power dissipation	NCO off;×2 interpolation; MDS off; invsinc off, phase correction off								
		V_{DDA} = 3.3 V; all V_{DDD} = 1.2 V								
		f_s = 983.04 Msps; four JESD204B lanes at 4.9152 Gbps	C	-	761	873	-	932	1059	mW
		f_s = 1474.56 Msps; four JESD204B lanes at 7.3728 Gbps	C	-	857	974	-	1028	1160	mW
		f_s = 1966.80 Msps; four JESD204B lanes at 9.8304 Gbps	C	-	941	1075	-	1112	1261	mW
		NCO on;×2 interpolation; MDS off; invsinc off, phase correction off								
		f_s = 983.04 Msps; four JESD204B lanes at 4.9152 Gbps	C		833	955	-	1004	1141	mW
		f_s = 1474.56 Msps; four JESD204B lanes at 7.3728 Gbps	C		953	1088	-	1124	1273	mW
		f_s = 1966.80 Msps; four JESD204B lanes at 9.8304 Gbps	C		1085	1233	-	1256	1418	mW
		full power-down[2]	C	-	-	5	-	-	5	mW
Analog outputs (pins IOUTA_P, IOUTA_N, IOUTB_P, IOUTB_N)										
$I_{O(fs)}$	full-scale output current		D	10	20	30	10	20	30	mA
$I_{O(cm\_offset)}$	additional common current	this additional common current is to be taken into account into filter design and component connection	D	-	1.6	-	-	1.6	-	mA
V_{O_comp}	output voltage compliance range	$V_{DDA(3V3)}$ =3.3 V	D	$V_{DDA(3V3)}$ -1.0	-	$V_{DDA(3V3)}$	0	-	1.0	V
		$V_{DDA(3V3)}$ =2.5 V	D	n.a.	n.a.	n.a.	0	-	0.6	V
R_o	internal output resistance		D	-	250	-	-	250	-	kΩ

Table 7. Specific characteristics …continued

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff; unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658D: High common-mode			DAC1653D: Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
C_{PN}	differential output capacitance		D	-	0.5	-	-	0.5	-	pF
C_P	positive output capacitance		D	-	5.5	-	-	5.5	-	pF
C_N	negative output capacitance		D	-	5.5	-	-	5.5	-	pF

[1] D = guaranteed by design; C = guaranteed by characterization; I = industrially tested.

[2] Full power-down mode is done by setting the following registers: x0043=x01; x0040=xF3 and x0020=x00.

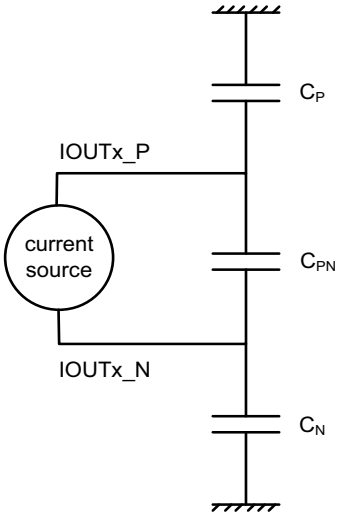

Fig 3. DAC output simplified model

10. Dynamic characteristics

Table 8. Dynamic characteristics DAC165xD

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	DAC1658D High common-mode			DAC1653D Low common-mode			Unit
			f_s	1 Gsps	1.5 Gsps	2 Gsps	1 Gsps	1.5 Gsps	2 Gsps	
SFDR	spurious-free dynamic range	interpolation x2 BW = f_s / 2 V_{DDA} = 3.3 V; f_o = 20 MHz								
		at −1 dBFS	C	92	91	90	92	91	90	dBc
		at −7 dBFS	C	86	86	87	86	85	85	dBc
		at −14 dBFS	C	80	80	79	80	80	79	dBc
		V_{DDA} = 3.3 V; f_o = 150 MHz								
		at −1 dBFS	I	85	84	83	82	83	81	dBc
		at −7 dBFS	C	83	81	79	80	79	77	dBc
		at −14 dBFS	C	77	76	72	77	75	73	dBc
		V_{DDA} = 3.3 V; f_o = 350 MHz								
		at −1 dBFS	C	67	76	75	66	76	73	dBc
		at −7 dBFS	C	70	76	75	68	75	73	dBc
		at −14 dBFS	C	70	72	70	70	72	70	dBc
IMD3	third-order intermodulation distortion	V_{DDA} = 3.3 V; f_{o1} = 20 MHz; f_{o2} = 21 MHz; −7 dBFS per tone	C	92	92	95	92	92	95	dBc
		V_{DDA} = 3.3 V; f_{o1} = 230 MHz; f_{o2} = 231 MHz; −7 dBFS per tone	C	80	83	87	80	83	87	dBc
ACPR	adjacent channel power ratio	f_o = 40 MHz								
		1 WCDMA carrier; BW = 5 MHz	C	80	80	80	80	80	80	dBc
		4 WCDMA carriers; BW = 20 MHz	C	77	78	77	77	78	77	dBc
		f_o = 350 MHz								
		1 WCDMA carrier; BW = 5 MHz	C	80	80	80	78	79	79	dBc
		4 WCDMA carriers; BW = 20 MHz	C	75	76	75.5	75	76	75	dBc
NSD	noise spectral density	f_o = 70 MHz at −1 dBFS	C		-167			−165		dBc/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = industrially tested.

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; input level = -1/-7/-14 dBFS; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

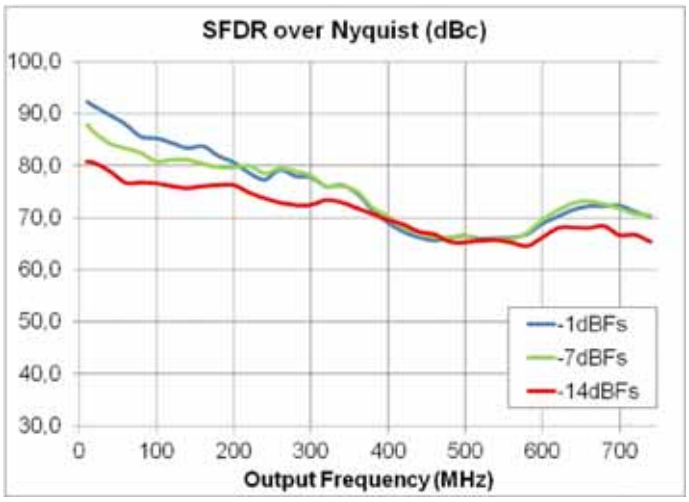

Fig 4. SFDR(dBc) over Nyquist depending of fout (MHz) and input level (dBFS)

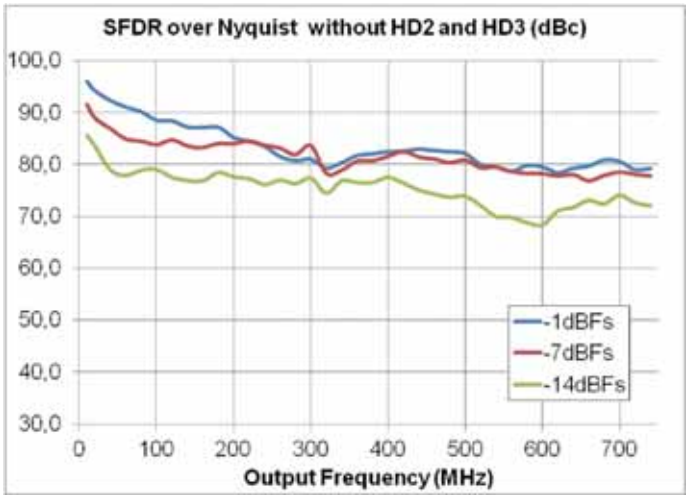

Fig 5. SFDR without HD2 and HD3 (dBc) over Nyquist depending of fout (MHz) and input level (dBFS)

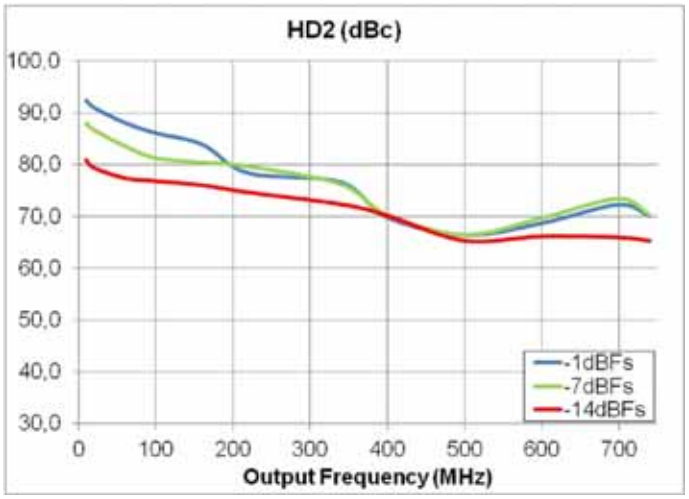

Fig 6. HD2(dBm) over Nyquist depending of fout (MHz) and input level (dBFS)

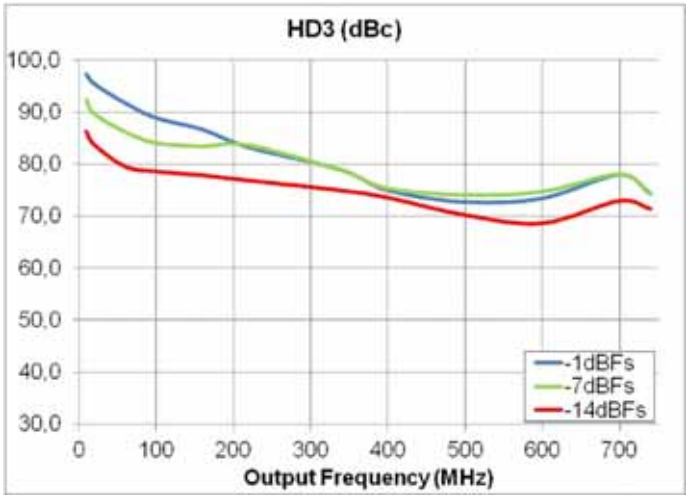

Fig 7. HD3 (dBm) over Nyquist depending of fout (MHz) and input level (dBFS)

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; input level = -7/ -14 / -19 dBFS per tone, 1 MHz spacing; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

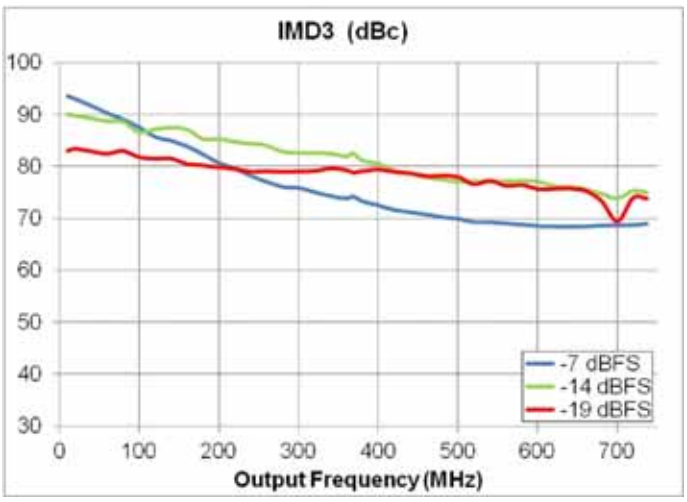

Fig 8. IMD3 (dBc) depending of fout (MHz) and input level per tone (dBFS)

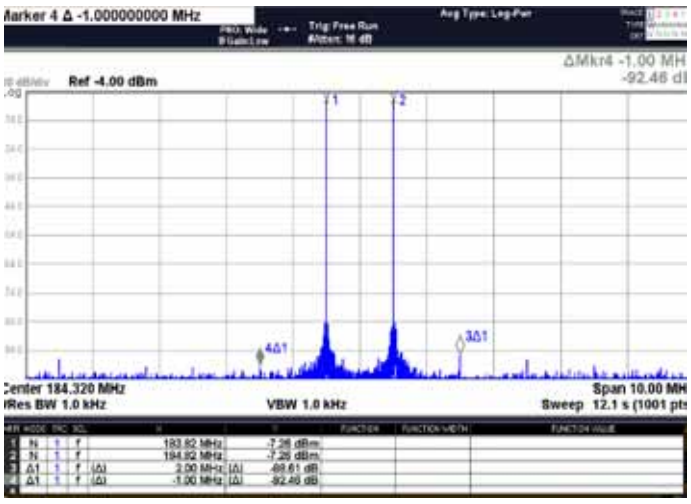

Fig 9. IMD3 (dBc) for two tones (spacing 1 MHz) centered at 184.32 MHz

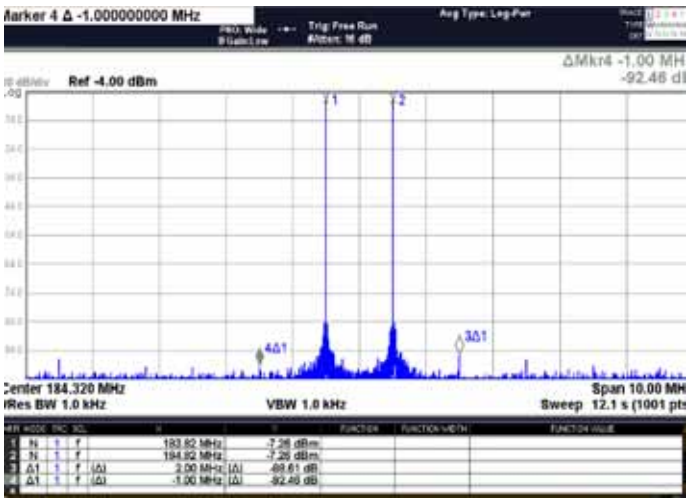

Fig 10. IMD3 (dBc) for two tones (spacing 10 MHz) centered at 184.32 MHz

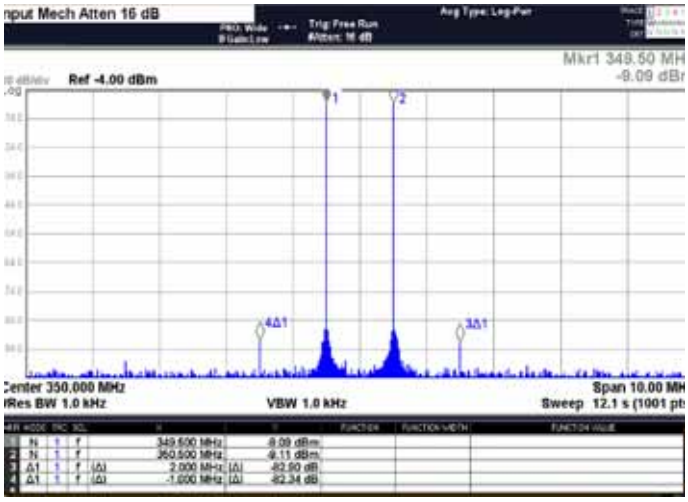

Fig 11. IMD3 (dBc) for two tones (spacing 1 MHz) centered at 350 MHz

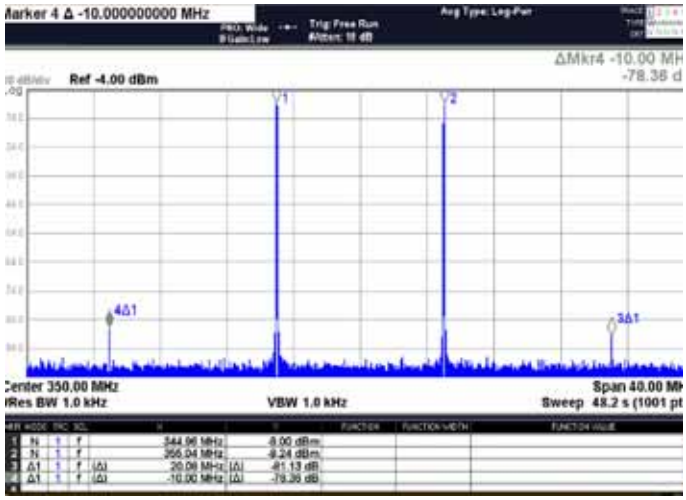

Fig 12. IMD3 (dBc) for two tones (spacing 10 MHz) centered at 350 MHz

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1 Gsps, 1.5 Gsps and 2 Gsps sample rates used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; input level = -1 dBFS; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

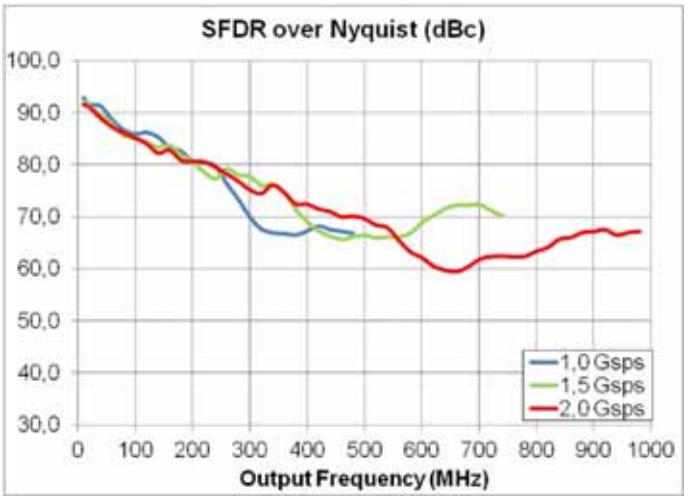

Fig 13. SFDR (dBc) over Nyquist depending of fout (MHz) and sampling frequency (Gsps)

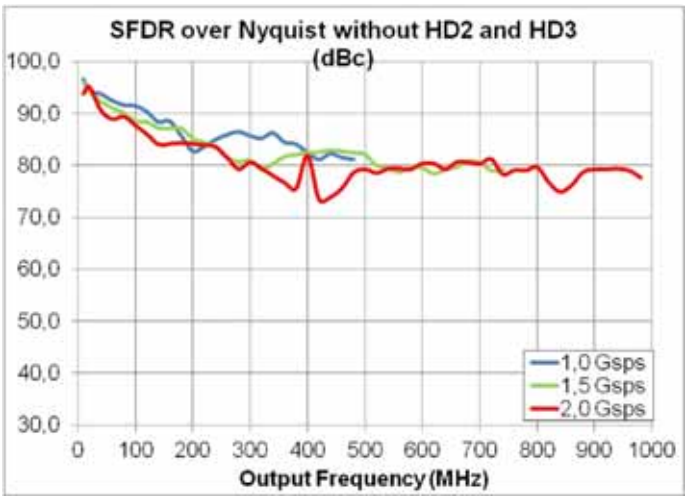

Fig 14. SFDR without HD2 and HD3 (dBc) over Nyquist depending of fout (MHz) and sampling frequency (Gsps)

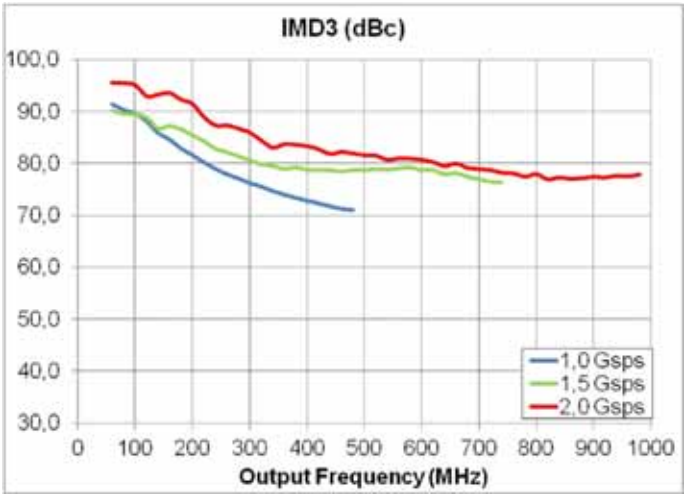

Fig 15. IMD3 (dBc) depending of fout (MHz) and sampling frequency (Gsps)

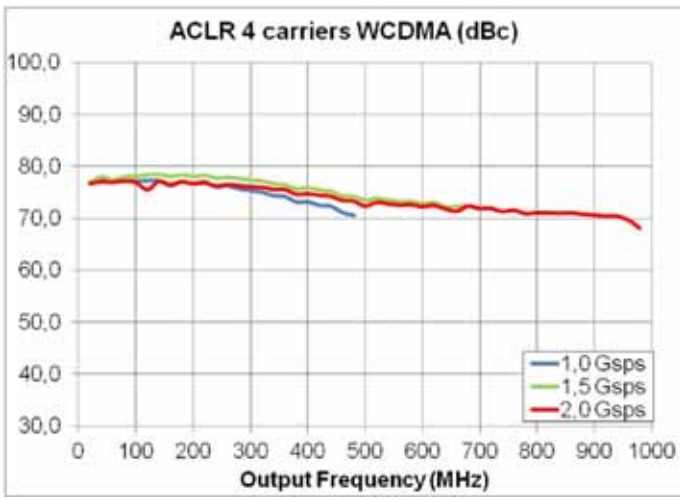

Fig 16. ACLR WCDMA 4 carriers depending of fout (MHz) and sampling frequency (Gsps)

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1 Gsps, 1.5 Gsps and 2 Gsps sample rates used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; input level = -1 dBFS; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

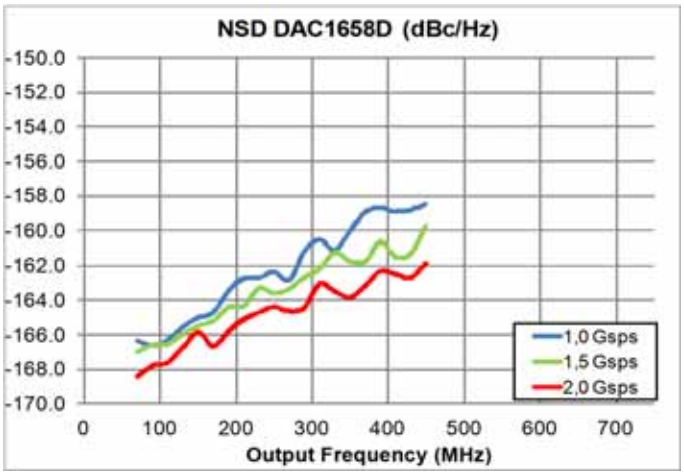

Fig 17. DAC1658D NSD (dBc/Hz) depending of output frequency (MHz)

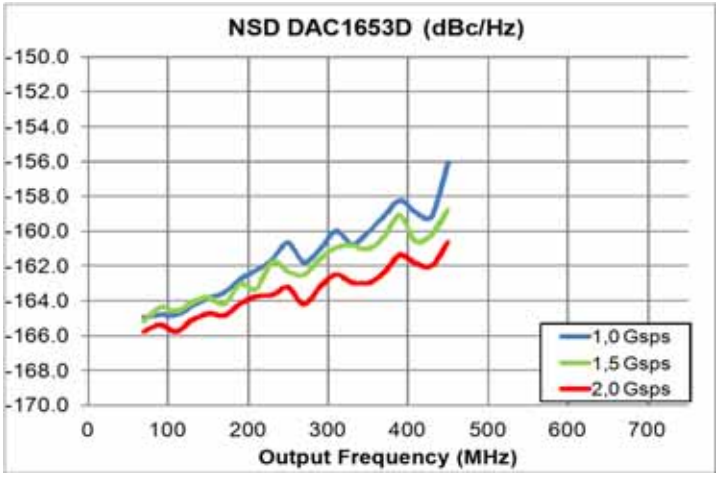

Fig 18. DAC1653D NSD (dBc/Hz) depending of output frequency (MHz)

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

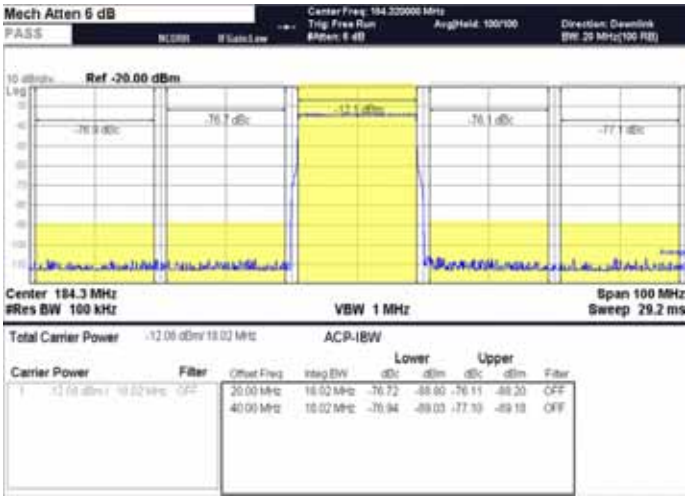

Fig 19. ACLR of 1 carrier LTE (BW=20 MHz) centered at 184.32 MHz

Fig 20. ACLR of 2 carriers LTE (BW=2 x 20 MHz) centered at 184.32 MHz

Fig 21. ACLR of 1 carrier LTE (BW=20 MHz) centered at 350 MHz

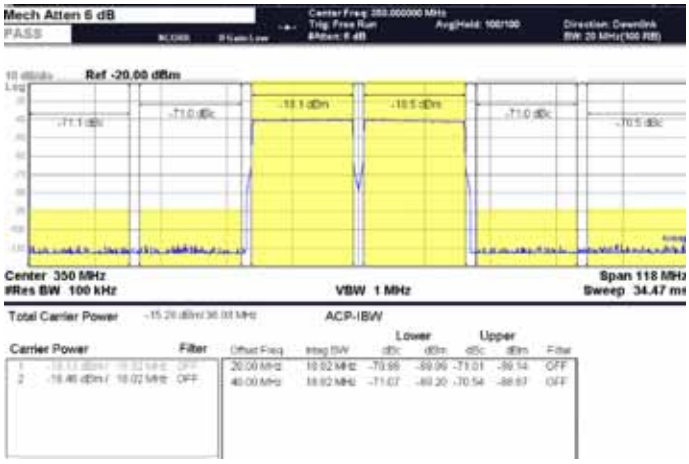

Fig 22. ACLR of 2 carriers LTE (BW=2 x 20 MHz) centered at 350 MHz

Other parameters are specified as follow: $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff, output signal frequency = 100 MHz; unless otherwise specified.

Reducing the $V_{DDA(3V3)}$ power supply allows to decrease the total power consumption for the DAC1653D. However, specific correctives factors needs to be apply to the dynamic performances for DAC1653D. These correctives factors depend of the value of analog power supply $V_{DDA(3V3)}$ and the value of the output common mode voltage V_{cm}.

Second harmonic distortion HD2 is only dependent of the $V_{DDA(3V3)}$ power supply value.

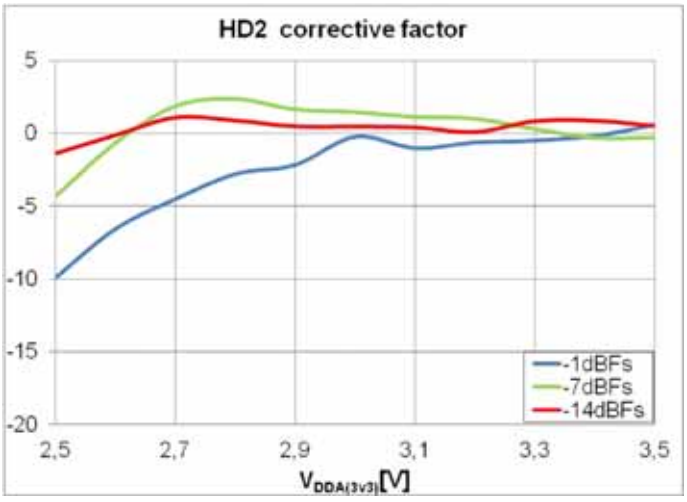

Fig 23. HD2 corrective factor (dB) depending of $V_{DDA(3V3)}$ (V) and input level per tone (dBFS)

Third harmonic distortion HD3 and Intermodulation product IMD3 are dependents of the difference voltage between $V_{DDA(3V3)}$ power supply and V_{cm} common mode output voltage.

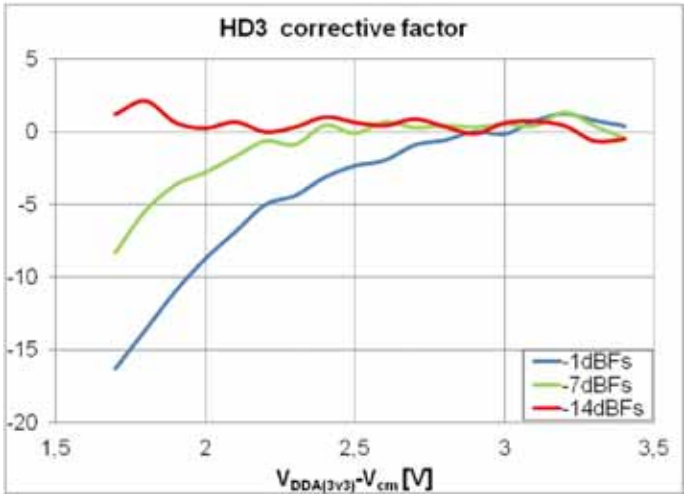

Fig 24. HD3 corrective factor (dB) depending of ($V_{DDA(3V3)}$- V_{cm}) (V) and input level per tone (dBFS)

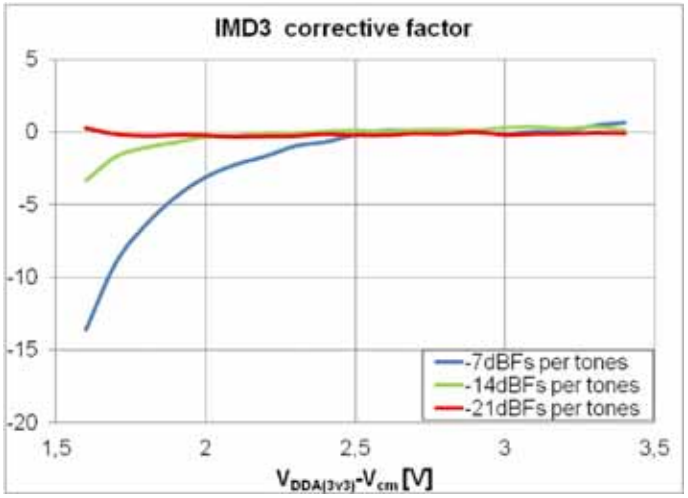

Fig 25. IMD3 corrective factor (dB) depending of ($V_{DDA(3V3)}$- V_{cm}) (V) and input level per tone (dBFS)

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; no inverse sin(x)/x; no output correction; input level = -1 dBFS; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

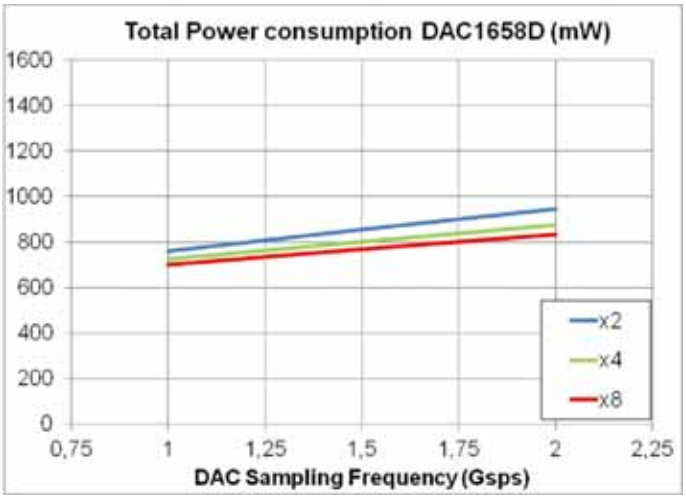

Fig 26. Total Power consumption DAC1658D (mW) depending of the DAC sampling frequency and the interpolation factor (all digital features off)

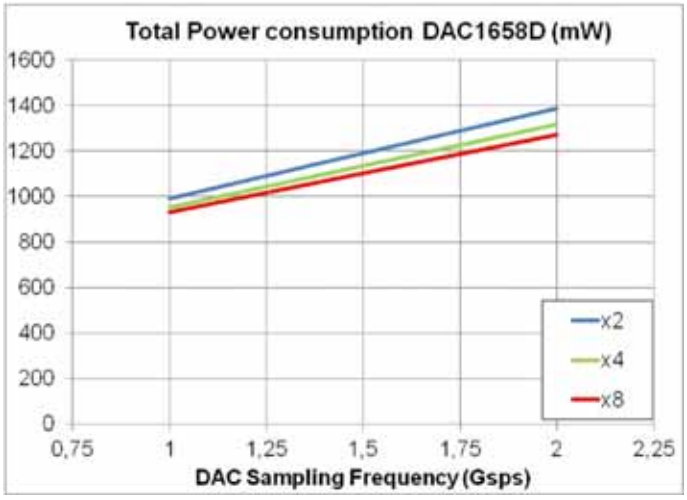

Fig 27. Total Power consumption DAC1658D (mW) depending of the DAC sampling frequency and the interpolation factor (all digital features on)

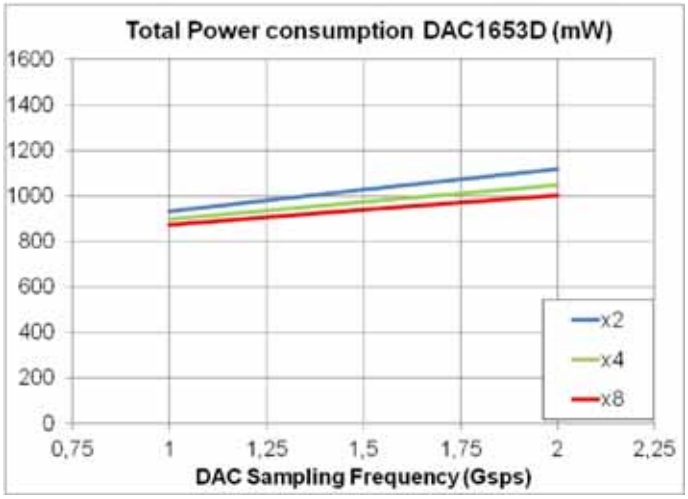

Fig 28. Total Power consumption DAC1653D (mW) depending of the DAC sampling frequency and the interpolation factor (all digital features off)

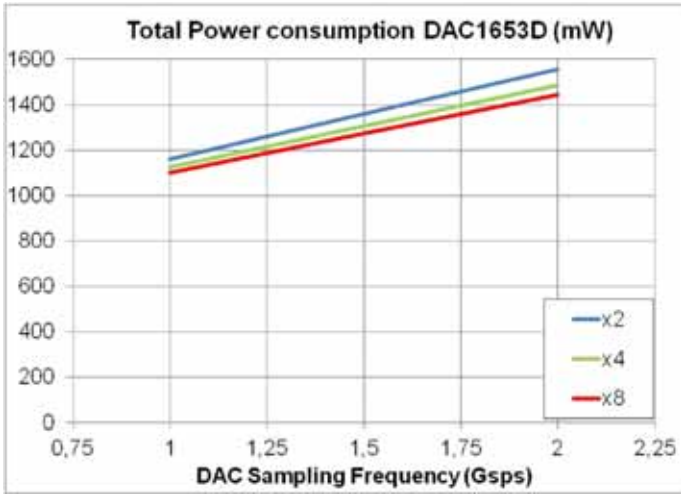

Fig 29. Total Power consumption DAC1653D (mW) depending of the DAC sampling frequency and the interpolation factor (all digital features on)

Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; ; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V(p-p),diff; output common mode voltage = 2.7 V (DAC1658D) or 0.5 V (DAC1653D); unless otherwise specified.

Power supplies consumption for $V_{DDA(3V3)}$ = 3.3 V and $V_{DDA(1V2)}$ = 1.2 V are not dependents of the DAC sampling rate or the interpolation factor.

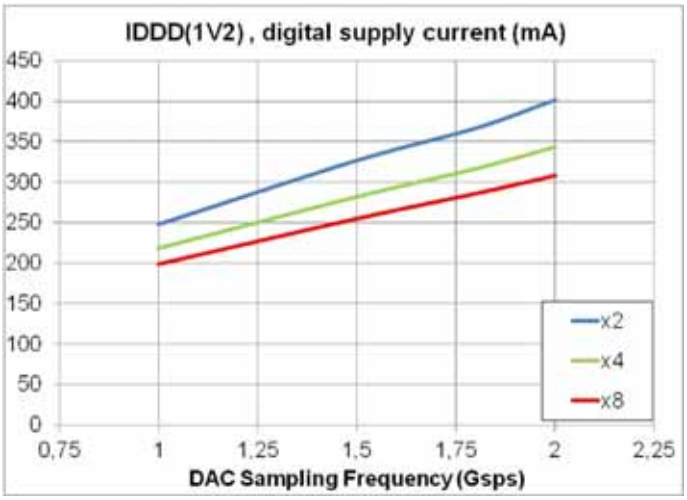

Fig 30. Digital supply current (IDDD(1v2) depending of the DAC sampling frequency and the interpolation factor (all digital features off)

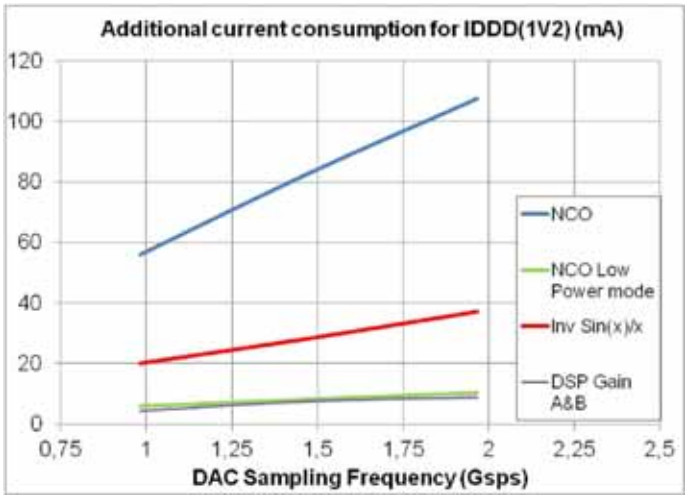

Fig 31. Additional digital supply current for IDDD(1v2) depending of the DAC sampling frequency and digital features

11. Application information

11.1 General description

The DAC165xD is a dual 16-bit DAC operating up to 2.0 Gsps. A maximum input data rate up to 1000 Msps is supported to enable more capability for wideband and multicarrier systems. The incorporated quadrature modulator and 40-bit Numerically Controlled Oscillator (NCO) simplifies the frequency selection of the system. This is also possible because of the ×2, ×4 or ×8 interpolation filters which remove undesired images.

The DAC165xD supports the following JESD204B key features:

- 10-bit/8-bit decoding
- Code group synchronization
- Initial Lane Alignment (ILA)
- $1 + x^{14} + x^{15}$ scrambling polynomial
- Character replacement
- TX/RX synchronization management via SYNC synchronization signals
- Multiple Converter Device Alignment-Multiple Lanes (MCDA-ML) device (subclass 1 compatible)
- Independent Link Synchronization support
- Deterministic latency
- Multiple Device Synchronization (MDS); JESD204B subclass 1 compatible
- Harmonic clocking support
- Number L of serial lanes: 1, 2, 4 (see LMF-S configuration)
- Number M of data converters: 1 or 2 (see LMF-S configuration)
- Number F of octets per frame: 1, 2, 4 (see LMF-S configuration)
- Number S of samples per frame: 1, 2 (see LMF-S configuration)
- Embedded test pattern (PRBS31, PRBS23, PRBS15, PRBS7, JTSPAT, STLTP)

The DAC165xD can be interfaced with any logic device that features high-speed SERializer/DESerializer (SERDES) functionality. This macro is now widely available in Field-Programmable Gate Array (FPGA) of different vendors. Standalone SERDES ICs can also be used.

The DAC165xD includes polarity swapping for each of the lanes and additionally offers lane swapping to enhance the intrinsic board layout simplification of the JESD204B standard. Each physical lane can be configured logically as lane 0, lane 1, lane 2 or lane 3.

This device is MCDA-ML compatible, offering inter lane alignment between several devices. An IDT proprietary mechanism in combination with the JESD204B subclass I clause enables maintenance of sample alignment between devices up to the final analog output stage. Output samples are automatically aligned to the SYSREF signal generated by a dedicated IC or by the FPGA itself. A system with several DAC165xDs can produce data with a guaranteed alignment of less than +/-1 DAC output clock period. The DAC165xD incorporates two differential SYSREF ports (located on opposite sides of the IC) to simplify the PCB layout design. The device also enables independent link reinitialization.

The DAC165xD generates two complementary current outputs on pins IOUTA_P/IOUTA_N and IOUTB_P/IOUTB_N, corresponding to channel 'A' and 'B', respectively, providing a nominal full-scale output current of 20 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.