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DAC1653Q/DAC1658Q

Quad 16-bit DAC: 10 Gbps JESD204B interface: x2, x4 and x8 interpolating

Advance data sheet

Revision 2.3.1

1. General description

DAC1653Q and DAC1658Q are high-speed, high-performance 16-bit quad channel Digital-to-Analog Converters (DACs). The devices provide sample rates up to 2 Gsps with selectable ×2, ×4 and ×8 interpolation filters optimized for multi-carrier and broadband wireless transmitters.

When both devices are referred to in this data sheet, the following convention will be used: DAC165xQ.

The DAC165xQ integrates a JEDEC JESD204B compatible high-speed serial input data interface running up to 10 Gbps over eight differential lanes. It offers numerous advantages over traditional parallel digital interfaces:

- Easier Printed-Circuit Board (PCB) layout
- Lower radiated noise
- Lower pin count
- Self-synchronous link
- Skew compensation
- Deterministic latency
- Multiple Device Synchronization (MDS); JESD204B subclass 1 compatible
- Harmonic clocking support
- Assured FPGA interoperability

There are two versions of the DAC165xQ:

- Low common-mode output voltage (part identification DAC1653Q)
- High common-mode output voltage (part identification DAC1658Q)

Two optional on-chip digital modulator converts the complex I/Q patterns from baseband to IF. The mixer frequency is set by writing to the Serial Peripheral Interface (SPI) control registers associated with the on-chip 40-bit Numerically Controlled Oscillator (NCO). This accurately places the IF carrier in the frequency domain. The 13-bit phase adjustment feature, the 12-bit digital gain and the 16-bit digital offset enable full control of the analog output signals.

The DAC165xQ is fully compatible with device subclass 1 of the JEDEC JESD204B standard, guaranteeing deterministic and repeatable interface latency using the differential SYSREF signal.

Multiple Device Synchronization (MDS) enables multiple DAC channels to be sample synchronous and phase coherent to within one DAC clock period. MDS is ideal for LTE and LTE-A MIMO transceiver applications.

The DAC165xQ includes a very low noise bypass-able integrated Phase-Locked Loop (PLL). This PLL is fully integrated and does not need any external passive components. The device also supports harmonic clocking. Both features are useful to reduce system-level clock synthesis and distribution challenges.

The internal regulator adjusts the full-scale output current between 10 mA and 30 mA.

The device is available in a HLA72 package (10 mm × 10 mm).

2. Features and benefits

- Quad channel 16-bit resolution
- 2 GSps maximum output update rate
- JEDEC JESD204B device subclass I compatible: SYSREF based deterministic and repeatable interface latency
- Multiple device synchronization enables multiple DAC channels to be sample synchronous and phase coherent to within one DAC clock period
- Up to 8 configurable JESD204B serial input lanes running up to 10 Gbps with embedded termination and programmable equalization gain (CTLE)
- SPI interface (3-wire or 4-wire mode) for control setting and status monitoring
- Flexible SPI power supply (1.8 V or 1.2 V) ensuring compatibility with on-board SPI bus
- Differential scalable output current from 10 mA to 30 mA
- Two embedded NCO with 40-bit programmable frequency and 16-bit phase adjustment
- Embedded complex (IQ) digital modulator
- Very low noise bypass-able integrated Phase-Locked Loop (PLL); no external capacitors
- 1.2 V and 3.3 V power supplies (for DAC1653Q series, the 3.3V supply voltage can be lowered to 2.8V for lower power consumption)
- Flexible differential SYNC signals power supply (1.8 V or 1.2 V) ensuring compatibility with on-board devices
- Embedded Temperature Sensor
- Configurable IOs pins for monitoring, interrupt
- XBERT features (PRBS31, 23, 15, 7, JTSPAT, STLTP)
- SFDR = 87 dBc typical (band = Nyquist, f_s = 1.50 Gsps; interpolation ×2; f_{out} = 50 MHz)
- NSD = −164 dBm/Hz typical (f_o = 20 MHz)
- IMD3 = 86 dBc typical (f_s = 1.50 Gsps; interpolation ×2; f_{o1} = 150 MHz; f_{o2} = 151 MHz)
- Four carriers WCDMA ACLR = 75 dBc typical (f_s = 1.50 Gsps; f_{NCO} = 350 MHz)
- RF enable/disable pin and RF automatic mute
- Clock divider by 2, 4, 6 and 8 available at the input of the clock path
- Group delay compensation
- Embedded Power On Reset
- Power-down mode controls
- On-chip 0.7 V reference
- Industrial temperature range −40 °C to +85 °C
- Low (DAC1653Q) or high (DAC1658Q) common-mode output voltage
- HLA 72 pins package (10 mm ´ 10 mm)
- Lane swapping and polarity swapping
- Signal Power Detector, IQ-Range detector, Level detectors with Auto-Mute feature

3. Applications

- Wireless infrastructure radio base station transceivers, including: LTE-A, LTE, MC-GSM, W-CDMA, TD-SCDMA
- LMDS/MMDS, point-to-point microwave back-haul
- Direct Digital Synthesis (DDS) instruments
- High-definition video broadcast production equipment
- Automated Test Equipment (ATE)

4. ORDERING INFORMATION

Table 1. Ordering information

Type number	Package			
	Name	Description	Shipping Packaging	Version
DAC1653Q2G0NAGA8	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tape & Reel	PSC-4438
DAC1653Q1G5NAGA8	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tape & Reel	PSC-4438
DAC1653Q1G0NAGA8	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tape & Reel	PSC-4438
DAC1658Q2G0NAGA8	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tape & Reel	PSC-4438
DAC1658Q1G5NAGA8	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tape & Reel	PSC-4438
DAC1658Q1G0NAGA8	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tape & Reel	PSC-4438
DAC1653Q2G0NAGA	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tray	PSC-4438
DAC1653Q1G5NAGA	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tray	PSC-4438
DAC1653Q1G0NAGA	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tray	PSC-4438
DAC1658Q2G0NAGA	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tray	PSC-4438
DAC1658Q1G5NAGA	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tray	PSC-4438
DAC1658Q1G0NAGA	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tray	PSC-4438

5. BLOCK DIAGRAM

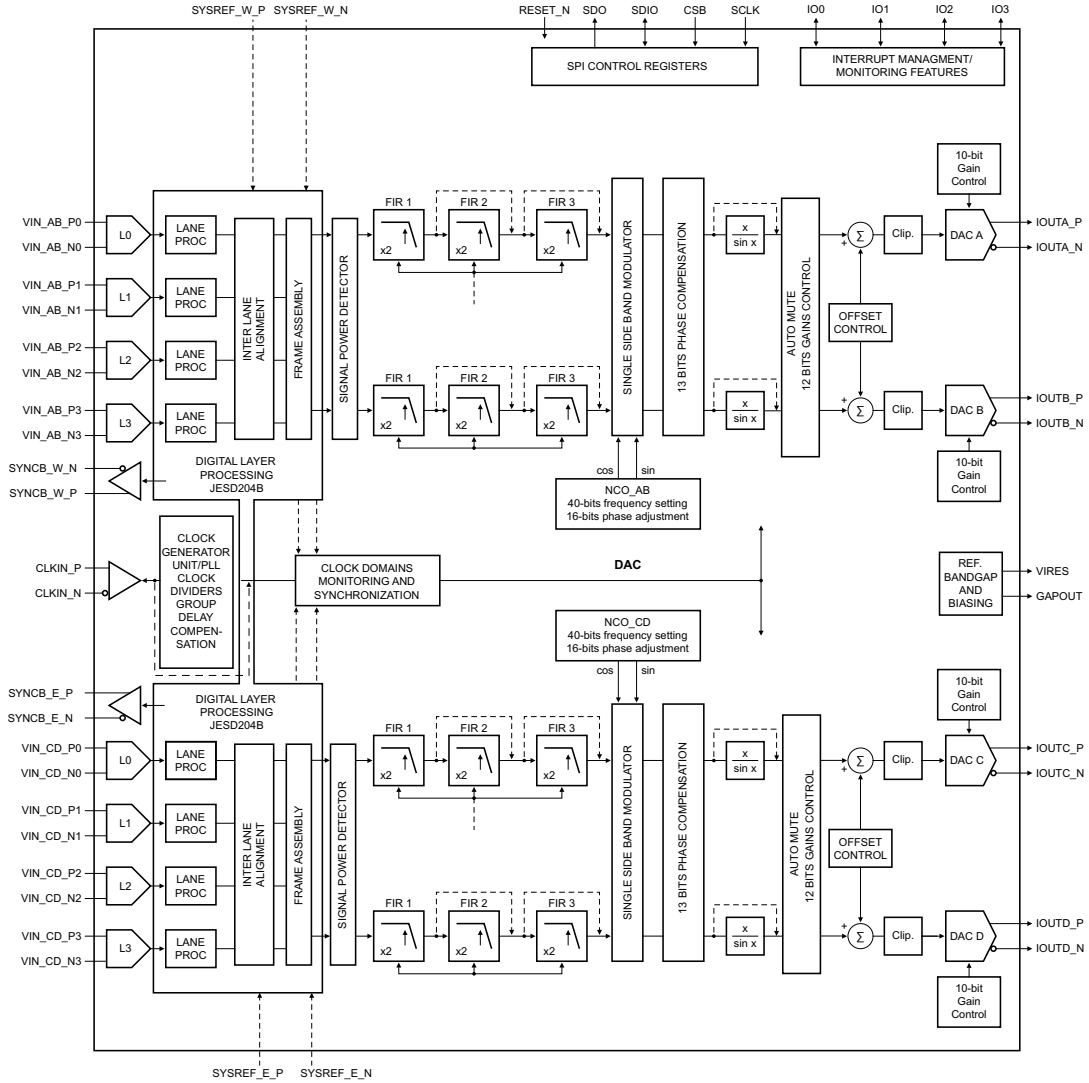

Fig 1. Block diagram

6. PINNING INFORMATION

6.1 Pinning

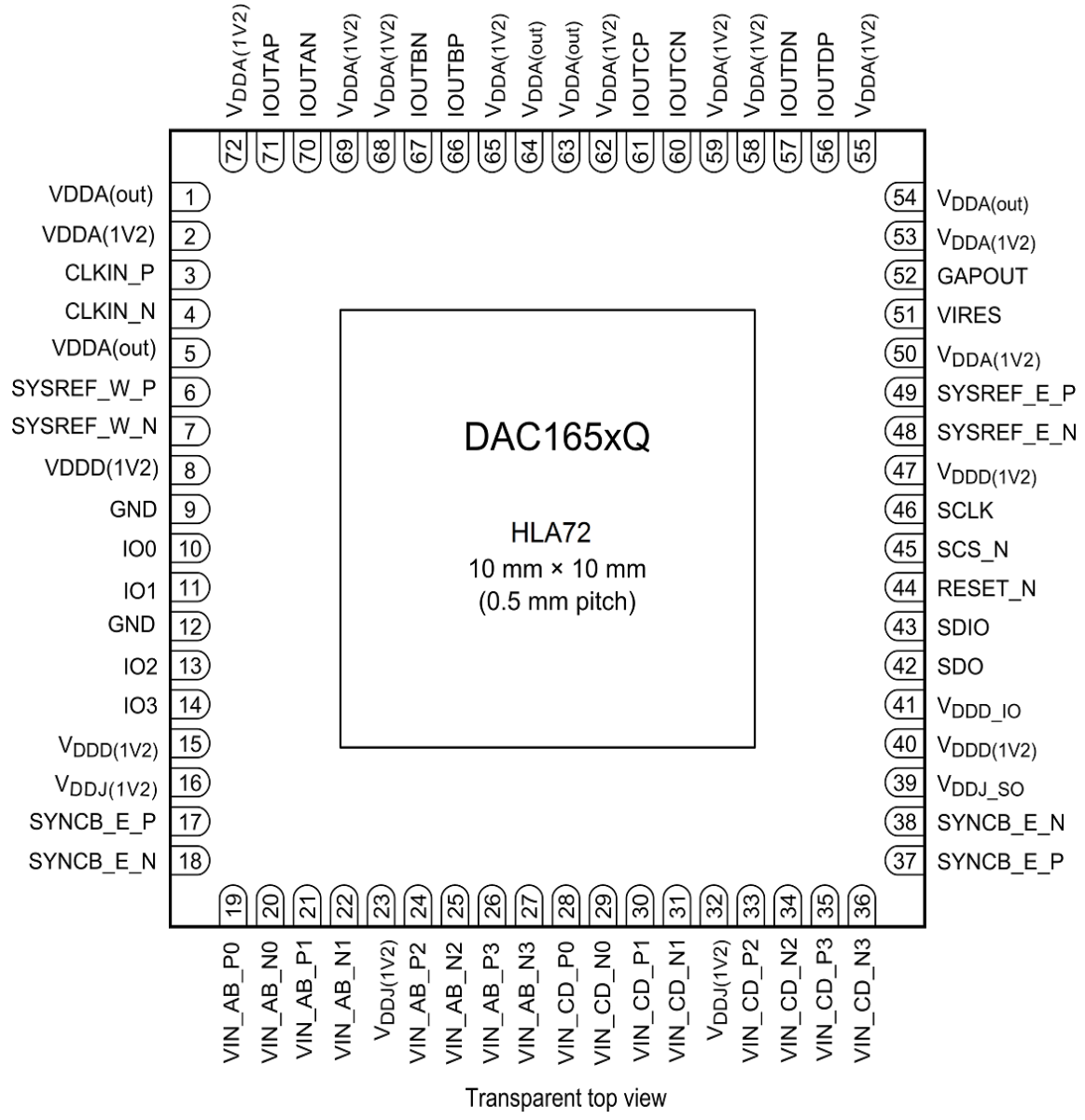

Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
$V_{DDA(out)}$	1	P	DAC output analog power supply
$V_{DDA(1V2)}$	2	P	1.2 V analog power supply
CLKIN_P	3	I	positive clock input (AC coupling recommended ;internal biasing and resistor load included)
CLKIN_N	4	I	negative clock input (AC coupling recommended; internal biasing and resistor load included)
$V_{DDA(out)}$	5	P	DAC output analog power supply
SYSREF_W_P	6	I/O	multiple devices synchronization positive signal, west side (DC coupling recommended)
SYSREF_W_N	7	I/O	multiple devices synchronization negative signal, west side (DC coupling recommended)
$V_{DDD(1V2)}$	8	P	1.2 V digital power supply
GND	9	G	ground
IO0	10	I/O	IO port bit 0
IO1	11	I/O	IO port bit 1
GND	12	G	ground
IO2	13	I/O	IO port bit 2
IO3	14	I/O	IO port bit 3
$V_{DDD(1V2)}$	15	P	1.2 V digital power supply
$V_{DDJ(1V2)}$	16	P	1.2 V JESD204B interface power supply
SYNCB_W_P	17	O	JESD204B SYNC signal, west side positive output (DC coupling recommended)
SYNCB_W_N	18	O	JESD204B SYNC signal, west side negative output (DC coupling recommended)
VIN_AB_P0	19	I	DAC A/B lane 0 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_AB_N0	20	I	DAC A/B lane 0 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
VIN_AB_P1	21	I	DAC A/B lane 1 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_AB_N1	22	I	DAC A/B lane 1 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
$V_{DDJ(1V2)}$	23	P	1.2 V JESD204B interface power supply
VIN_AB_P2	24	I	DAC A/B lane 2 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_AB_N2	25	I	DAC A/B lane 2 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
VIN_AB_P3	26	I	DAC A/B lane 3 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_AB_N3	27	I	DAC A/B lane 3 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
VIN_CD_P0	28	I	DAC C/D lane 0 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_CD_N0	29	I	DAC C/D lane 0 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
VIN_CD_P1	30	I	DAC C/D lane 1 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)

Table 2. Pin description

Symbol	Pin	Type[1]	Description
VIN_CD_N1	31	I	DAC C/D lane 1 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
$V_{DDJ(1V2)}$	32	P	1.2 V JESD204B interface power supply
VIN_CD_P2	33	I	DAC C/D lane 2 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_CD_N2	34	I	DAC C/D lane 2 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
VIN_CD_P3	35	I	DAC C/D lane 3 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_CD_N3	36	I	DAC C/D lane 3 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
SYNCB_E_P	37	O	JESD204B SYNC signal, east side positive output (DC coupling recommended)
SYNCB_E_N	38	O	JESD204B SYNC signal, east side negative output (DC coupling recommended)
V_{DDJ_SO}	39	P	JESD204B SYNC output buffer power supply (1.2 V or 1.8 V)
$V_{DDD(1V2)}$	40	P	1.2 V digital power supply
V_{DDD_IO}	41	P	digital IO power supply (1.2 V or 1.8 V) (including SPI)
SDO	42	O	SPI data output
SDIO	43	I/O	SPI data input/output
RESET_N	44	I	general reset (active LOW)
SCS_N	45	I	SPI chip select (active LOW)
SCLK	46	I	SPI clock input
$V_{DDD(1V2)}$	47	P	1.2 V digital power supply
SYSREF_E_N	48	I/O	multiple devices synchronization negative signal, east side (DC coupling recommended)
SYSREF_E_P	49	I/O	multiple devices synchronization positive signal, east side (DC coupling recommended)
$V_{DDA(1V2)}$	50	P	1.2 V analog power supply
VIRES	51	I/O	biasing resistor (connect this pin to GND through 562ohm resistor)
GAPOUT	52	I/O	bandgap output voltage
$V_{DDA(1V2)}$	53	P	1.2 V analog power supply
$V_{DDA(out)}$	54	P	DAC output analog power supply
$V_{DDA(1V2)}$	55	P	1.2 V analog power supply
IOUTD_P	56	O	DAC D output current
IOUTD_N	57	O	complementary DAC D output current
$V_{DDA(1V2)}$	58	P	1.2 V analog power supply
$V_{DDA(1V2)}$	59	P	1.2 V analog power supply
IOUTC_N	60	O	complementary DAC C output current
IOUTC_P	61	O	DAC C output current
$V_{DDA(1V2)}$	62	P	1.2 V analog power supply
$V_{DDA(out)}$	63	P	DACoutput analog power supply
$V_{DDA(out)}$	64	P	DACoutput analog power supply
$V_{DDA(1V2)}$	65	P	1.2 V analog power supply
IOUTB_P	66	O	DAC B output current
IOUTB_N	67	O	complementary DAC B output current

Table 2. Pin description

Symbol	Pin	Type[1]	Description
$V_{DDA(1V2)}$	68	P	1.2 V analog power supply
$V_{DDA(1V2)}$	69	P	1.2 V analog power supply
IOUTA_N	70	O	complementary DAC A output current
IOUTA_P	71	O	DAC A output current
$V_{DDA(1V2)}$	72	P	1.2 V analog power supply

[1] P: power supply; G: ground; I: input; O: output.

[2] JESD204B input lanes can be swapped between P and N using dedicated registers. The order of lanes can be updated logically (see Section 11.9.5.3).

7. LIMITING VALUES

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDA(out)}$	DAC output analog supply voltage		–0.5	+4.6	V
$V_{DDD(1V2)}$	digital supply voltage		–0.5	+1.5	V
$V_{DDDJ1V2)}$	1.2 V JESD204B interface power supply		–0.5	+1.5	V
$V_{DDA(1V2)}$	analog supply voltage		–0.5	+1.5	V
V_{DDD_IO}	I/O digital supply voltage	pins SDO; SDIO; SCLK; SCS_N; RESET_N; ; IO0; IO1; IO2; IO3	–0.5	2.1	V
V_{DDJ_SO}	digital supply voltage for differential sync output buffers	pins SYNCB_E_P; SYNCB_E_N; SYNCB_W_P; SYNCB_W_N	–0.5	2.1	V
V_I	input voltage for JESD204B lanes	pins VIN_CD_Px; VIN_CD_Nx; VIN_AB_Px; VIN_AB_Nx	–0.5	1.5	V
V_I	input voltage	input pins referenced to GND. pins CLKIN_P, CLKIN_N, SYSREF_W_P, SYSREF_W_N, SYSREF_E_P, SYSREF_E_N	–0.5	1.95	V
V_O	output voltage	pins IOUTA_P; IOUTA_N; IOUTB_P; IOUTB_N;IOUTC_P; IOUTC_N; IOUTD_P; IOUTD_N; referenced to GND	–0.5	+4.6	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		–40	+125	°C

8. THERMAL CHARACTERISTICS

Table 4.Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
JEDEC 4L board					
θ_{JA}	thermal resistance from junction to ambient		[3]	22.5	°C/W
θ_{JC}	thermal resistance from junction to case		[3]	9.3	°C/W
θ_{JB}	thermal resistance from junction to bottom case		[3]	0.4	°C/W
ψ_{JT}	Junction to top characterization parameter		[3]	0.07	°C/W
ψ_{JB}	Junction to board characterization parameter		[3]	0.3	°C/W

[3] In compliance with JEDEC test board in free air; 5.9x7.2mm ePAD soldered down, 48 thermal via

Multi layers board, air flow or heat sinking increases heat dissipation with effective reduction of θ_{JA}. It may be required for sustaining operation at 85°C and fulfill the maximum Junction temperature conditions. The DAC165xQ includes a junction temperature sensor that could be very useful in order to check in real system that the specification of the maximum junction temperature T_j is guarantied (see Section 11.7).

The Table 5 shows evolution of θ_{JA} in several PCB / air flow configuration:

Table 5. θ_{ja} in different PCB / air flow configuration.

PCB configuration	air flow			Unit
	0 m/s	1m/s	2m/S	
4 layers board 48 thermal vias	22.5	18.9	17.4	°C/W
6 layers board 48 thermal vias	18.8	15	13.6	°C/W
12 layers board 48 thermal vias	12.7	9.5	8.5	°C/W

9. STATIC CHARACTERISTICS

9.1 Common characteristics

Table 6. Common characteristics

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; PLL off; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Voltages							
$V_{DDA(out)}$	DAC output analog supply voltage	DAC1658Q: high common mode output	C	3.15	3.3	3.45	V
		DAC1653Q: low common mode output	C	2.5	3.3	3.45	V
$V_{DDD(1V2)}$	digital supply voltage	Fs ≤ 1.5 GHz	C	1.14	1.2	1.26	V
		Fs > 1.5 GHz		1.25	1.3	1.35	V
$V_{DDA(1V2)}$	analog supply voltage	Fs ≤ 1.5 GHz	C	1.14	1.2	1.26	V
		Fs > 1.5 GHz	C	1.25	1.3	1.35	V
V_{DDD_IO}	I/O digital supply voltage		C	1.14	1.2	1.9	V
V_{DDJ_SO}	digital supply voltage for differential SYNC output buffers		C	1.14	1.2	1.9	V
Temperature Sensor							
T_{α}	temperature sensor coefficient		C	-	4.64	-	°C
T_{offset}	temperature sensor offset		C	-	50.3	-	°C
Clock inputs (pins CLKIN_P, CLKIN_N)							
$V_{i(diff)}$	differential Peak-to-Peak voltage		D	400	1000	2000	mV
f_{clkin}	Input frequency compliance range	direct clocking	D			2000	MHz
		harmonic clocking (using clock divider)	D			3000	MHz
f_{ref}	PLL Input frequency compliance range. $f_{ref}=f_{clkin}/prediv$	in PLL mode	C	50	-	123	MHz
f_{dco}	PLL DCO frequency compliance range.	in PLL mode	D	3500	-	4710	MHz
$R_{i(diff)}$	differential input resistor		D	80	100	120	Ω
C_i	input capacitance		D	-	2	-	pF
Digital inputs/outputs (SYSREF_W_P/SYSREF_W_N, SYSREF_E_P/SYSREF_E_N)							
$V_{i(cm)}$	common-mode input voltage	$V_{DDD(IO)}$=1.8V	D	800	1200	1400	mV
		$V_{DDD(IO)}$=1.2V	D	800	950	1100	mV
$V_{i(diff)}$	differential Peak-to-Peak voltage		D	400	800	1000	mV
$R_{i(diff)}$	differential input resistor (could be disconnected see Table 99)		D	-	100	-	Ω

Table 6. Common characteristics

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; PLL off; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
C_i	input capacitance		D	-	1.1	-	pF
Digital inputs (pins , SDIO, SCLK, SCS_N, RESET_N, IO0, IO1, IO2, IO3)							
V_{IL}	LOW-level input voltage		C	GND	-	$0.3V_{DDD\_IO}$	V
V_{IH}	HIGH-level input voltage		C	$0.7V_{DDD\_IO}$	-	V_{DDD_IO}	V
Digital inputs (VIN_Px/VIN_Nx) compliant with the LV-OIF-11G-SR; CML format							
$V_{pp\text{-}diff}$	differential peak-to-peak voltage	below 8 Gbps	C	80	-	-	mV
		above 8 Gbps	C	110	-	-	mV
Z_{diff}	differential impedance	controlled by SPI register	I	71	100	190	Ω
Hi-Z_{diff}	tri-state observed impendance		D	-	64	-	kΩ
DR	data rate		D	2	-	10	Gbps
Digital outputs (pins SYNC_OUT_P and SYNC_OUT_N)							
V_{cm}	common-mode voltage	controlled by SPI register			-		
		V_{DDJ_SO} = 1.8 V	D	1.0	-	1.7	V
		V_{DDJ_SO} = 1.2 V	D	0.4	-	1.1	V
$V_{O(diff)(swing)}$	swing differential output voltage		D	100	-	1200	mV
Digital outputs (pins SDO, SDIO, IO0, IO1, IO2, IO3)							
V_{OL}	LOW-level output voltage		D	-	-	$0.3V_{DDD(IO)}$	V
V_{OH}	HIGH-level output voltage		D	$0.7V_{DDD(IO)}$	-	-	V
Reference voltage output (pin GAPOUT)							
$V_{O(ref)}$	reference output voltage	T_{amb} = 25 °C	C	-	0.70	-	V
DAC output timing							
f_s	sampling rate	DAC165xQ2G0	C	-[2]	-	2000	Msps
		DAC165xQ1G5	C	-[2]	-	1500	Msps
		DAC165xQ1G0	C	-[2]	-	1000	Msps
t_s	settling time	t_o = ±0.5LSB	D	-	20	-	ns

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

[2] Minimum value is linked to the JESD204B link configuration and lane rate

9.2 Specific characteristics

Table 7. Specific characteristics

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC165xQ:			Unit
				Min	Typ	Max	
Currents							
$I_{DDA(out)}$	DAC output analog supply current	DAC1658Q , all use cases	C	-	116		mA
		DAC1653Q, all use cases	C	-	227		mA
I_{DDD_IO}	digital supply current for IO pins	depends on SPI and IO0/IO1/IO2/IO3 activity	C	-	< 1		mA
I_{DDD_SO}	digital supply current for SYNC pins	V_{DDD_SO} = 1.2 V	C	-	23		mA
		V_{DDD_SO} = 1.8 V	C	-	38		mA
$I_{DDD(1V2)}$	digital supply current	NCO off; ×4 interpolation; DLQ LMF222;					
		f_s = 983.04 Msps	C	-	361		mA
		f_s = 1228.8 Msps	C	-	429		mA
		f_s = 1474.56 Msps	C	-	497		mA
		NCO on at 150 MHz; ×4 interpolation; DLQ LMF222					
		f_s = 983.04 Msps	C	-	521		mA
		f_s = 1228.8 Msps	C	-	589		mA
		f_s = 1474.56 Msps	C	-	712		mA
$I_{DDA(1V2)}$	analog supply current	$V_{DDA(1V2)}$ = 1.2 V	C	-	371		mA
		$V_{DDA(1V2)}$ = 1.3 V	C	-	380		mA

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

Table 8. Specific characteristics

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658Q: High common-mode			DAC1653Q: .Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
Power										
P_{tot}	total power dissipation	f_s = 983.04 Msps; DLQ LMF222, NCO off; ×4 interpolation;	C	-	1371	-	-	1738	-	mW
		f_s = 1228.8 Msps; DLQ LMF222, NCO off; ×4 interpolation;	C	-	1457	-	-	1823	-	mW
		f_s = 1474.56 Msps; DLQ LMF222, NCO off; ×4 interpolation;	C	-	1543	-	-	1909	-	mW
		f_s = 1474.56 Msps; DLQ LMF222, NCO off; ×4 interpolation; $V_{DDA(out)}$ = 2.8 V;	C	-	na	-	-	1793	-	mW
		f_s = 983.04 Msps; DLQ LMF422, NCO off; ×2 interpolation;	C	-	1491	-	-	1857	-	mW
		f_s = 983.04 Msps; DLQ LMF222, NCO on; ×4 interpolation;	C	-	1371	-	-	1738	-	mW
		f_s = 983.04 Msps; DLQ LMF222, NCO off; ×4 interpolation;PLL on	C	-	1506	-	-	1872	-	mW
		full power-down	C	-	12	-	-	12	-	mW
Analog outputs (pins IOUTA_P, IOUTA_N, IOUTB_P, IOUTB_N, OUTC_P, IOUTC_N, IOUTD_P, IOUTD_N,)										
$I_{O(fs)}$	full-scale output current		D	10	20	30	10	20	30	mA
I_{bias}	DAC output biasing current	this additional current has to be used in order to calculate DAC output common mode voltage (Vcm)	D	-	1.6	-	-	1.6	-	mA
$I_{aux(fs)}$	AUX DAC full-scale output current	normal resolution	I	-	2.3	-	-	2.3	-	mA
		high resolution	D	-	0.04	-	-	0.04	-	mA
V_{O_comp}	output voltage compliance range	$V_{DDA(out)}$ =3.3 V	D	$V_{DDA(out)}$ -1.0	-	$V_{DDA(out)}$	$V_{DDA(out)}$ -1.0	-	$V_{DDA(out)}$	V
		$V_{DDA(out)}$ =2.5 V	D	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.	V
R_o	internal output resistance		D	-	250	-	-	250	-	kΩ

Table 8. Specific characteristics

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658Q: High common-mode			DAC1653Q: .Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
C_{PN}	differential output capacitance		D	-	0.5	-	-	0.5	-	pF
C_P	positive output capacitance		D	-	8.4	-	-	8.4	-	pF
C_N	negative output capacitance		D	-	8.3	-	-	8.3	-	pF

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

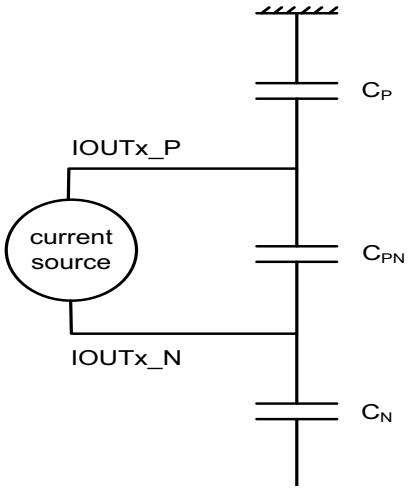

Fig 3. DAC output simplified model

10. Dynamic characteristics

Table 9. Dynamic characteristics DAC165xQ

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; no auxiliary DAC used; PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3 V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	DAC1658Q High common-mode Typical values			DAC1653Q Low common-mode Typical values			Unit
			f_s	1 Gsps	1.5 Gsps	2 Gsps	1 Gsps	1.5 Gsps	2 Gsps	
SFDR	spurious-free dynamic range	interpolation x4								
		BW = f_s / 2								
		$V_{DDA(out)}$ = 3.3 V; f_o = 20 MHz								
		at −1 dBFS	C		85			88		dBc
		at −7 dBFS	C		82			82.5		dBc
		at −14 dBFS	C		76			75		dBc
		$V_{DDA(out)}$ = 3.3 V; f_o = 150 MHz								
		at −1 dBFS	C		81			80		dBc
		at −7 dBFS	C		79			77		dBc
		at −14 dBFS	C		73			73		dBc
		$V_{DDA(out)}$ = 3.3 V; f_o = 280 MHz								
		at −1 dBFS	C		72			74		dBc
		at −7 dBFS	C		72			75		dBc
		at −14 dBFS	C		67			71.5		dBc
$SFDR_{woH2/H3}$	spurious-free dynamic range without H2 or H3	interpolation x4; BW = f_s / 2; $V_{DDA(out)}$ = 3.3 V; f_o = 150 MHz								
		at −1 dBFS	C		83.5			84.5		dBc
		at −7 dBFS	C		81			82		dBc
		at −14 dBFS	C		73			74		dBc
IMD3	third-order intermodulation distortion	$V_{DDA(out)}$ = 3.3 V; f_{o1} = 20 MHz; f_{o2} = 21 MHz; −9 dBFS per tone	C		98			94		dBc
		$V_{DDA(out)}$ = 3.3 V; f_{o1} = 210 MHz; f_{o2} = 211 MHz; −9 dBFS per tone	C		87			83		dBc
ACLR	adjacent channel power ratio	f_o = 50 MHz								
		1 WCDMA carrier; BW = 5 MHz	C		82			81		dBc
		4 WCDMA carriers; BW = 20 MHz	C		78			76		dBc

Table 9. Dynamic characteristics DAC165xQ

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; no auxiliary DAC used; PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3 V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	DAC1658Q High common-mode Typical values			DAC1653Q Low common-mode Typical values			Unit
			f_s	1 Gsps	1.5 Gsps	2 Gsps	1 Gsps	1.5 Gsps	2 Gsps	
		f_o = 350 MHz								
		1 WCDMA carrier; BW = 5 MHz	C		81			80		dBc
		4 WCDMA carriers; BW = 20 MHz	C		77			75		dBc
Channel Isolation	DAC B <-> C direct crosstalk	f_o = 20 MHz	C		tbd			>95		dBc
NSD	noise spectral density	f_o = 70 MHz at −1 dBFS	C		tbd			−163		dBc/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used;PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3 V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

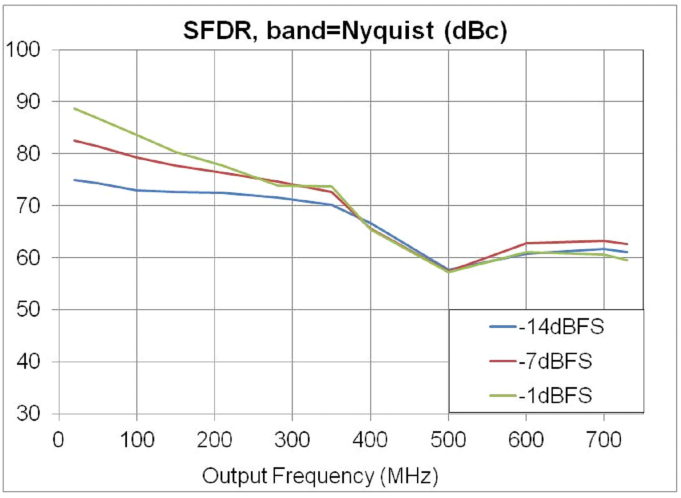

Fig 4. SFDR(dBc) over Nyquist depending on Fout (MHz) and input level (dBFS)

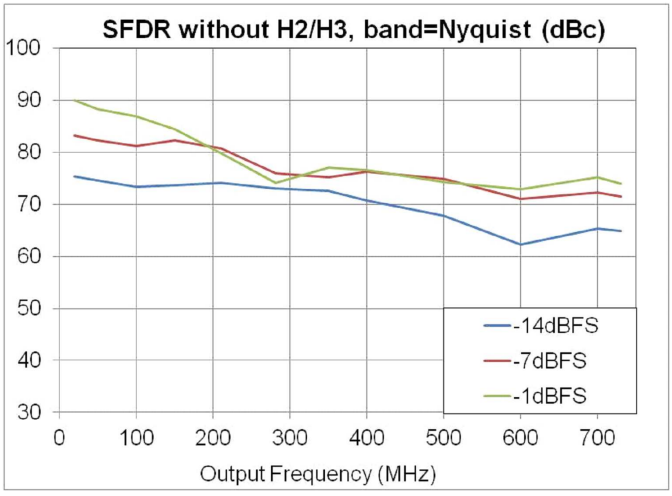

Fig 5. SFDR without H2 and H3 (dBc) over Nyquist depending on Fout (MHz) and input level (dBFS)

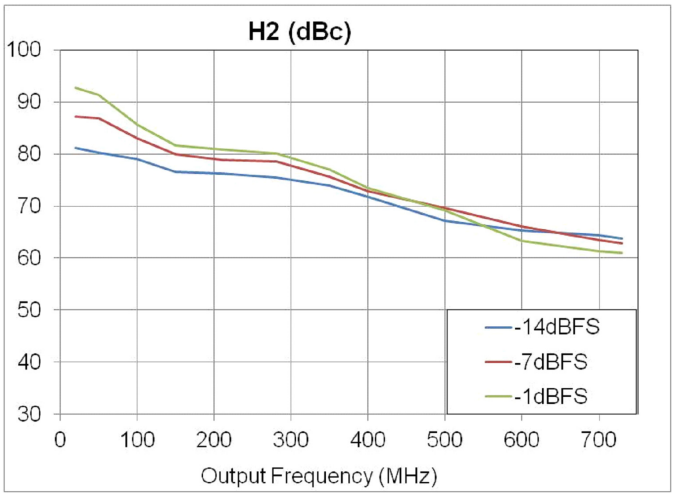

Fig 6. H2 (dBc) over Nyquist depending on Fout (MHz) and input level (dBFS)

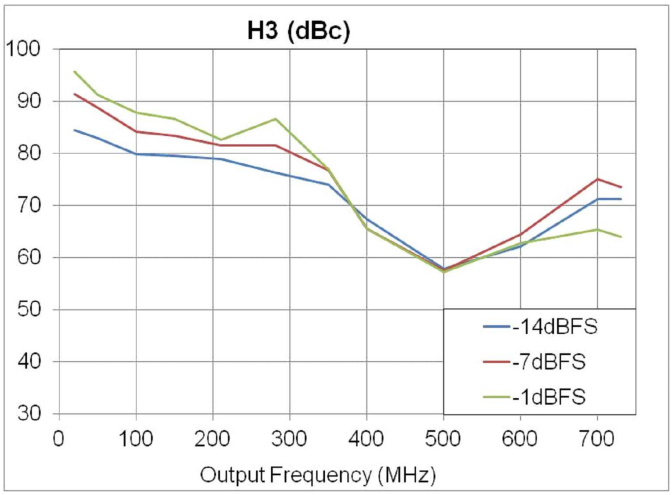

Fig 7. H3 (dBc) over Nyquist depending on Fout (MHz) and input level (dBFS)

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used;PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

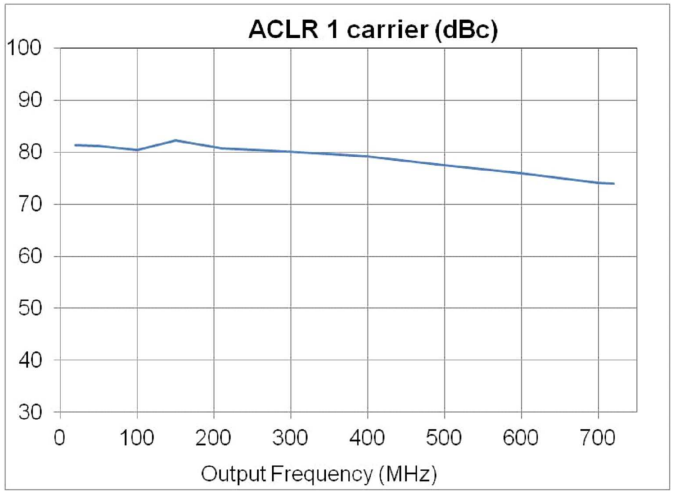

Fig 8. ACLR 1 carrier (dBc) for WCDMA depending on Fout (MHz)

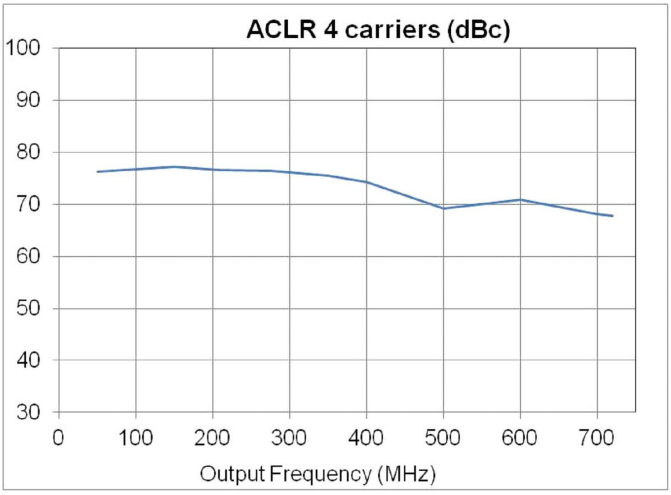

Fig 9. ACLR 4 carriers (dBc) for WCDMA depending on Fout (MHz)

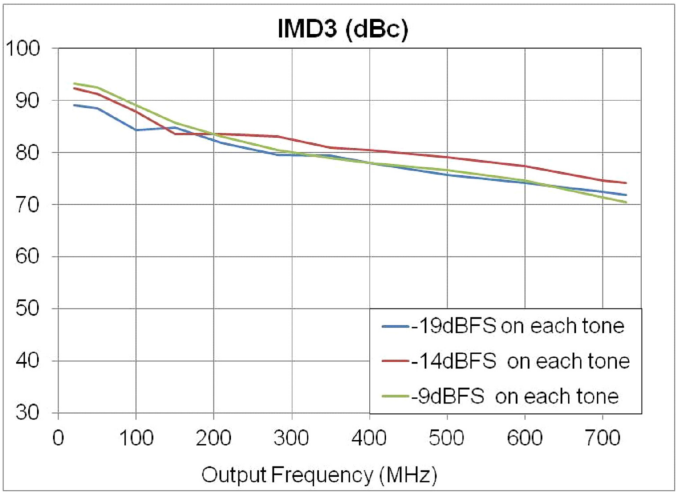

Fig 10. IMD3 (dBc) (1 MHz spacing) depending on Fout (MHz) and input level per tone (dBFS)

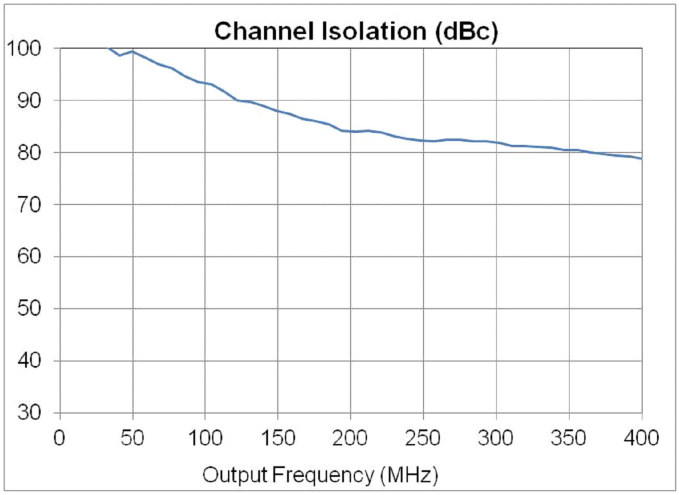

Fig 11. Channel isolation DAC B <--> DAC C direct crosstalk (dBc) depending on Fout (MHz)

VDDA(out) = 3.3 V; VDDA(1V2) = 1.2 V; VDDD(1V2) = 1.2 V; Typical values measured at Tamb = +25 °C; IO(fs) = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3 V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

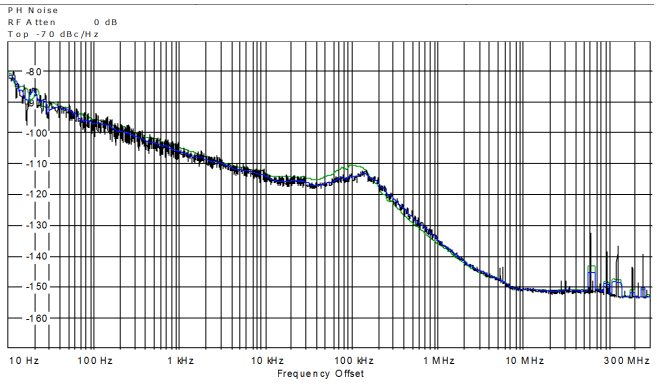

Fig 12. PLL Phase noise (dBc/Hz)

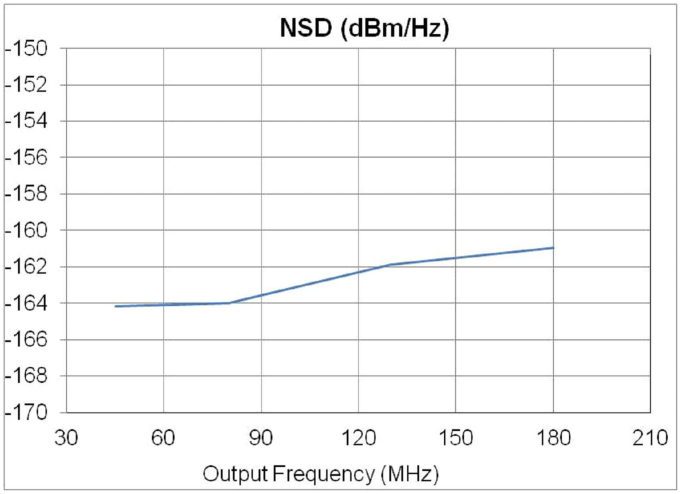

Fig 13. DAC1653Q NSD (dBm/Hz) depending on Fout (MHz) and input level per tone (dBFS)

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used;PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3 V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

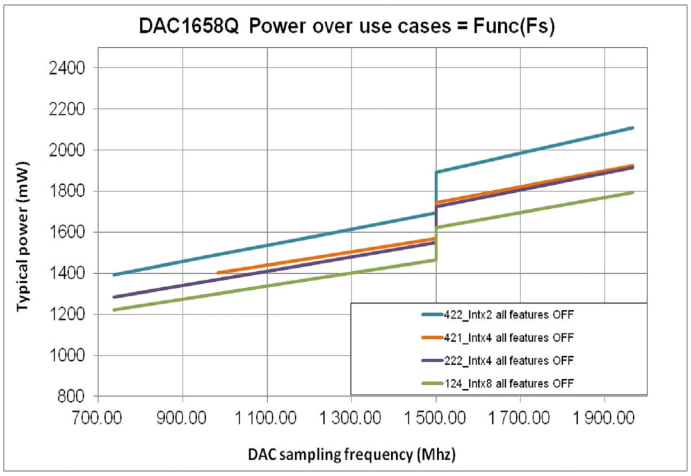

Fig 14. DAC1658Q total power dissipation (mW) depending on sampling frequency Fs (all digital feature off)

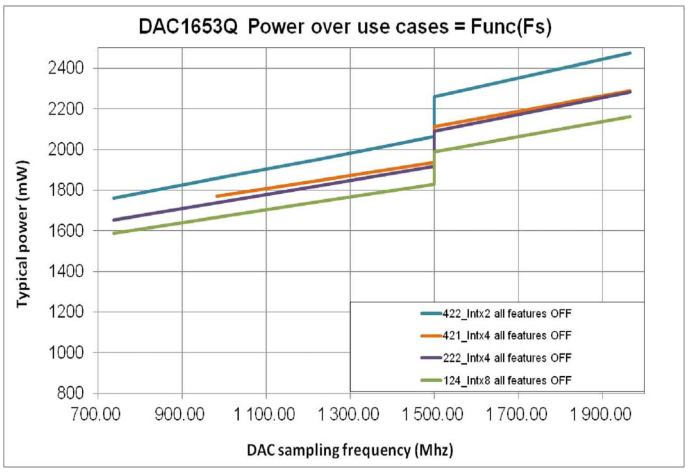

Fig 15. DAC1653Q total power dissipation (mW) depending on sampling frequency Fs (all digital feature off)

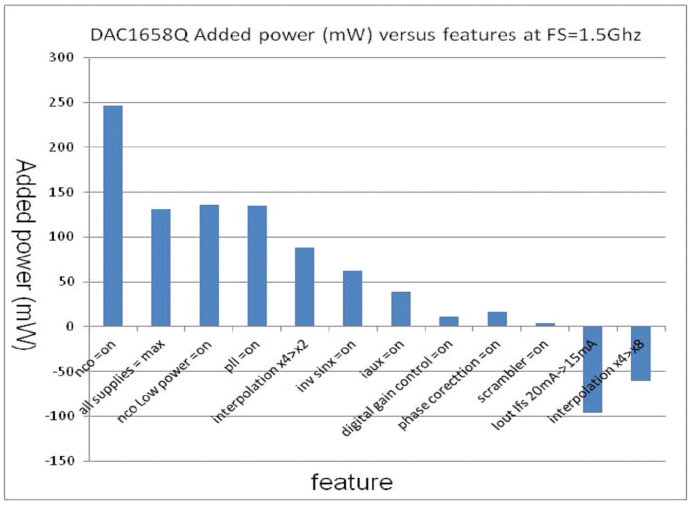

Fig 16. DAC1658Q additional power dissipation (mW) depending on added feature at Fs= 1.5 GHz

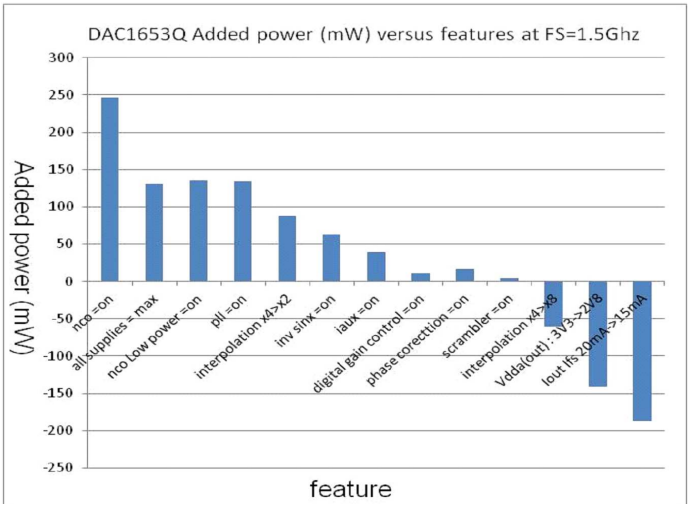

Fig 17. DAC1653Q additional power dissipation (mW) depending on added feature at Fs= 1.5 GHz

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used;PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3 V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

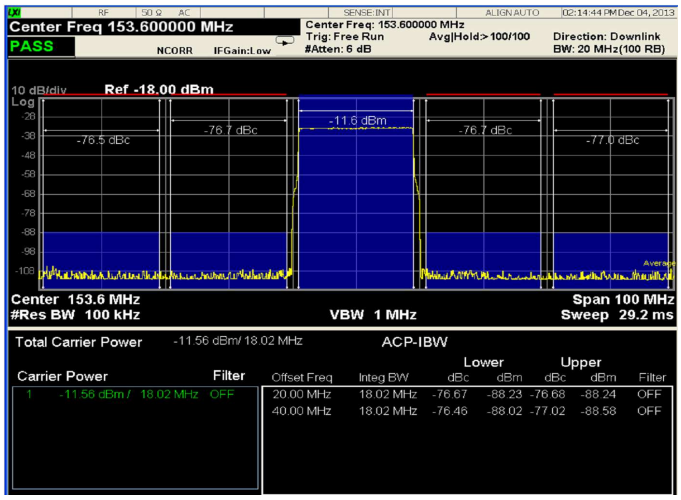

Fig 18. : ACLR of 1 carrier LTE (BW=20 MHz) centered at 153.6 MHz

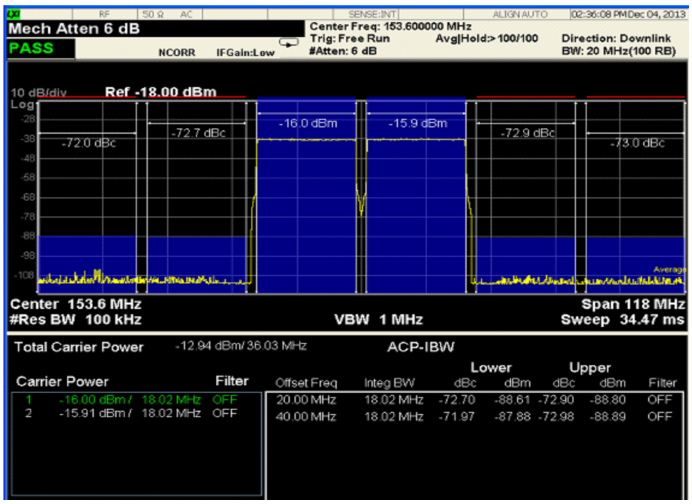

Fig 19. : ACLR of 2 carriers LTE (BW=2 x 20 MHz) centered at 153.6 MHz

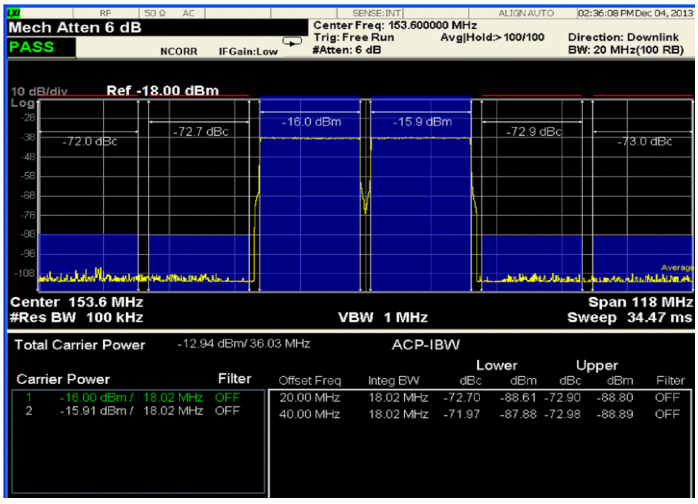

Fig 20. : ACLR of 1 carrier LTE (BW=20 MHz) centered at 350 MHz

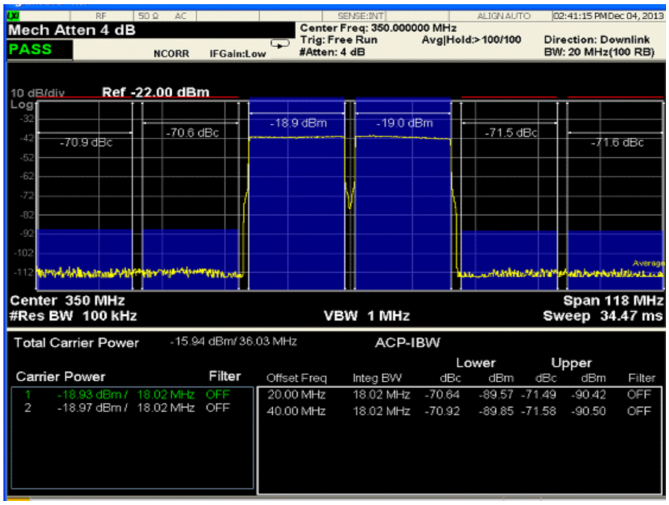

Fig 21. : ACLR of 2 carriers LTE (BW=2 x 20 MHz) centered at 350 MHz

11. Application information

11.1 General description

The DAC165xQ is a quad 16-bit DAC operating up to 2 Gsps. A maximum input data rate up to 1000 Msps is supported to enable more capability for wideband and multicarrier systems. The incorporated quadrature modulator and 40-bit Numerically Controlled Oscillators (NCOs) simplifies the frequency selection of the system. This is also possible because of the ×2, ×4 or ×8 interpolation filters which remove undesired images.

The DAC165xQ embeds four DAC channels (A, B, C and D) that can be configured as a Single Link Quad (SLQ) in which all four DACs are synchronized together or as two Dual Link Quad (DLQ) in which the two dual DACs (A/B and C/D) are synchronized independently. The two NCOs are linked to the A/B and the C/D dual DACs, respectively. Regarding the quad/dual mode used, the eight JESD204B lanes are configured as one single link configuration JESD204 link (one SYNC signal for a specified number of lanes), or dual link configuration JESD204B links (two SYNC signals associated with a specified number of lanes).

The DAC165xQ supports the following JESD204B key features:

- 10-bit/8-bit decoding
- Code group synchronization
- Initial Lane Alignment (ILA)
- $1 + x^{14} + x^{15}$ scrambling polynomial
- Character replacement
- TX/RX synchronization management via SYNC synchronization signals
- Multiple Converter Device Alignment-Multiple Lanes (MCDA-ML) device (subclass 1 compatible)
- Independent Link Synchronization support
- Deterministic latency
- Multiple Device Synchronization (MDS); JESD204B subclass 1 compatible
- Harmonic clocking support
- Number L of serial lanes: 1, 2, 4 or 8 (see LMF-S configuration)
- Number M of data converters: 1,2 or 4 (see LMF-S configuration)
- Number F of octets per frame: 1, 2, 4 (see LMF-S configuration)
- Number S of samples per frame: 1, 2 (see LMF-S configuration)
- Embedded test pattern (PRBS31, PRBS23, PRBS15, PRBS7, JTSPAT, STLTP)

The DAC165xQ can be interfaced with any logic device that features high-speed SERializer/DESerializer (SERDES) functionality. This macro is now widely available in Field-Programmable Gate Array (FPGA) of different vendors. Standalone SERDES ICs can also be used.

The DAC165xQ includes polarity swapping for each of the lanes and additionally offers lane swapping to enhance the intrinsic board layout simplification of the JESD204B standard. Within each group of 4 lanes each physical lane can be configured logically as lane 0, lane 1, lane 2 or lane 3.

This device is MCDA-ML compatible, offering inter lane alignment between several devices. An IDT proprietary mechanism in combination with the JESD204B subclass I clause enables maintenance of sample alignment between devices up to the final analog output stage. Output samples are automatically aligned to the SYSREF signal generated by a dedicated IC or

by the FPGA itself. A system with several DAC165xQs can produce data with a guaranteed alignment of less than +/-1 DAC output clock period. The DAC165xQ incorporates two differential SYSREF ports (located on opposite sides of the IC) to simplify the PCB layout design. The device also enables independent link reinitialization.

The DAC165xQ generates four complementary current outputs on pins IOUTA_P/IOUTA_N and IOUTB_P/IOUTB_N, IOUTC_P/IOUTC_N, and IOUTD_P/IOUTD_N corresponding to channel 'A', 'B', 'C', and 'D', respectively, providing a nominal full-scale output current of 20 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.

The DAC165xQ requires configuration before operating. It features an SPI slave interface to access the internal registers. Some of these registers also provide information about the JESD204B interface status. Optionally, an interrupt capability can be programmed using those registers to ensure ease of use of the device.

Because of the JESD204B standardization, the DAC165xQ does not require any adjustment from the Transmit Logic Device (TLD) to capture the input data streams. Some autolock features can be monitored using the SPI registers.

The DAC165xQ supports the following LMF configuration as described in the JESD204B standard (register XY_LMF_CNTRL (00DEh 02DEh 04DEh)):

Table 10. LMF configuration if DAC165xQ configures in dual JEDS204B links

Link configuration	L-M-F	S[1]	HD[2]
dual link (DLQ)	1-2-4	1	0
dual link (DLQ)	2-2-2	1	0
dual link (DLQ)	4-2-2	2	0
dual link (DLQ)	4-2-1	1	1
single link (SLQ)	2-4-4	2	0
single link (SLQ)	4-4-2	2	0
single link (SLQ)	8-4-2	4	0
single link (SLQ)	8-4-1	2	1

[1] S is the number of samples per frame.

[2] HD is the high-density bit as described in the JESD204B specification.

A new IDT auto-mute feature enables switching off of the RF output signal as a result of various internal events occurring.

A signal level detector allows auto-muting of the DAC outputs if they exceed the detection limit.

The DAC165xQ requires 3.3 V and 1.2 V power supplies. The 1.2 V supply has separate digital and analog power supply pins.

In order to program the device in LMF841 (SLQ) configuration, each DAC AB and DAC CD instance of XY_LMF_CNTRL registers will have to be programmed in LMF421. In parallel, SLQ configuration (common ILA, common sync) must also be selected. Same apply, in order to get SLQ LMF842/LMF442/LMF244 configuration, LMF422/LMF222/LMF124 will have to be programmed for each dual DAC.

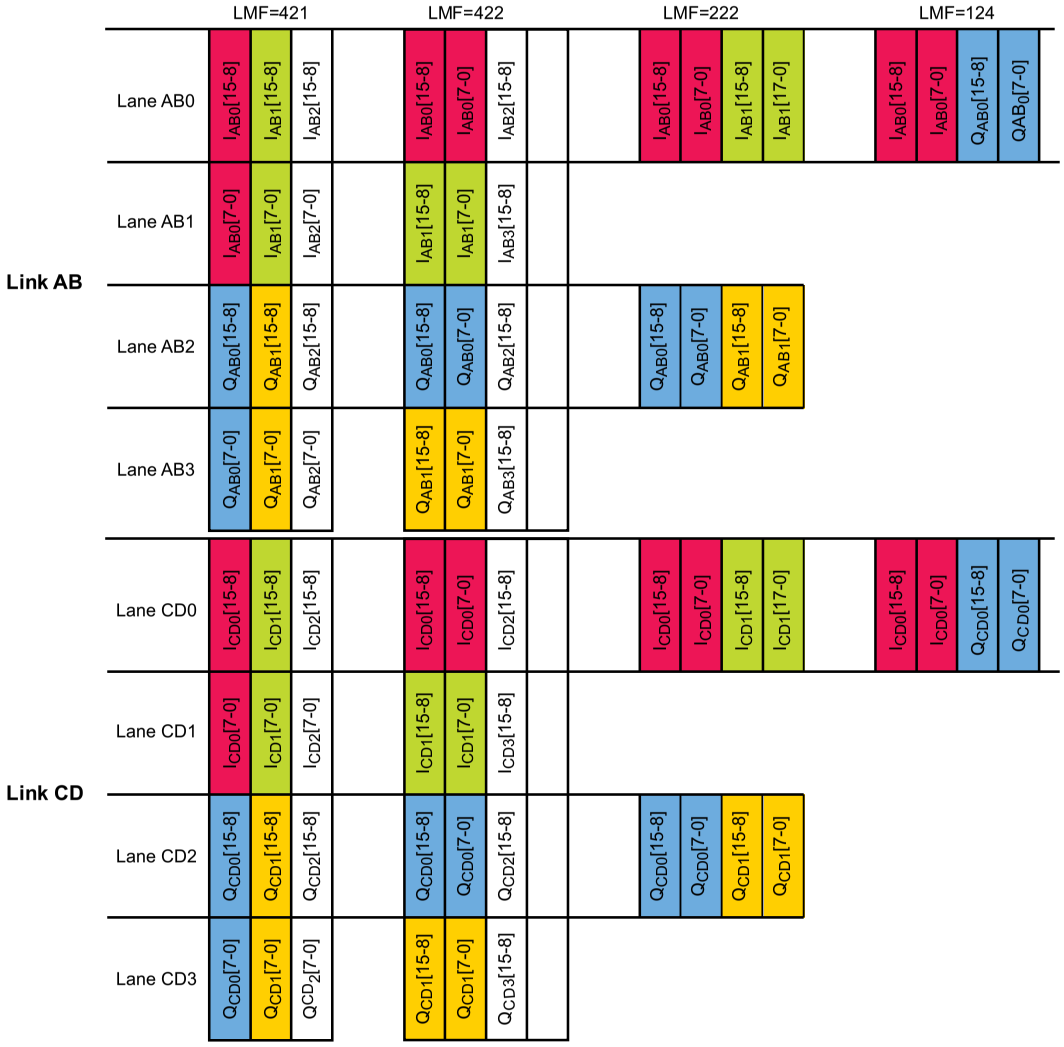

Fig 22. Frame assembly byte representation