Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Qualcomm Technologies International, Ltd.

Qualcomm Technologies International, Ltd.
Churchill House
Cambridge Business Park
Cambridge, CB4 0WZ
United Kingdom

CSR µEnergy® CSR1000™ QFN

Bluetooth low energy Single-mode IC

Production Information

CSR1000A04

Issue 4

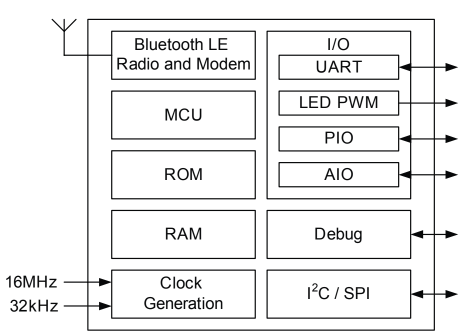
Features

- 128KB memory: 64KB RAM and 64KB ROM
- Bluetooth® v4.0 specification
- 7.5dBm Bluetooth low energy maximum transmit output power
- -92.5dBm Bluetooth low energy receive sensitivity
- Support for Bluetooth v4.0 specification host stack including ATT, GATT, SMP, L2CAP, GAP
- RSSI monitoring for proximity applications
- <600nA current consumption in dormant mode
- 32kHz and 16MHz crystal or system clock
- Switch-mode power supply
- Programmable general purpose PIO controller
- 10-bit ADC
- 12 digital PIOs
- 3 analogue AIOs
- UART
- I²C / SPI for EEPROM / flash memory ICs and peripherals
- Debug SPI
- 3 PWM modules
- Wake-up interrupt and watchdog timer
- QFN 32-lead, 5 x 5 x 0.6mm, 0.5mm pitch

General Description

CSR1000 QFN is a CSR µEnergy platform device. CSR µEnergy are CSR's single-mode Bluetooth low energy products for the Bluetooth Smart market.

CSR µEnergy enables ultra low-power connectivity and basic data transfer for applications previously limited by the power consumption, size constraints and complexity of other wireless standards. The CSR µEnergy platform provides everything required to create a Bluetooth low energy product with RF, baseband, MCU, qualified Bluetooth v4.0 stack and customer application running on a single IC.



Applications

- Building an ecosystem using Bluetooth low energy

CSR is the industry leader for Bluetooth low energy, also known as Bluetooth Smart. Bluetooth Smart energy enables the transfer of simple data sets between compact devices opening up a completely new class of Bluetooth applications such as watches, TV remote controls, medical sensors and fitness trainers.

Bluetooth low energy takes less time to make a connection than conventional Bluetooth wireless technology and can consume approximately 1/20th of the power of Bluetooth Basic Rate. CSR1000 QFN supports profiles for sensors, watches, HIDs and time synchronisation.

Typical Bluetooth low energy applications:

- Sports and fitness
- Healthcare
- Home entertainment
- Office and mobile accessories
- Automotive
- Commercial
- Watches
- Human interface devices

Ordering Information

Device	Package			Order Number
	Type	Size	Shipment Method	
CSR1000 QFN	QFN-32-lead (Pb free)	5 x 5 x 0.6mm 0.5mm pitch	Tape and reel	CSR1000A04-IQQM-R

Note:

The minimum order quantity is 2kpcs taped and reeled.

Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

CSR1000 QFN Development Kit Ordering Information

Description	Order Number
CSR1000 QFN Development Kit example design	DK-CSR1000-10048-3A

Contacts

General information	www.csr.com
Information on this product	Sales@csr.com
Customer support for this product	www.csrsupport.com
Details of compliance and standards	Product.compliance@csr.com
Help with this document	Comments@csr.com

Device Details

Bluetooth Radio

- On-chip balun (50Ω impedance in TX and RX modes)
- No external trimming is required in production
- Bluetooth v4.0 specification compliant

Bluetooth Transmitter

- 7.5dBm RF transmit power with level control from integrated 6-bit DAC over a dynamic range >30dB
- No external power amplifier or TX/RX switch required

Bluetooth Receiver

- -92.5dBm sensitivity
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Fast AGC for enhanced dynamic range

Bluetooth Stack

CSR's protocol stack runs on the integrated MCU:

- Support for Bluetooth v4.0 specification features:
  - Master and slave operation
  - Including encryption
- Software stack in firmware includes:
  - GAP
  - L2CAP
  - Security manager
  - Attribute protocol
  - Attribute profile
  - Bluetooth low energy profile support

Synthesiser

- Fully integrated synthesiser requires no external VCO varactor diode, resonator or loop filter

Baseband and Software

- Hardware MAC for all packet types enables packet handling without the need to involve the MCU

Physical Interfaces

- SPI master interface
- SPI programming and debug interface
- I^2C
- Digital PIOs
- Analogue AIOs
- UART

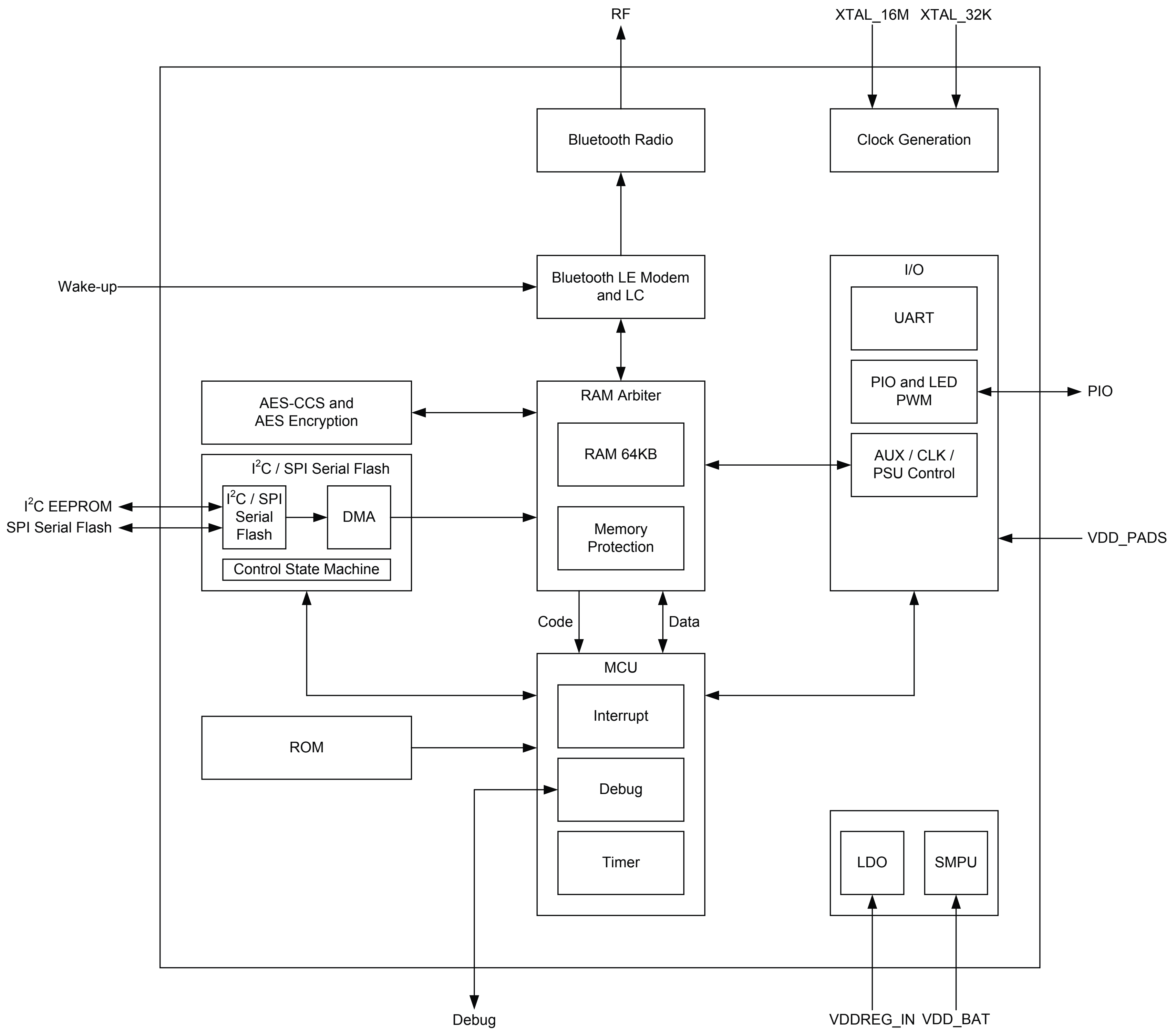
Auxiliary Features

- Battery monitor
- Power management features include software shutdown and hardware wake-up
- CSR1000 QFN can run in low power modes from an external 32.768kHz clock signal
- Integrated switch-mode power supply
- Linear regulator (internal use only)
- Power-on-reset cell detects low supply voltage

Package

- 32-lead 5 x 5 x 0.6mm, 0.5mm pitch QFN

Functional Block Diagram



Document History

Revision	Date	Change Reason
1	21 JUL 11	Original publication of this document.
2	27 OCT 11	Updates to Absolute Maximum Ratings, Recommended Operating Conditions and CSR Green Semiconductor Products and RoHS Compliance details.
3	06 JAN 12	Updates to schematic and wake-up options.
4	08 APR 13	Updates include: ▪ Removal of NDA statement. ▪ Temperature sensor added. ▪ Battery monitor added. ▪ SPI timing diagram added. ▪ Change from VDD to VDD_PADS in Digital Terminals. ▪ Auxiliary ADC and DAC parameters added.

Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Life Support Policy and Use in Safety-critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

CSR Green Semiconductor Products and RoHS Compliance

CSR1000 QFN devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). CSR1000 QFN devices are also free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals. For more information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products*.

Confidentiality Status

This document is non-confidential. The right to use, copy and disclose this document may be subject to license restrictions in accordance with the terms of the agreement entered into by CSR plc and the party that CSR plc delivered this document to.

Trademarks, Patents and Licences

Unless otherwise stated, words and logos marked with ™ or ® are trademarks registered or owned by CSR plc or its affiliates. Bluetooth ® and the Bluetooth ® logos are trademarks owned by Bluetooth ® SIG, Inc. and licensed to CSR. Other products, services and names used in this document may have been trademarked by their respective owners.

The publication of this information does not imply that any license is granted under any patent or other rights owned by CSR plc and/or its affiliates. Neither the whole nor any part of the information contained in, or the product described in, this document may be adapted or reproduced in any material form except with the prior written permission of the copyright holder.

CSR reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

Refer to www.csrsupport.com for compliance and conformance to standards information.

Contents

List of Figures

List of Tables

1 Package Information

1.1 Pinout Diagram

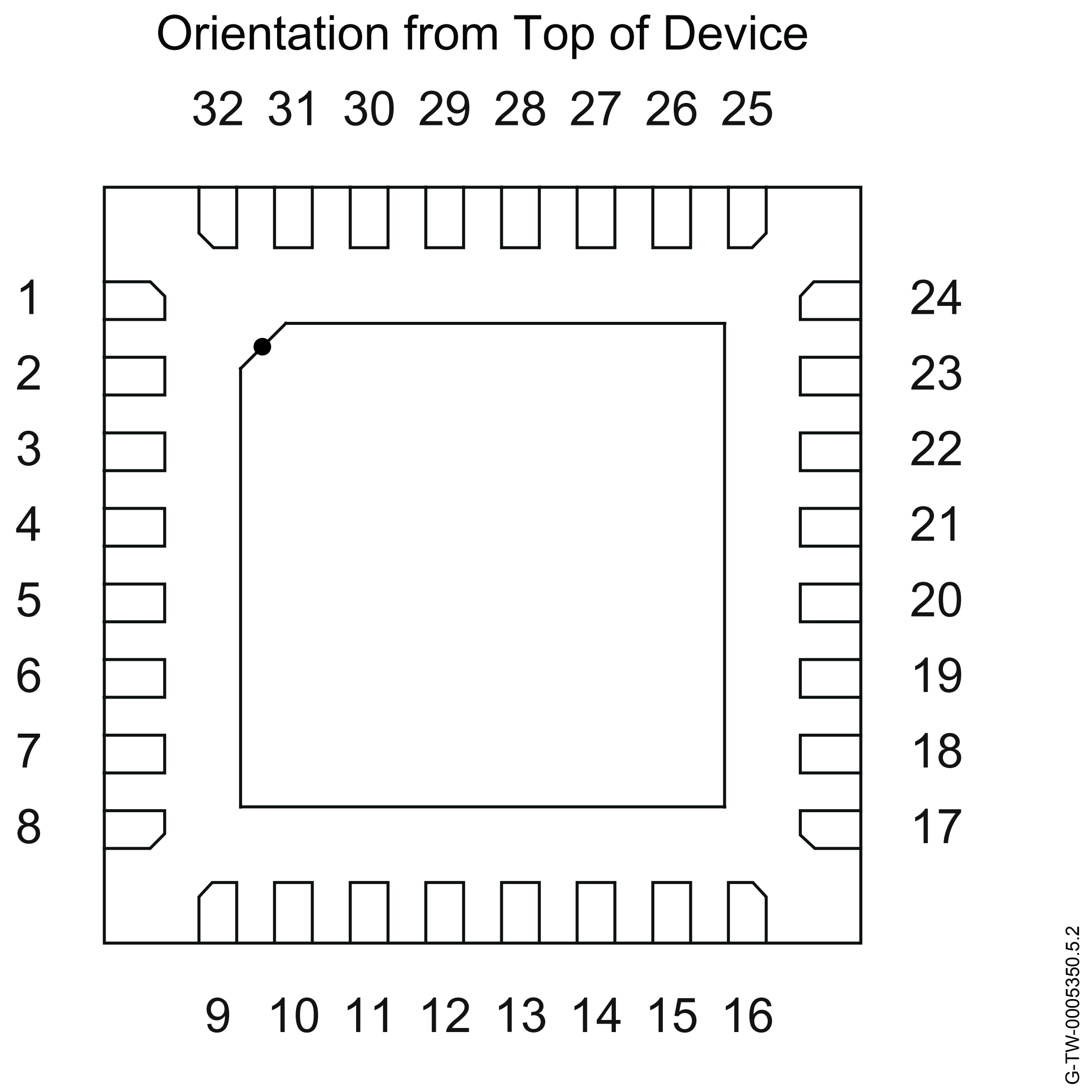


Figure 1.1: Pinout Diagram

CSR1000 QFN Data Sheet

1.2 Device Terminal Functions

Radio	Lead	Pad Type	Supply Domain	Description
RF	7	RF	VDD_RADIO[a]	Bluetooth transmitter / receiver.

[a] The VDD_RADIO domain is generated from VDD_REG_IN, see Figure 6.1.

Synthesiser and Oscillator	Lead	Pad Type	Supply Domain	Description
XTAL_32K_OUT	2	Analogue	VDD_BAT	Drive for sleep clock crystal.
XTAL_32K_IN	3	Analogue	VDD_BAT	32.768kHz sleep clock input.
XTAL_16M_OUT	9	Analogue	VDD_ANA[b]	Drive for crystal.
XTAL_16M_IN	10	Analogue	VDD_ANA[b]	Reference clock input.

[b] The VDD_ANA domain is generated from VDD_REG_IN, see Figure 6.1.

I^{2}C Interface	Lead	Pad Type	Supply Domain	Description
I2C_SDA	29	Bidirectional, tristate, with weak internal pull-up	VDD_PADS	I^{2}C data input / output or SPI serial flash data output (SF_DOUT). If connecting to SPI serial flash, connect this pin to SO on the serial flash. See Section 5.3.
I2C_SCL	28	Input with weak internal pull-up	VDD_PADS	I^{2}C clock or SPI serial flash clock output (SF_CLK), see Section 5.3.

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[11]	25	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line.
PIO[10]	24			
PIO[9]	23			
PIO[8] / DEBUG_MISO	22	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or debug SPI MISO selected by SPI_PIO#.
PIO[7] / DEBUG_MOSI	20			Programmable I/O line or debug SPI MOSI selected by SPI_PIO#.
PIO[6] / DEBUG_CS#	19			Programmable I/O line or debug SPI chip select (CS#) selected by SPI_PIO#.
PIO[5] / DEBUG_CLK	18			Programmable I/O line or debug SPI CLK selected by SPI_PIO#.

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[4] / SF_CS#	17	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or SPI serial flash chip select (SF_CS#), see Section 5.3.
PIO[3] / SF_DIN	16	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or SPI serial flash data (SF_DIN) input. If connecting to SPI serial flash, this pin connects to SI on the serial flash. See Section 5.3.
PIO[2]	27	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or I²C power.
PIO[1] / UART_RX	15	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or UART RX.
PIO[0] / UART_TX	14	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable I/O line or UART TX.
AIO[2]	11	Bidirectional analogue	VDD_AUX[c]	Analogue programmable I/O line.
AIO[1]	12	Bidirectional analogue	VDD_AUX[c]	Analogue programmable I/O line.
AIO[0]	13	Bidirectional analogue	VDD_AUX[c]	Analogue programmable I/O line.

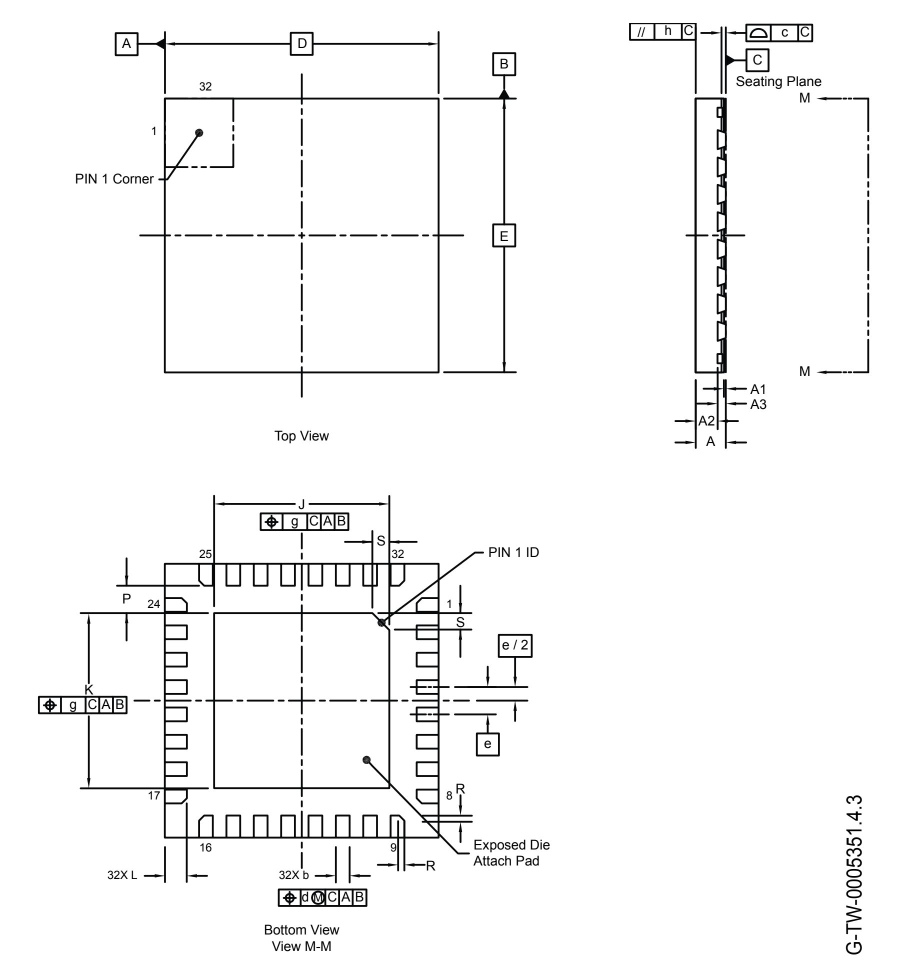
[c] The VDD_AUX domain is generated from VDD_REG_IN, see Figure 6.1.

Test and Debug	Lead	Pad Type	Supply Domain	Description
SPI_PIO#	26	Input with strong internal pull-down	VDD_PADS	Selects SPI debug on PIO[8:5].

Wake-up	Lead	Pad Type	Supply Domain	Description
WAKE	4	Input has no internal pull-up or pull-down, use external pull-down.	VDD_BAT	Input to wake CSR1000 QFN from hibernate or dormant.

Power Supplies and Control	Lead	Description
VDD_BAT	1	Battery input and regulator enable (active high).
VDD_BAT_SMPS	32	Input to high-voltage switch-mode regulator.
SMPS_LX	31	High-voltage switch-mode regulator output.
VDD_CORE	5, 30	Positive supply for digital domain.
VDD_PADS	21	Positive supply for all digital I/O ports PIO[11:0].
VDD_REG_IN	6	Positive supply for Bluetooth radio and digital linear regulator.
VDD_XTAL	8	Leave unconnected. **Note:** Add connection to a 470nF decoupling capacitor to this pin, see Section 7. The decoupling capacitor is not fitted in normal operation.
VSS	Exposed pad	Ground connections.

1.3 Package Dimensions



Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.50	0.55	0.60	e	-	0.5	-
A1	0	0.035	0.05	g	-	0.1	-
A2	-	0.4	0.425	h	-	0.1	-
A3	-	0.152	-	J	3.1	3.2	3.3
b	0.20	0.25	0.30	K	3.1	3.2	3.3
c	-	0.08	-	L	0.35	0.40	0.45
D	4.9	5.0	5.1	P	0.3	-	-
d	-	0.10	-	R	-	0.093	-
E	4.9	5.0	5.1	S	-	0.3	-
Notes	1. Coplanarity applies to leads, corner leads and die attach pad.						
Description	32-lead Quad-flat No-lead Package						
Size	5 x 5 x 0.6mm			JEDEC	MO-220		
Pitch	0.5			Units	mm		

1.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 5 x 5 x 0.6mm QFN 32-lead package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- CSR recommends that the PCB land pattern is in accordance with IPC standard IPC-7351.
- Solder paste must be used during the assembly process.

1.5 Typical Solder Reflow Profile

See *Typical Solder Reflow Profile for Lead-free Devices* for information.

2 Bluetooth Modem

2.1 RF Ports

CSR1000 QFN contains an integrated balun which provides a single-ended RF TX / RX port pin. No matching components are needed as the receive mode impedance is 50Ω and the transmitter has been optimised to deliver power in to a 50Ω load.

2.2 RF Receiver

The receiver features a near-zero IF architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input allows the receiver to be used in close proximity to GSM and W-CDMA cellular phone transmitters without being significantly desensitised.

An ADC digitises the IF received signal.

2.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the balanced port of the integrated balun.

2.2.2 RSSI Analogue to Digital Converter

The ADC samples the RSSI voltage on a packet-by-packet basis and implements a fast AGC. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference-limited environments.

2.3 RF Transmitter

2.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit packet, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

2.3.2 Power Amplifier

The internal PA has a maximum 7.5dBm output power without needing an external RF PA.

2.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v4.0 specification.

2.5 Baseband

2.5.1 Physical Layer Hardware Engine

Dedicated logic performs:

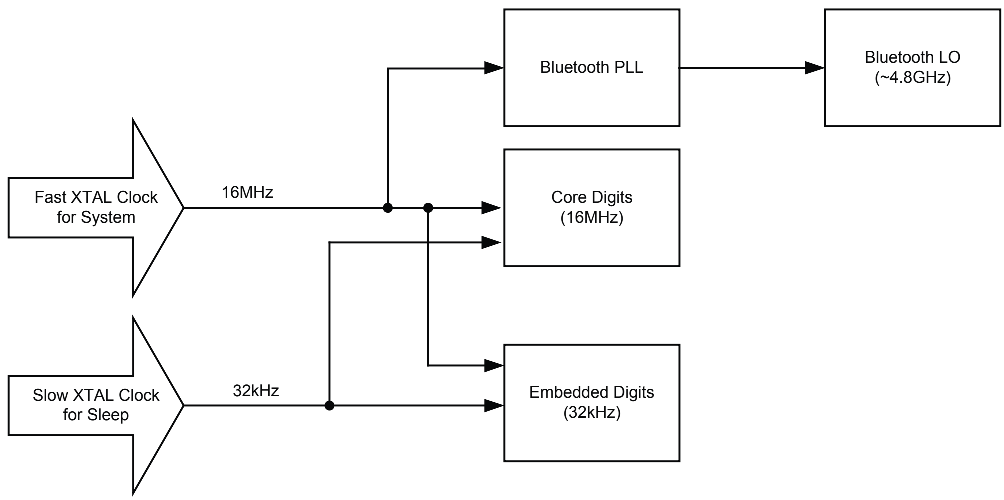
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation

The hardware supports all optional and mandatory features of Bluetooth v4.0 specification.

3 Clock Generation

The Bluetooth reference clock for the system is generated from an external 16MHz clock source, see Figure 3.1. All the CSR1000 QFN internal digital clocks are generated using a phase locked loop, which is locked to the frequency of either the external reference clock source or a sleep clock frequency of 32.768kHz, see Figure 3.1.

3.1 Clock Architecture

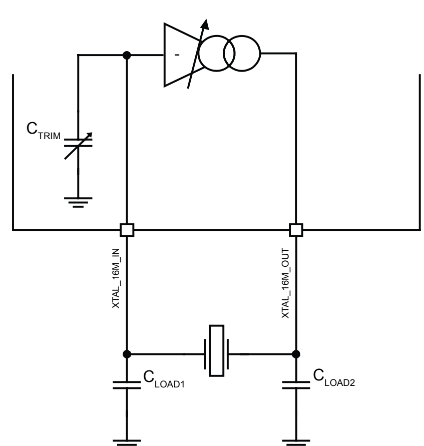


G-TW-0005266.2.2

Figure 3.1: Clock Architecture

3.2 Crystal Oscillator: XTAL_16M_IN and XTAL_16M_OUT

CSR1000 QFN contains crystal driver circuits. This operates with an external crystal and capacitors to form a Pierce oscillator. Figure 3.2 shows the external crystal is connected to pins XTAL_16M_IN and XTAL_16M_OUT.



G-TW-0005348.1.1

Figure 3.2: Crystal Driver Circuit

Note:

C_{TRIM} is the internal trimmable capacitance in Table 3.1.

C_{LOAD1} and C_{LOAD2} in combination with C_{TRIM} and any parasitic capacitance provide the load capacitance required by the crystal.

3.2.1 Crystal Specification

Table 3.1 shows the specification for an external crystal.

Parameter	Min	Typ	Max	Unit
Frequency	-	16	-	MHz
Frequency tolerance (without trimming) [a]	-	-	±25	ppm
Frequency trim range[b]	-	±50	-	ppm
Drive level	-	-	100	µW
Equivalent series resistance	-	-	60	Ω
Load capacitance	-	9	-	pF
Pullability	10	-	-	ppm/pF

Table 3.1: Crystal Specification

[a] Use integrated load capacitors to trim initial frequency tolerance in production or to trim frequency over temperature, increasing the allowable frequency tolerance.

[b] Frequency trim range is dependent on crystal load capacitor values and crystal pullability.

3.2.2 Frequency Trim

CSR1000 QFN contains variable integrated capacitors to allow for fine-tuning of the crystal resonant frequency. This firmware-programmable feature allows accurate trimming of crystals on a per-device basis on the production line. The resulting trim value is stored in non-volatile memory.

3.3 Sleep Clock

The sleep clock is an externally provided 32.768kHz clock that is used during deep sleep and in other low-power modes. Figure 3.3 shows the sleep clock crystal driver circuit.

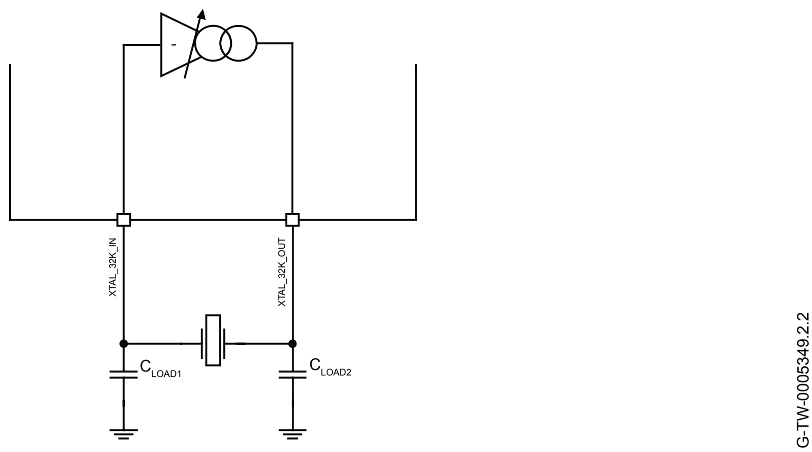


Figure 3.3: Sleep Clock Crystal Driver Circuit

Note:

C_{LOAD1} and C_{LOAD2} in combination with any parasitic capacitance provide the load capacitance required by the crystal.

3.3.1 Crystal Specification

Table 3.2 shows the requirements for the sleep clock.

Sleep Clock	Min	Typ	Max	Units
Frequency	30	32.768	35	kHz
Frequency tolerance[(a)] [(b)]	-	-	250	±ppm
Frequency trim range	-	50	-	±ppm
Drive level	-	0.4	-	V
Load capacitance	-	-	1	pF
Equivalent series resistance	40	-	65	kΩ
Duty cycle	30:70	50:50	70:30	%

Table 3.2: Sleep Clock Specification

(a) The frequency of the slow clock is periodically calibrated against the system clock. As a result the rate of change of the frequency is more important than the maximum deviation. To meet the accuracy requirements the frequency should not drift due to temperature or other effects by more than 80ppm in any 5 minute period.

(b) CSR1000 QFN can correct for ±1% by using the fast clock to calibrate the slow clock.

4 Microcontroller, Memory and Baseband Logic

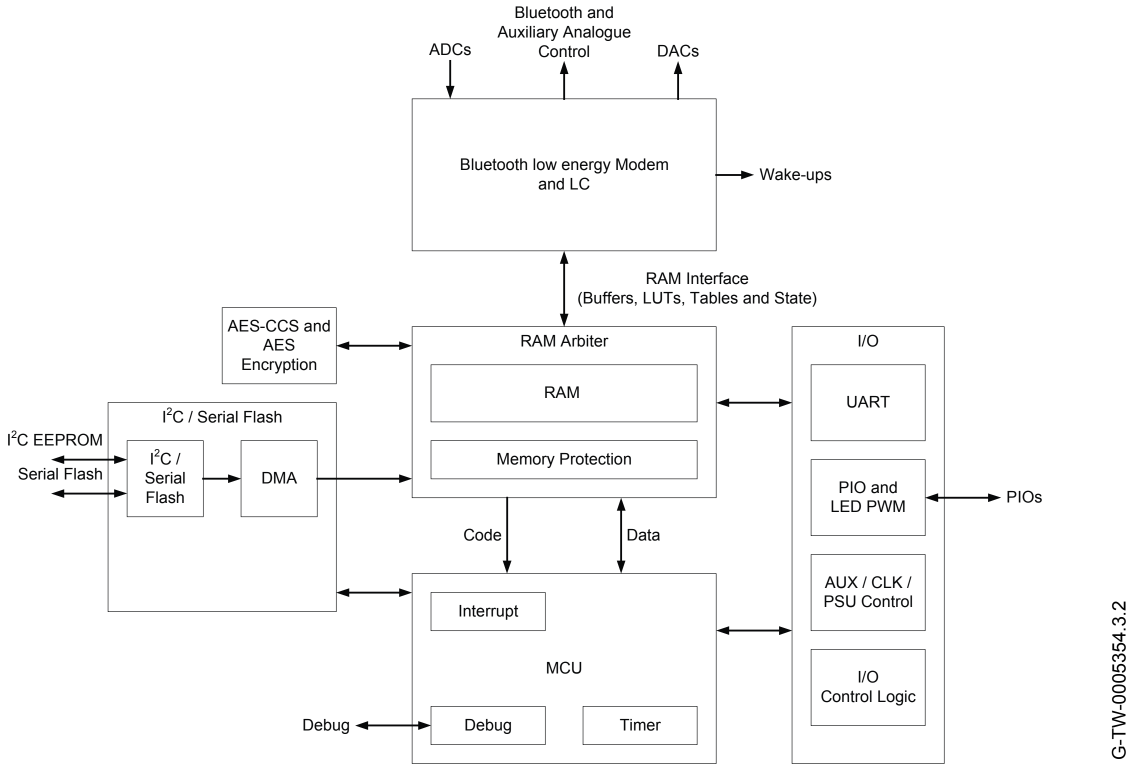


Figure 4.1: Baseband Digits Block Diagram

4.1 System RAM

64KB of integrated RAM supports the RISC MCU and is shared between the ring buffers used to hold data for each active connection and the general-purpose memory required by the Bluetooth stack.

4.2 Internal ROM

CSR1000 QFN has 64KB of internal ROM. This memory is provided for system firmware implementation. If the internal ROM holds valid program code, on boot-up, this is copied into the program RAM.

4.3 Microcontroller

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and external interfaces. A 16-bit RISC microcontroller is used for low power consumption and efficient use of memory.

4.4 Programmable I/O Ports, PIO and AIO

12 lines of programmable bidirectional I/O are provided. They are all powered from VDD_PADS.

PIO lines are software-configurable as weak pull-up, weak pull-down, strong pull-up or strong pull-down.

Note:

At reset all PIO lines are inputs with weak pull-downs.

Any of the PIO lines can be configured as interrupt request lines or to wake the IC from deep sleep mode. Table 4.1 lists the options for waking the IC from the sleep modes.

Sleep Mode	Wake-up Options
Dormant	Can only be woken by the WAKE pin.
Hibernate	Can be woken by the WAKE pin or by the watchdog timer.
Deep Sleep	Can be woken by any PIO configured to wake the IC.

Table 4.1: Wake Options for Sleep Modes

The CSR1000 QFN supports alternative functions on the PIO lines:

- SPI interface, see Section 1.2 and Section 5.4
- UART, see Section 1.2 and Section 5.1.1
- LED flasher / PWM module, see Section 4.5

Note:

CSR cannot guarantee that the PIO assignments remain as described. Implementation of the PIO lines is firmware build-specific, for more information see the relevant software release note.

CSR1000 QFN has 3 general-purpose analogue interface pins, AIO[2:0].

4.5 LED Flasher / PWM Module

CSR1000 QFN contains a LED flasher / PWM module that works in sleep modes.

These functions are controlled by the on-chip firmware.

4.6 Temperature Sensor

CSR1000 QFN contains a temperature sensor that measures the temperature of the die to an accuracy of 1 °C.

4.7 Battery Monitor

CSR1000 QFN contains an internal battery monitor that reports the battery voltage to the software.

5 Serial Interfaces

5.1 Application Interface

5.1.1 UART Interface

The CSR1000 QFN UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

2 signals implement the UART function, UART_TX and UART_RX. When CSR1000 QFN is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices.

UART configuration parameters, e.g. baud rate and data format, are set using CSR1000 QFN firmware.

When selected in firmware PIO[0] is assigned to a UART_TX output and PIO[1] is assigned to a UART_RX input, see Section 1.2.

The UART CTS and RTS signals can be assigned to any PIO pin by the on-chip firmware.

Note:

> To communicate with the UART at its maximum data rate using a standard PC, the PC requires an accelerated serial port adapter card.

Table 5.1 shows the possible UART settings for the CSR1000 QFN.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	2Mbaud (≤1%Error)
Flow control		CTS / RTS
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 5.1: Possible UART Settings

5.1.1.1 UART Configuration While in Deep Sleep

The maximum baud rate is 9600 baud during deep sleep.

5.2 Master I²C Interface

The master I²C interface communicates to EEPROM, external peripherals or sensors. An external EEPROM connection can hold the program code externally to the CSR1000 QFN. The maximum clock speed is 400kHz.

Figure 5.1 shows an example of an EEPROM connected to the I²C interface where I2C_SCL, I2C_SDA and PIO[2] are connected to the external EEPROM. The PIO[2] pin supplies the power to the EEPROM supply pin, e.g. VDD. At boot-up, if there is no valid ROM image in the CSR1000 QFN ROM area the CSR1000 QFN tries to boot from the I²C interface, see Figure 5.3. This involves reading the code from the external EEPROM and loading it into the internal CSR1000 QFN RAM.

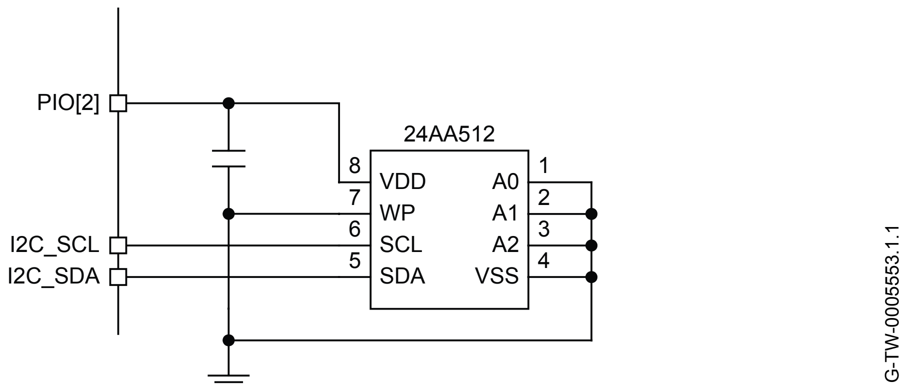


Figure 5.1: Example of an I²C Interface EEPROM Connection

5.3 SPI Master Interface

The SPI master memory interface in the CSR1000 QFN is overlaid on the I²C interface and uses a further 3 PIOs for the extra pins, see Table 5.2.

SPI Flash Interface	Pin
Flash_VDD	PIO[2]
SF_DIN	PIO[3]
SF_CS#	PIO[4]
SF_CLK	I2C_SCL
SF_DOUT	I2C_SDA

Table 5.2: SPI Master Serial Flash Memory Interface

Note:

If an application using CSR1000 QFN is designed to boot from SPI serial flash, it is possible for the firmware to map the I²C interface to alternative PIOs.

Figure 5.2 shows simple SPI timing diagram.

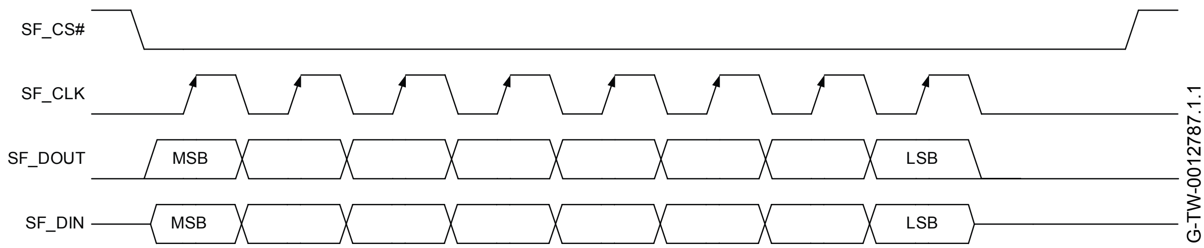


Figure 5.2: SPI Timing Diagram

The boot-up sequence for CSR1000 QFN is controlled by hardware and firmware. Figure 5.3 shows the sequence of loading RAM with content from RAM, EEPROM and SPI serial flash.

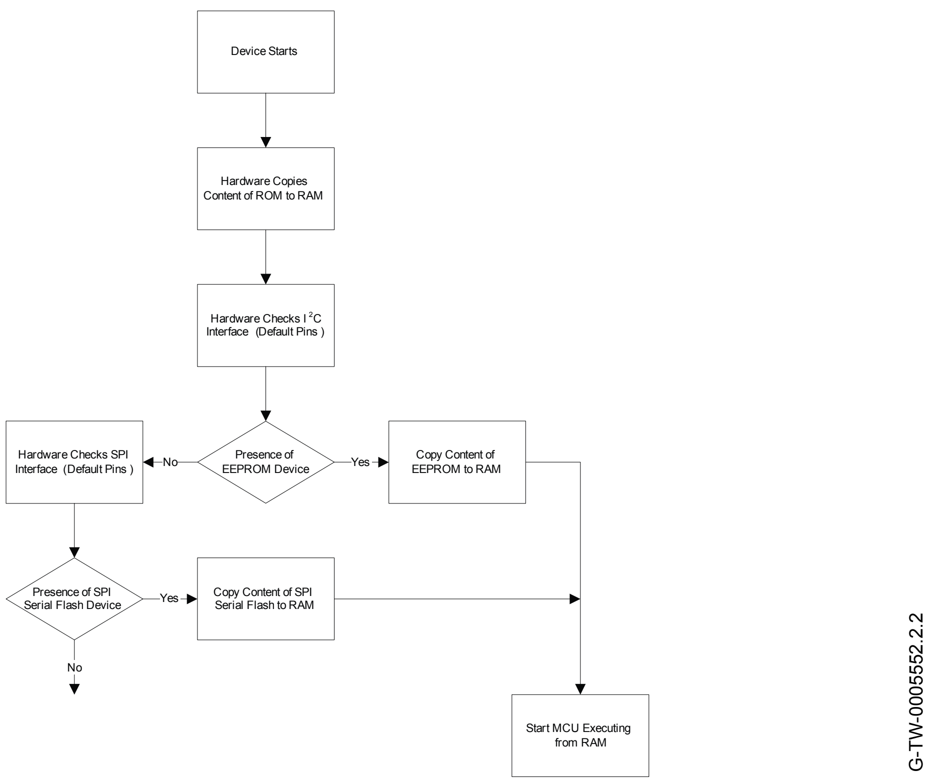


Figure 5.3: Memory Boot-up Sequence