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16-bit High Performance ADC Drivers

DESCRIPTION

Demonstration circuit 1058 is a reference design featuring Linear Technology Corporation's 16-bit High Performance ADC Drivers. DC1058 demonstrates good circuit layout techniques and recommended component selection for optimal system performance. The ADC driver input and output networks are flexible, allowing for AC or DC coupling, single-ended or differential configurations, and additional filtering before the ADC.

DC1058 comes installed with one of Linear Technology's 16-bit ADC drivers—LT1994, LTC6404, LTC6406, or

LTC6403. For ease of evaluation, a 16-bit Analog-to-Digital Converter (ADC) is included on the board. DC1058 includes an on-board 40-pin edge connector for use with the DC718 Data Acquisition demo board and Linear Technology's PScope data processing software, available on our website at <http://www.linear.com>.

Design files for this circuit board are available. Call the LTC factory.

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QUICK START PROCEDURE

Validating the performance of the ADC Driver-ADC combination is simple with DC1058, and requires only two signal generators and some basic test equipment. Table 1 shows the function of each I/O connector and selectable jumper on the board. Refer to Figure 1 for proper board evaluation equipment setup and follow the procedure below:

1. Connect the power supplies as shown (see Table 2 for voltages). The power supply connector labeled V+ powers the ADC driver. VDD powers the ADC, and OVP provides power to both the ADC output stage and the two CMOS output buffers. The entire board and all components share a common ground. Check the datasheets of the respective IC's before applying power, to avoid damage from over-voltage conditions.
2. Provide an encode clock to the ADC via SMA connector J3. For best performance, a high-quality sine wave synthesizer with an external band-pass filter will provide a stable, low-phase-noise clock source. A crystal oscillator will also provide good performance. DC1058A-A includes an on-board clock buffer IC to provide a fast-edge clock to the ADC.

NOTE. A poor quality encode clock can significantly degrade the signal-to-noise ratio (SNR) of the driver-ADC combination.

Table 1: DC1058 Connector and Descriptions

REFERENCE	FUNCTION
J1 (40 pin conn)	Provides direct connection to DC718. CMOS Output Buffers provide parallel data output and clock signals (see schematic).
J3 (Encode Input)	ADC Encode Clock. For best performance, use a high-quality low-phase-noise clock source.
J2 (AIN-)	Analog Input (by default, tied to ground via resistor R3 – apply input signal at J4)
J4 (AIN+)	Analog Input (50Ω source impedance)
JP1	Invert Clock. Default is NORM position.
JP2 (SHDN)	Enables or Disables U2/U3, the ADC driver
JP3 (PGA)	ADC Input Range Select. LO selects 2.25V _{pp} Input Range, HI selects 1.5V _{pp} range.
JP4 (RAND)	Output Randomizer. NORM is default, RAND randomizes the DC1058 digital output.
JP5 (DITH)	ADC Additive Dither. See ADC datasheet.

3. Apply an input signal to the board. DC1058 allows great flexibility in applying input signals (see the section on Applying Input Signals). For best results, use a low distortion, low noise signal generator with sufficient filtering to avoid degrading the performance of the amplifier and ADC.
4. Observe the ADC output with demo circuit DC718, a USB cable, a Windows computer, and Linear Technology's QuickEval-II (Pscope) data processing software.

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NOTE. Even a high-quality signal synthesizer will still have noise and harmonics that should be attenuated with a low-pass or band-pass filter. For good-quality high order filters, see TTE, Lark Engineering, or equivalent.

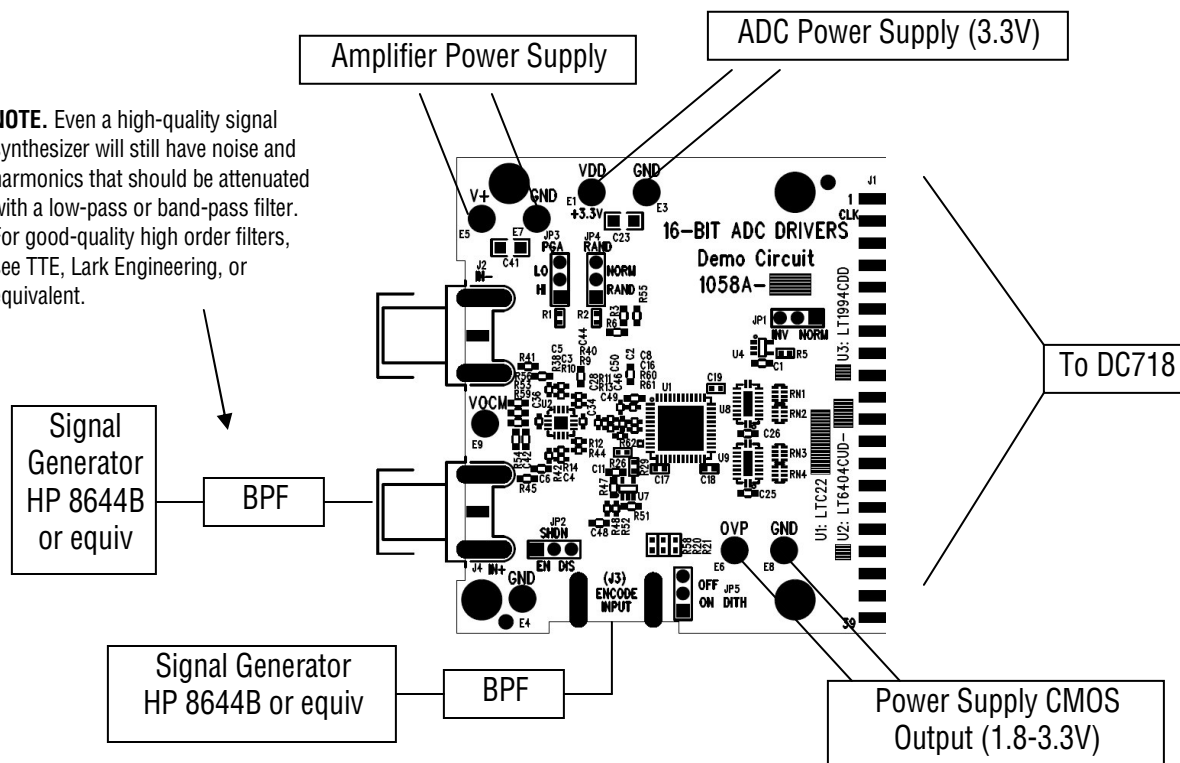


Figure 1. Proper Evaluation Equipment Setup

Version	V+	VDD	OVP
-A	2.375-12.6V	3.135-3.465V	1.85-3.6V (limited by DC718)
-B	2.7-5.25V		
-C	2.7-5.25V		
-D	2.7-5.25V		
-E	2.7-3.5V		
-F	2.7-5.25V		

Table 2: Supply Voltages for various demo board versions

ADDITIONAL INFORMATION

DC1058 comes pre-installed with LT1994, LTC6404, LTC6406, or LTC6403. **Note that the LT1994 has a different pinout, and thus is located on the bottom side of the PCB (U3).** Although the DC1058 demo board is ready to use on delivery, it has additional flexibility built in for various types of input networks, filtering configurations, and single-ended or differential inputs. Below is some information about configuring DC1058 to meet the specific needs of your evaluation.

APPLYING INPUT SIGNALS

The input network consists of various components designed to allow either single-ended or differential inputs, AC-coupled or DC-coupled. Table 3 shows some possible input configurations, and which components to install. Linear Technology's 16-bit ADC driver families are generally characterized and designed for excellent performance with both single-ended and differential input drive. When using DC coupled inputs, the inputs to DC1058 may need to be level-shifted to avoid violating the input common-mode voltages of the amplifier. Check the amplifier datasheet for details.

Table 3: DC1058 Input Configuration Guide

CONFIGURATION	COMPONENTS NECESSARY
Single-Ended Input AC-Coupled (Default Setup)	Install 0Ω jumper at R41. Install 50Ω impedance matching resistor at R45 if necessary. Install C5, C6 for AC coupling.
Single-Ended Input DC Coupled*	Install 0Ω jumper at R41. Install 50Ω impedance matching resistor at R45 if necessary. Remove C5 and C6, replace with 0Ω jumpers.
Differential Input AC-Coupled	Replace R41 and R45 with impedance matching resistors if necessary. Install C5 and C6 for AC coupling.
Differential Input DC-Coupled*	Replace R41 and R45 with impedance matching resistors if necessary. Remove C5 and C6, replace with 0Ω jumpers.

NOTE. * When driving the ADC driver with a direct DC-coupled path, be aware of the increased input currents that may occur due to the output common-mode voltage and the amplifier gain/feedback resistors.

The common-mode voltage at the ADC drivers must remain within the datasheet-stated limits. When replacing C5 and C6 with 0Ω jumpers, make sure to level-shift the inputs if necessary so that the ADC driver's input common-mode voltage requirements are met.

POWER SUPPLY BYPASS CAPACITANCE

Depending on the quality of the power supplies provided to DC1058, it may be desirable to add larger bulk capacitors at C27, C35, and C39. This is not necessary with clean, low-impedance DC power supplies.

FILTER NETWORKS

Components for an RC or LC filter are included at the ADC input for low-pass or bandpass filter designs. To achieve the low distortion necessary for driving high-performance 16-bit ADCs, the ADC drivers have very wide signal bandwidths. Reducing the bandwidth at the ADC input will reduce the amount of wideband noise sampled by the ADC, and therefore improve the overall signal-to-noise ratio (SNR).

CHANGING THE ADC DRIVER'S OUTPUT COMMON-MODE VOLTAGE

The LT1994 and LTC6403/4/6 have internal resistive dividers that can set the output common-mode voltage automatically, but if the user wishes to change that voltage, it can be done in one of three ways. By changing the resistors R59 and R54 that comprise a resistive divider from the V+ voltage, it is possible to tune the common-mode voltage independently of all other factors. Alternatively, R59 and R54 can be removed, and the ADC can supply the common-mode voltage by installing R53 (this is the default). A third option is to drive E9 (VOCM) on the board using an external voltage source. If driving this voltage from an active buffer such as an op amp, removal of C42 may be necessary to avoid loading.

ENCODE CLOCK PATHS

As shown in the schematic, there are two clock paths that can be used on DC1058. The differential clock path with transformer T2 comes installed with the LTC2207 105Msps ADC. The single-ended clock path with clock buffer U8 comes installed with the lower speed LTC2203.

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INVERT OUTPUT CLOCK

Jumper JP1 inverts the clock output from DC1058 to DC718 (data acquisition board). This ensures that DC718 latches the output data on the correct edge of the clock. If the output data/FFT appears unusual, try changing the position of JP1 to latch data on the opposite clock edge. The correct position of Jumper JP1 may change if you vary the clock frequency.

QUICKDAACS CIRCUITRY

Logic gate U5, installed on the back of DC1058, enables the CMOS output buffers when DC1058 is plugged into DC718, which pulls its input high. Device U6 is an EEPROM device that is used by the QuickEval software, and does not affect board operation or performance.

USING PSCOPE (QUICKEVAL II) SOFTWARE

PScope, downloadable from Linear Technology's website <http://www.linear.com/>, processes data from the DC718

QuickDAACS board and displays FFT and signal analysis information on the computer screen. This section describes how to use the software to view the output from DC1058.

The on-board EEPROM should enable automatic board detection and auto-configuration of the software, but in case the user wishes to change the settings, they can easily do so.

From the Configure menu in the toolbar, uncheck "Autodetect Device". The next step is to use the proper settings for the DC1058 output in the Device menu, also under Configure. See Figure 3. Select "User Configure" from the menu bar, and select the "Randomized" checkbox if the output randomizer is turned on (via JP4). The other settings will generally be the same as shown in the figure. After configuration is through, the program should be ready to collect and display data. See the Help file for instructions on general software use.

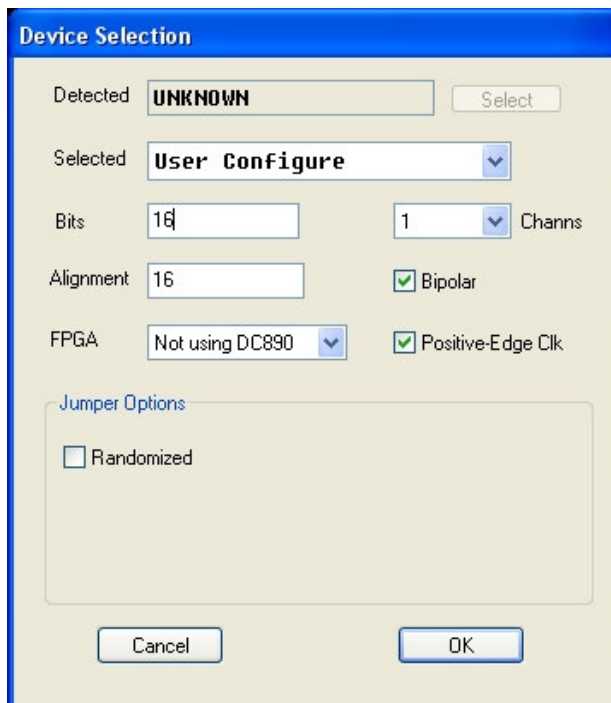


Figure 2. Entering the correct device information for your ADC. Select the correct device for your board.

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