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DESCRIPTION

Demonstration circuit 1151 supports a family of 16-bit 105, 80, and 65MSPS analog to digital converters. Each assembly features the following devices: LTC2274, LTC2273, or LTC2272 high speed, serial output ADCs.

The versions of the DC1151 demo board are listed in Table 1. Depending on the sample rate, input frequency and CML data rate, the DC1151 is supplied with the appropriate ADC and with an optimized input circuit, and de-serializing circuit. The circuitry on the analog inputs is optimized for analog input frequencies from 1MHz to 70MHz or from 70MHz to 140MHz. For higher input frequencies, contact the factory for support.

Design files for this circuit board are available. Call the LTC factory.

Table 1: DC1151 Variants

DC1151 VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	MINIMUM SAMPLE RATE (LIMITED BY DESERIALIZER)	INPUT FREQUENCY
1151A-C	LTC2274	16-Bit	105Msps	75Msps	1MHz - 70MHz
1151A-D	LTC2274	16-Bit	105Msps	75Msps	70MHz - 140MHz
1151A-E	LTC2273	16-Bit	80Msps	75Msps	1MHz - 70MHz
1151A-F	LTC2273	16-Bit	80Msps	75Msps	70MHz - 140MHz
1151A-G	LTC2272	16-Bit	65Msps	3Msps	1MHz - 70MHz
1151A-H	LTC2272	16-Bit	65Msps	3Msps	70MHz - 140MHz

1. Performance Summary (T_A = 25°C)

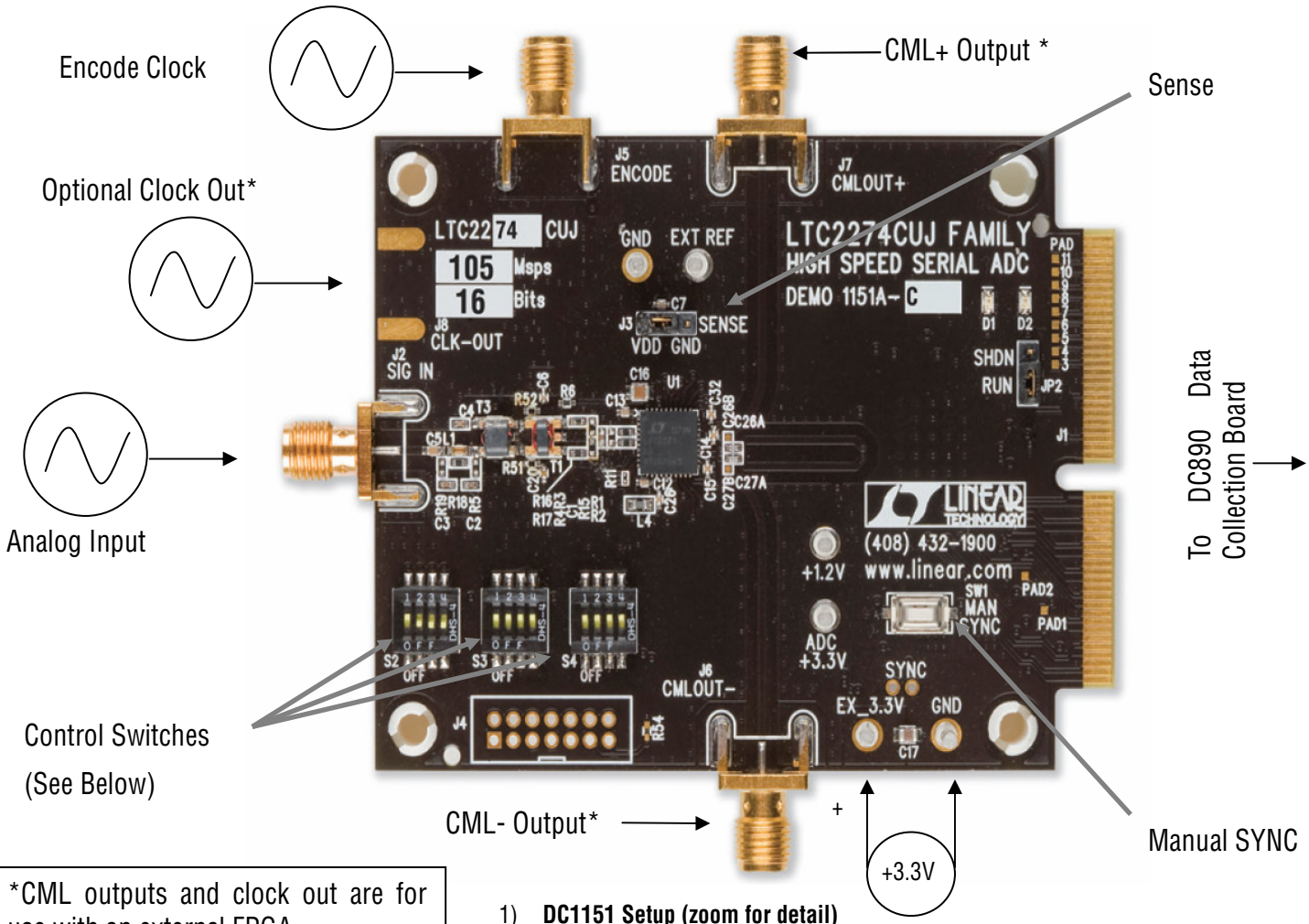
PARAMETER	CONDITION	VALUE
Supply Voltage	Supply must provide up to 500mA.	Optimized for 3.3V [3.135 ⇔3.465V min/max]
Analog Input Range	Depending on Sense Pin Voltage(and converter inputs)	$1.5V_{PP}$ to $2.25V_{PP}$
Logic Input Voltages	Minimum Logic High	2V
	Maximum Logic Low	0.8V
Logic Output Voltage	Minimum Logic High	OVdd-0.2V
	Maximum Logic Low	OVdd-0.4V
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Convert Clock Level	50 Ω Source Impedance, AC coupled or ground referenced (Convert Clock input is capacitor coupled on board and terminated with 50Ω.)	$2V_{P-P}$ ⇔$2.5V_{P-P}$ Sine Wave or Square wave
Resolution	See Table 1	
Input Frequency Range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 1151 is easy to set up to evaluate the performance of any member of the LTC2274 family of A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

SETUP

If a DC890 FastDAACS Data Analysis and Collection System was supplied with the DC1151 demonstration circuit, follow the DC890 Quick Start Guide to install the required software and for connecting the DC890 to the DC1151 and to a PC running Windows 98, 2000 or XP.



*CML outputs and clock out are for use with an external FPGA

1) **DC1151 Setup (zoom for detail)**

JUMPERS, SWITCHES, & INDICATORS CONT.

J3: Sense – Tie sense to Vdd to select the internal 2.5V bandgap reference. An external reference of 2.5V or 1.25V may be used; both reference values will set a full scale ADC range of 2.25V (PGA=0). (Default = Vdd)

SW1: Manual Sync – Asserting the manual sync push button will force the LTC227X to output a series of COMMA characters used for re-synchronization.

D1: SYNC Error – This LED will be lit if the onboard decoder is not synchronized to the LTC227X. It is only valid when using the DC890.

D2: Data Good – This LED will be lit when there is data being presented to the onboard decoder. It is only valid when using the DC890.

Switches

S2: Pin 1: Dith – Enables dither. Refer to the datasheet for more information on internal dither. (Default Up, Dither off)

Pin 2: ISMODE – When ISMODE is asserted a special Idle SYNC mode is enabled where synchronization is preformed by sending a K28.5 character followed by the appropriate data code group to set up a negative running disparity. The code group used will be either D5.6 or D16.2. This is the mode used with the on board decoder. Disabling ISMODE will enable synchronization with a series of COMMAs, K28.5. This mode should be used when using FPGAs. (Default Down, ISMODE on)

Pin 3 & 4: Sample Rate Range Select: Sets the internal PLL to the correct clock frequency. See Table 2 for correct frequency. (Default UP, UP, Clock rate = 65 -105 Msps)

S3: Pin 1: ADC shut down – Powers down analog circuitry (Default UP, Analog on)

Table 2 Sample Rate Range Select

Pin 3	Pin 4	Clock Range
X	Up	20 - 40Msps
Up	Down	35 - 70Msps
Down	Down	65 -105 Msps

Pin 2: Serial Shutdown – Powers down serial output. (Default UP, Digital on)

Pin 3: FAM: Enables Frame alignment monitoring. This mode is not supported by the on board decoder. See the LTC2274 for more information. (Default UP, FAM off)

Pin 4: SCRAM: Enables Polynomial Scrambling. This mode is not supported by the on board decoder. See the LTC2274 datasheet for more information. (Default UP, SCRAM off)

S4: Pin 1 & 2: Test Pattern Select – Provides various test patterns on the serial outputs. See table 3 for more information. (Default UP, UP, ADC data)

Table 3: Test Pattern Select

Pin 1	Pin 2	Test Pattern
Down	Down	$1+x^{14}+x^{15}$ pseudo random test pattern
Up	Down	$1+x^{9}+x^{11}$ pseudo random test pattern
Down	Up	1010101010.... Code group D21.5
Up	Up	ADC Data

Pin 3: PGA – Selects appropriate input range. Up selects the 2.25V input range. Down Selects the 1V input range. (Default UP, 2.25V range)

Pin 4: MSBINV: Inverts MSB, Down selecting 2's compliment output (Default UP, offset binary)

POWER

If a DC890 is used to acquire data from the DC1151, the DC890 must be provided with an external 6V±0.5V 1A supply on turrets G7(+) and G1(-) or the adjacent 2.1mm power jack to support the power requirements of the Xilinx Spartan 3 FPGA. The DC890B will not enable collection mode without externally applied power present. Apply +3.3V across the pins marked "EX_3.3V" and "GND" on the DC1151. The DC1151 demonstration circuit requires up to 500mA depending on the sampling rate and the A/D converter supplied.

ENCODE CLOCK

NOTE: This is not a logic compatible input. Apply an encode clock to the SMA connector on the DC1151 demonstration circuit board marked "J5 ENCODE". The transformer is terminated on the secondary side with 100 ohms, and further terminated at the ADC (at C12).

For the best noise performance, the ENCODE CLOCK must be driven with a very low jitter source. When using a sinusoidal generator, the amplitude should be large, up to $2V_{P-P}$ or 19dBm. Using band pass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broad band noise. Low phase noise Agilent 8644B generators are used with TTE band pass filters for both the Clock input and the Analog input.

ANALOG INPUT NETWORK

Apply the analog input signal of interest to the SMA connectors on the DC1151 demonstration circuit board marked "J2 SIG IN". These inputs are capacitive coupled to Balun transformers ETC1-1-13, or directly coupled through Flux coupled transformers ETC1-1T. (See Schematic)

For optimal distortion and noise performance the RC network on the analog inputs should be optimized for different analog input frequencies. Refer to the provided schematics. These two input networks cover a broad bandwidth and are not optimized for operation at a specific input frequency. For input frequencies less than 5MHz, or greater than 150MHz, other input networks may be more appropriate.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR. In some cases, 3-10dB pads may be required to obtain low distortion.

If your generator cannot deliver full scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and High IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively low Q filter used between the amplifier and the demo circuit.

DIGITAL OUTPUTS

The LTC2274 family has a high speed serial output. The output data is serialized according to the JEDEC specification for serial converters (JESD204).

The LTC2274 family uses CML drivers to transmit high-speed data. The output driver bias current is typically 16mA, generating a signal swing potential of 400mVpp (800mVdiff) across the combined internal and external termination resistance of 20ohms on each output.

The standard DC1151 demo board is configured to be used with the DC890. Capacitors C26 and C27 are in the "A" position. This drives the output of the LTC2274 into an 8B/10B decoder that also deserializes the data for use with the parallel connector of the DC890. If an FPGA is used to receive the CML output signals directly, capacitors C26 and C27 should be moved to position "B" and the jumper on JP2 should be moved to SHDN. This drives the CML out-

puts to the CML- and CML+ SMA connectors (J6 and J7), and disables the on-board decoder. When using the DC1151 with an external FPGA, care should be taken to use matched cables to connect to the FPGA demo board. If the FPGA requires a reference clock the DC1151 can be modified to provide it. This requires an SMA connector to be added at J8 CLK-OUT, as well a 0 ohm resistor at R55.

SOFTWARE

The DC890B board is configurable by *PScope System Software* provided or down loaded from the Linear Technology website at http://www.linear.com/software/. If a DC890 was provided, follow the DC890 Quick Start Guide and the instructions below.

To start the data collection software if "*PScope.exe*", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1151 demonstration circuit is properly connected to the DC890, PSCOPE should automatically detect the DC1151, and configure itself accordingly. **The data will appear on the channel 2 of PScope.** If necessary the procedure below explains how to manually configure PSCOPE.

Configure PScope for the appropriate variant of the DC1151 demonstration circuit by selecting the correct A/D Converter as installed on the DC1151. Under the "Configure" menu, go to "Device." Under the "Device" pull down menu, select device, LTC2274. Select the part in the Device List and PScope will automatically blank the last two LSBs when using a DC1151 supplied with a 14-Bit part. If you are operating with a version of PScope that does not include LTC2274 in the device menu, you may manually configure as:

User configure

16-Bit

Channs: 2

Alignment: Left-16

Bipolar = Unchecked

Positive clock edge = Checked

Type: CMOS

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. The data will appear on the channel 2 of PScope. Additional information and help for *PScope* is available in the DC890 Quick Start Guide and in the online help available within the *PScope* program itself.