Chipsmall

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DESCRIPTION

Demonstration circuit 1350 supports a family of 12 and 14-Bit 25Msps ADC. This assembly features one of the following devices: LTC2226H or LTC2246H high speed, high dynamic range industrial grade ADCs.

The versions of the 1350 demo board that support the LTC2246H family of 12 and 14-Bit ADCs are listed on Table 1. Depending on the required resolution, sample rate and input frequency, the DC1350 is sup-

plied with the appropriate A/D. The circuitry on the analog inputs is optimized for analog input frequencies below 70 MHz. For higher operating frequencies, refer to the datasheet.

Design files for this circuit board are available. Call the LTC factory.

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Table 1. DC1350 Variants

DC1350 VARIANTS	ADC PART NUMBER	RESOLUTION*	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1350A-A	LTC2246H	14-Bit	25Msps	$1MHz < A_{IN} < 70MHz$
1350A-B	LTC2226H	12-Bit	25Msps	$1MHz < A_{IN} < 70MHz$

Table 2. Performance Summary ($T_A = 25°C$)

PARAMETER	CONDITION	VALUE
Supply Voltage	Supply must provide up to 150mA.	Optimized for 5.0V [4.3V ⇔ 5.7V min/max]
Analog input range	Depending on Sense Pin Voltage	$1V_{PP}$ to $2V_{PP}$
Logic Input Voltages	Minimum Logic High	2.0 V
	Maximum Logic Low	0.8V
Logic Output Voltage (FXLH42245 output buffer, V_{cc} = 3.0V)	Minimum Logic High @ -12mA	2.2V
	Maximum Logic Low @ 12mA	0.81V
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Convert Clock Level	50 ••Source Impedance, AC coupled or ground referenced (Convert Clock input is capacitor coupled on board and terminated with 50•.)	$2V_{P-P}$ ⇔ $2.5V_{P-P}$ Sine Wave or Square wave
Resolution	See Table 1	
Input frequency range	$1MHz < A_{IN} < 70MHz$	
SFDR	See Data Sheet	
SNR	See Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 1350 is easy to set up to evaluate the performance of the LTC2246 family of industrial grade A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

SETUP

If a DC718 QuickDAACs+ Data Acquisition and Test System was supplied with the DC1350 demonstration circuit, follow the DC718 Quick Start Guide to install the required software and for connecting the DC718 to the DC1350 and to a PC running Windows98, 2000 or XP.
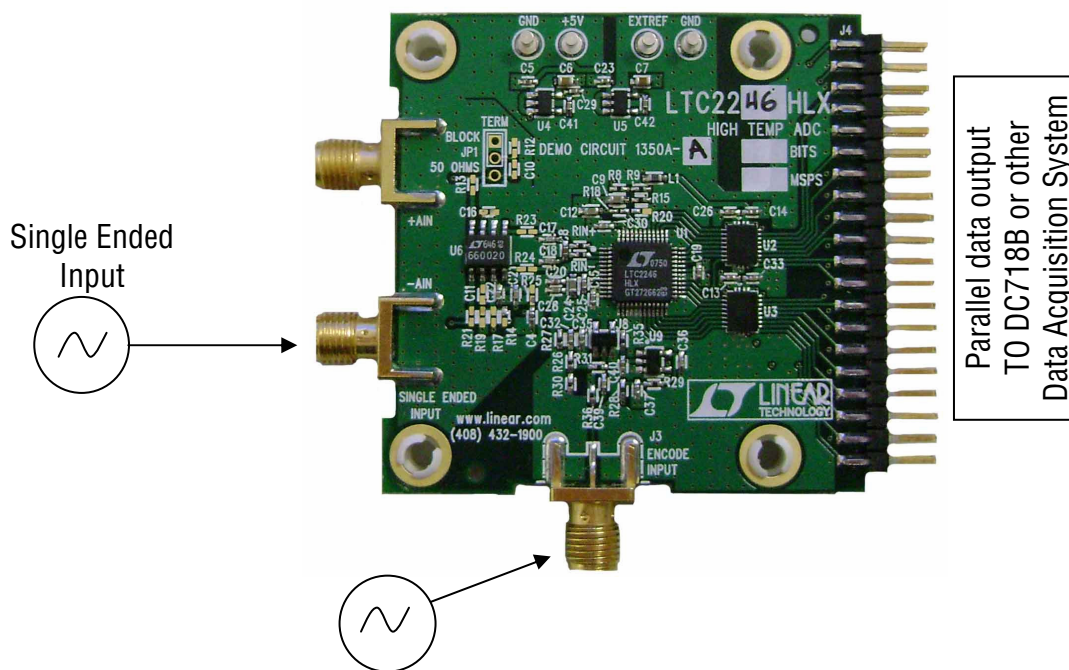

Figure 1. Proper Measurement Equipment Setup

DC1350 DEMONSTRATION CIRCUIT BOARD JUMPERS

The DC1350 demonstration circuit board should have the following jumper settings:

JP1 (optional): Signal Termination: 50Ω for proper impedance matching.

POWER

If a DC718 is used to acquire data from the DC1350, the DC718 must FIRST be connected to a powered USB port or provided an external 6-9V BEFORE applying +5V across the pins marked "+5V" and "GND" on the DC1350. The DC1350 demonstration circuit requires up to 200mA depending on the sampling rate and the A/D converter supplied.

The DC718 data collection board is powered by the USB cable and does not require an external power supply unless it is connected to the PC through an un-powered hub. In this case it must be supplied with 6-9V on turrets G7 (+) and G1 (-) or the adjacent 2.1mm power jack.

ENCODE CLOCK

NOTE: THIS IS NOT A LOGIC LEVEL INPUT. Apply an encode clock to the SMA connector on the DC1350 demonstration circuit board marked "CLOCK INPUT".

For the best noise performance, the CLOCK INPUT must be driven with a very low jitter source. When using a sinusoidal generator, the amplitude should be as large as possible, up to $3V_{P-P}$. Using band pass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broadband noise. Low phase noise Agilent 8664B generators used with TTE band pass filters for both the Clock input and the Analog input are appropriate.

Apply the analog input signal of interest to the SMA connector on the DC1350 demonstration circuit board marked "J2 SINGLE ENDED INPUT". This input is capacitively coupled to the primary of transformer T1.

ANALOG INPUT NETWORK

For optimal distortion and noise performance the RC network on the analog inputs are optimized for input frequencies between 1MHz and 70 MHz. For higher operating frequencies, contact the factory for support.

This demo board also has prevision for a differential input through an LT6600 amplifier. Implementing this path requires first removing R6 and R7. Then populate R13, R16, R17, R21, R22, R23, R24, C11, and C16 with the values provided in the provided schematic. This input path will require a differential signal provided at J1 and J2. With the values given in the schematic the LT6600 will provide a gain of one, and a maximum input frequency of 20MHz. Refer to LT6600-20 data sheet for more information.

DIGITAL OUTPUTS

An internally generated conversion clock output is available on pin 3 of J4 and the data is available on Pins 11-37 for 14-Bit or (15-37 for 12-Bit) of J2. Data can be collected via a logic analyzer, cabled to a development system through a SHORT 2 to 4 inch long 40 pin ribbon cable or collected by the DC718 QuickEval-II Data Acquisition Board.

SOFTWARE

The DC718B board is configurable by *PScope System Software* provided or down loaded from the Linear Technology website at http://www.linear.com/software/. If a DC718 was provided, follow the DC718 Quick Start Guide and the instructions below.

To start the data collection software if "*PScope.exe*", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1350 demonstration circuit is properly connected to the DC718, PSCOPE should automatically detect the DC1350, and configure itself ac-

cordingly. If necessary the procedure below explains how to manually configure PSCOPE.

Configure PScope for the appropriate variant of the DC1350 demonstration circuit by selecting the correct A/D Converter as installed on the DC1350. Under the "Configure" menu, go to "Device." Under the "Device" pull down menu, select device, LTC2246H or LTC222H. Select the part in the Device List and PScope will automatically blank the last two LSBs when using a DC1350 supplied with a 12-Bit part. If you are operating with a version of PScope that does not include LTC2246H in the device menu, you may manually configure as:

Selected: User configure

Bits: 14 (or 12-Bit if using LTC2226H)
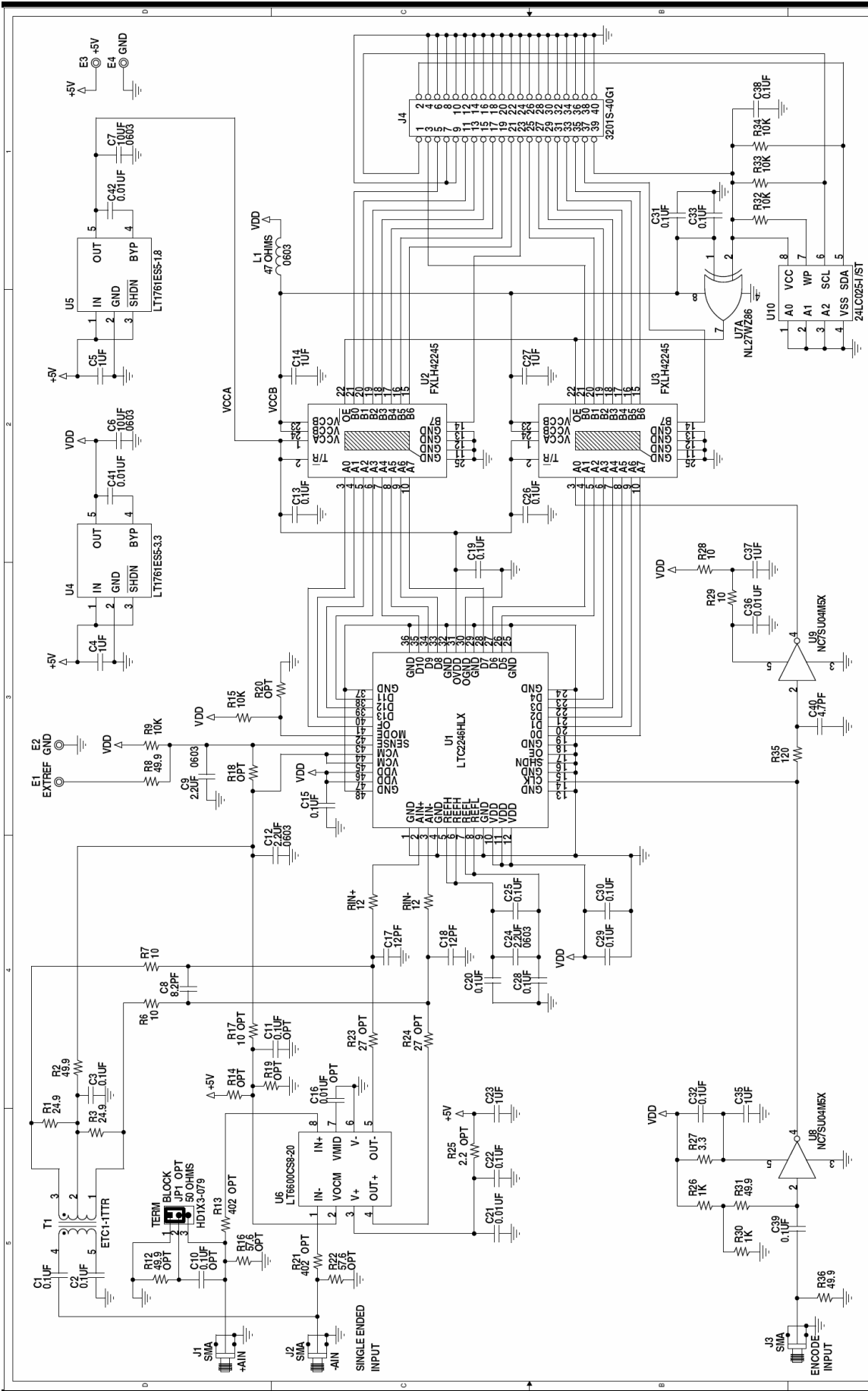
Alignment: 14

Channel: 1

Bipolar: Checked

Positive clock edge: Unchecked

Type: Not using DC890

Randomize: Unchecked

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for *PScope* is available in the DC718 Quick Start Guide and in the online help available within the *PScope* program itself.

1630 McCarthy Blvd.
Milpitas, CA 95035
Phone: (408)432-1900
Fax: (408)434-0507
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LINEAR TECHNOLOGY

TITLE: SCHEMATIC

HIGH TEMP ADC

DWG NO.
DC1350A-1 * LTC2200 FAMILY

SIZE A   REV A-1

DATE: Monday, February 04, 2008   SHEET 1 OF 1

CONTRACT NO.
APPROVALS
DRAWN: KIM T.
CHECKED:
ENGINEER:
DESIGNER: CLARENCE M.

★ FOR ASSEMBLY

ASSY	U1	BITS	MSPS
-A	LTC2246HLX	14	25
-B	LTC2226HLX	12	25

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 0402.
   ALL CAPACITORS ARE 0402.
2. INSTALL SHUNT ON JP1(1&2).

LT LINEAR TECHNOLOGY

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