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LTC2656

16-Bit, Octal Rail-to-Rail DAC with 10ppm/°C Max Reference

DESCRIPTION

Demonstration circuit 1397B features the **LTC[®]2656** Octal 16-bit DAC with ± 4 LSB INL error. This device establishes a new board-density benchmark for 16-bit DACs and advances performance standards for output drive, crosstalk and load regulation in single supply, voltage-output multiple DACs.

The DC1397B has many features for evaluating the performance of the LTC2656. An external 1.25V precision reference is provided.

Another feature of this board is the onboard LTC2428 20-bit delta-sigma ADC for monitoring the DAC output voltage. The 16ppm total error of this device is adequate for taking meaningful measurements of various LTC2656 parameters.

Design files for this circuit board are available at <http://www.linear.com/demo>

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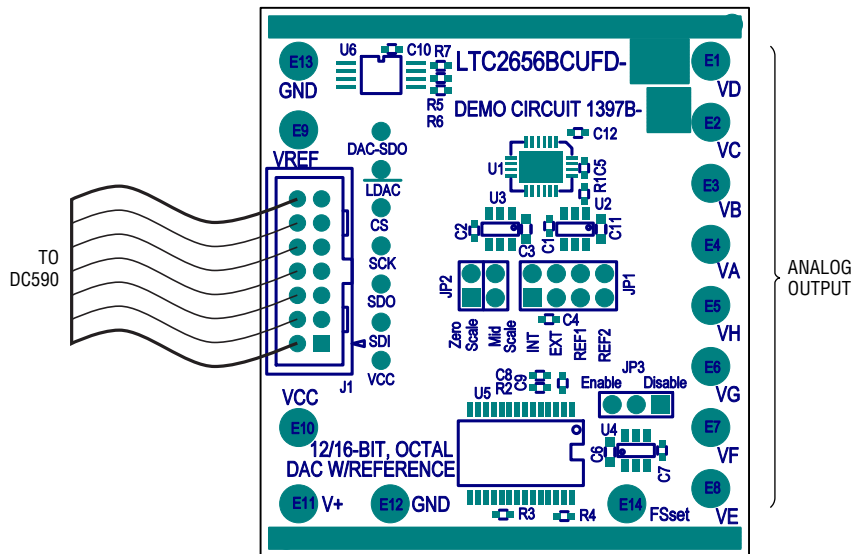


Figure 1. DC1397B Connection Diagram

PERFORMANCE SUMMARY

Specifications are at $T_A = 25^\circ\text{C}$

PARAMETER	CONDITION	VALUE
Resolution		16 Bits
Monotonicity	$V_{CC} = 5V$	16 Bits
Differential Nonlinearity	$V_{CC} = 5V$	± 1 LSB Maximum
Integral Nonlinearity	$V_{CC} = 5V$	± 4 LSB Maximum
Load Regulation	$V_{CC} = 5V$, Mid-Scale, $I_{OUT} = \pm 15\text{mA}$	2LSB/mA Maximum
DC Crosstalk	Due to Load Current Change on Any Other Channel	3.5 $\mu\text{V}/\text{mA}$

DEMO BOARD TYPE	LTC2656 VARIATION	FULL SCALE
DC1397B-A	LTC2656BCUFD-L16	2.5V
DC1397B-B	LTC2656BCUFD-H16	4.096V

QUICK START PROCEDURE

Connect DC1397B to a DC590 USB serial controller using the supplied 14-conductor ribbon cable. Connect DC590 to a host PC with a standard USB A/B cable. Run the evaluation software supplied with DC590 or download it from www.linear.com/software. The correct control panel will be loaded automatically. Click the COLLECT button

to begin outputting codes to the DACs and reading back the resulting output voltage for each DAC.

Complete software documentation is available from the Help menu item, as features may be added periodically.

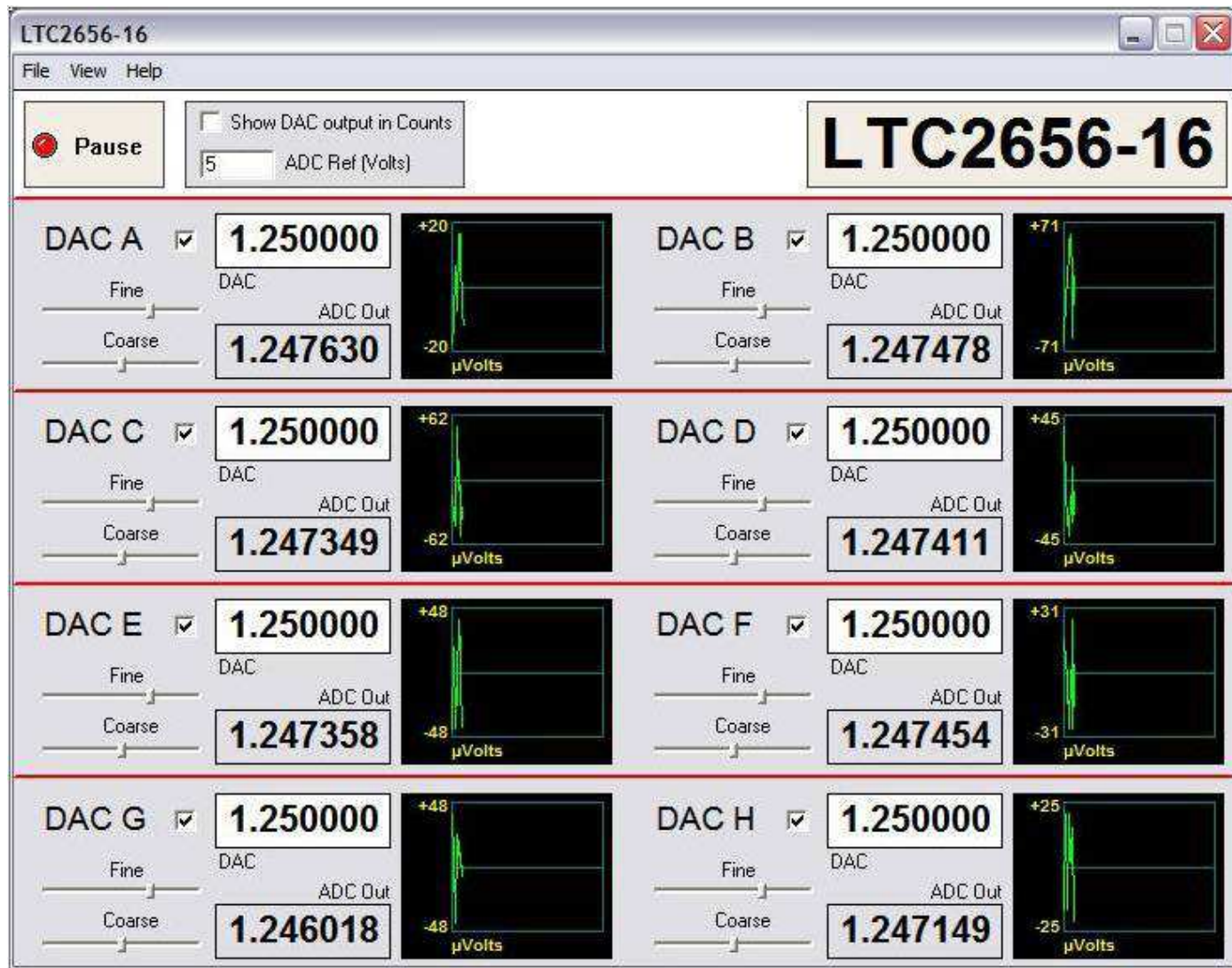


Figure 2. Demo Board Software

HARDWARE SETUP

Jumpers

JP1 – V_{REF} Select. Either a 1.25V/2.048V internal or 1.25V onboard reference can be selected. To apply an external reference through the V_{REF} turret, set jumper to EXT.

JP2 – Power-Up Mode. The LTC2656 can be set to either power up at Mid-Scale or Zero-Scale.

JP3 – ADC Disable. Set to ON for normal operation, with the onboard ADC enabled. For very sensitive noise measurements, the ADC may be disabled. The software will then display a positive full-scale reading.

Analog Connections

DAC Outputs – The eight DAC outputs from the LTC2656 are brought out to turrets labeled DAC A through DAC H. These may be connected to external instruments or other circuitry. DAC outputs are not in alphabetical order on the circuit board.

V_{REF} – The V_{REF} turret is connected directly to the REFIN/OUT pin of the LTC2656.

When one of the onboard references is being used, the reference voltage may be monitored at this point. An external reference may also be applied to this turret after setting JP1 to EXT.

Grounding and Power Connections

Power (V_{CC}) – Normally DC1397B is powered by the DC590 controller. V_{CC} can be supplied to this turret, however the power supply on DC590 must be disabled! Refer to DC590 Quick Start Guide for more details on this mode of operation.

Grounding – Signal ground is connected to the exposed ground planes at the top and bottom edges of the board, and to the two turrets labeled “Gnd.” Use signal ground as the reference point for measurements and connections to external circuits.

DEMO MANUAL DC1397B

PARTS LIST

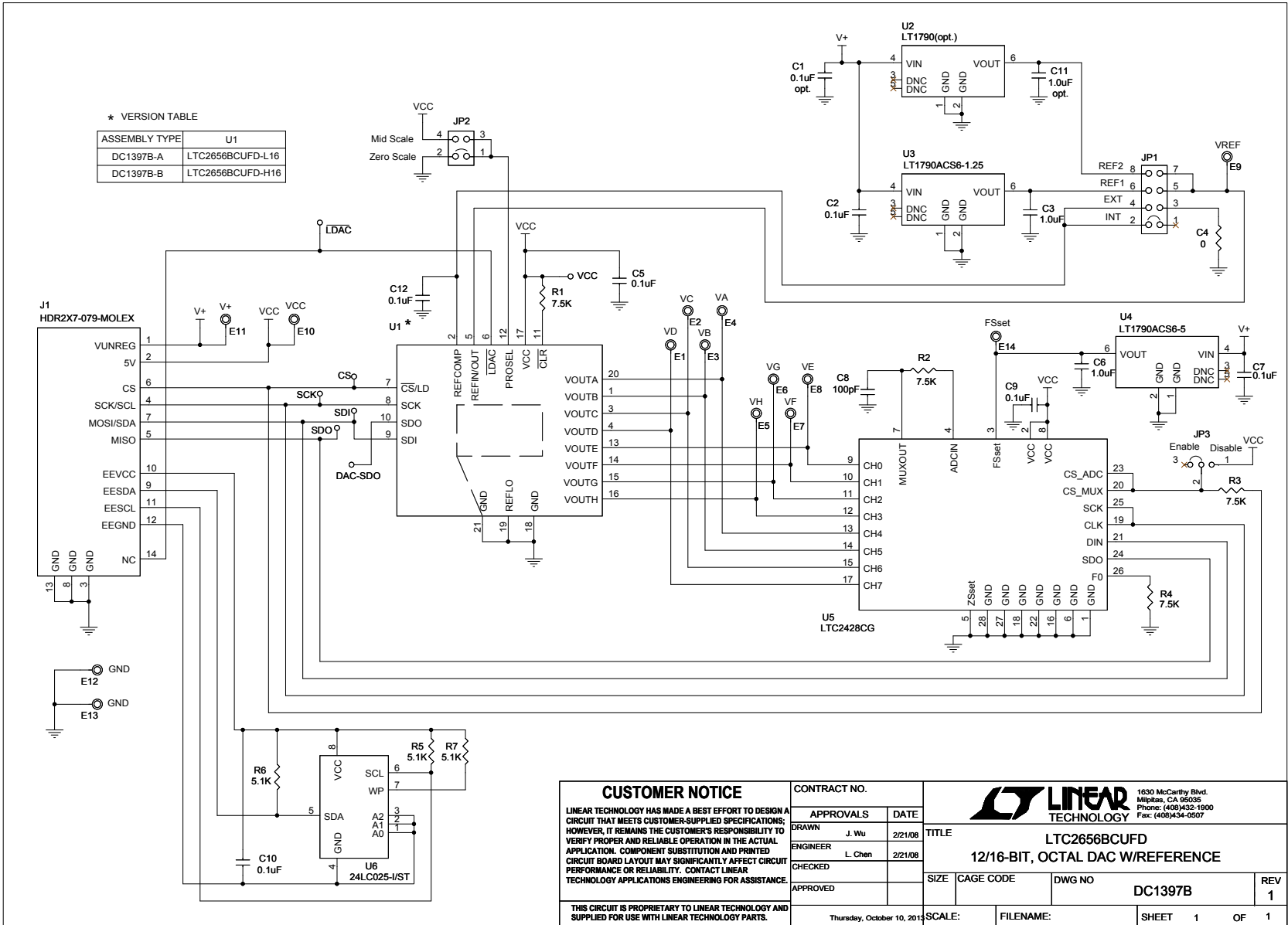
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	0	C1 (Opt.)	CAP., 0402	
2	5	C2, C5, C7, C9, C10	CAP., X7R, 0.1 μ F, 16V, 10% 0402	TAIYO YUDEN, EMK105BJ104KV
3	2	C3, C6	CAP., X7R, 1.0 μ F, 10V, 10% 0603	TAIYO YUDEN, LMK107BJ105KA
4	1	C4	RES., CHIP, 0, 0402	VISHAY, CRCW04020000Z0ED
5	1	C8	CAP., C0G, 100pF, 25V, 5% 0402	AVX, 04023A101JAT2A
6	0	C11 (Opt.)	CAP., 0603	
7	14	E1-E14	TESTPOINT, TURRET, 0.061" PBF	MILL-MAX, 2308-2-00-80-00-00-07-0
8	1	JP1	2X4, 0.079 DOUBLE ROW HEADER	SAMTEC, TMM104-02-L-D
9	1	JP2	2X2, 0.079 DOUBLE ROW HEADER	SAMTEC, TMM102-02-L-D
10	1	JP3	3 PIN 0.079 SINGLE ROW HEADER	SAMTEC, TMM103-02-L-S
11	3	SHUNT	SHUNT, 0.079" CENTER	SAMTEC, 2SN-BK-G
12	1	J1	CONNECTOR, DUAL 2X7 0.079CC	MOLEX, 87831-1420
13	4	R1, R2, R3, R4	RES., CHIP, 7.5k, 1/16W, 5% 0402	VISHAY, CRCW04027K50JNED
14	3	R5, R6, R7	RES., CHIP, 5.1k, 1/16W, 5% 0402	VISHAY, CRCW04025K10JNED
15	0	U2 (Opt.)	I.C., LT1790 SOT23-6	
16	1	U3	I.C., LT1790ACS6-1.25 SOT23-6	LINEAR., LT1790ACS6-1.25#PBF
17	1	U4	I.C., LT1790ACS6-5 SOT23-6	LINEAR., LT1790ACS6-5#PbF
18	1	U5	I.C., LTC2428CG SSOP-28G	LINEAR., LTC2428CG#PBF
19	1	U6	I.C., Serial EEPROM TSSOP8	MICROCHIP, 24LC025-I/ST
Assembly Type-A				
20	1	U1	I.C., LTC2656BCUFD-L16, UFD-20	LINEAR TECH
Assembly Type-B				
20	1	U1	I.C., LTC2656BCUFD-H16, UFD-20	LINEAR TECH

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
B	10/13	Add REFCOMP Capacitor	Throughout

* VERSION TABLE

ASSEMBLY TYPE	U1
DC1397B-A	LTC2656BCUFD-L16
DC1397B-B	LTC2656BCUFD-H16



CUSTOMER NOTICE		CONTRACT NO.				
<p>LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.</p>		APPROVALS	DATE	<p>1630 McCarthy Blvd. Milpitas, CA 95035 Phone: (408)432-1900 Fax: (408)434-0507</p>		
		DRAWN	J. Wu			2/21/08
		ENGINEER	L. Chen			2/21/08
		CHECKED				
<p>THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.</p>		APPROVED		TITLE	LTC2656BCUFD 12/16-BIT, OCTAL DAC W/REFERENCE	
		Thursday, October 10, 2013	SCALE:	FILENAME:	DC1397B	
					REV 1	
					SHEET 1 OF 1	

DEMO MANUAL DC1397B

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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