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LT1222 and LT1793 Low Noise Transimpedance Amplifier

DESCRIPTION

Demonstration circuit 1416 is a low noise transimpedance amplifier. It utilizes the low voltage noise LT[®]1222 op amp, and the low current noise LT1793 op amp, along with the discrete NXP JFET BF862¹ or equivalent, allowing the user to take advantage of each component's particular opti-

mization. These components are arranged with jumpers allowing various composite configurations. A socketed photodiode, OSRAM SFH213, is also provided.

Design files for this circuit board are available at <http://www.linear.com/demo/DC1416>

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PERFORMANCE SUMMARY

Specifications are at $T_A = 25^\circ\text{C}$, $V_S = \pm 12\text{V}$

| SYMBOL | PARAMETER | CONDITIONS | TYP | UNITS |
|--------------|------------------------------|---|-------------|------------------------------|
| V_S | Supply Voltage | | ± 12 | V |
| A_Z | TIA Gain | | 1M | Ω |
| V_{OS} | Input Offset Voltage | LT1793 ($V_{OS} + I_{BIAS} \cdot 10\text{M}$) | 300 | μV |
| dV_{OS}/dT | Input Offset Voltage Drift | LT1793 ($dV_{OS}/dT + dI_{BIAS}/dT \cdot 10\text{M}$) | 10 | $\mu\text{V}/\text{C}$ |
| I_{BIAS} | Input Bias Current | LT1793 + BF862 ¹ | 6 | pA |
| e_n | Input Voltage Noise Density | $f = 100\text{kHz}$, JFET In Gain Configuration | 1 | $\text{nV}/\sqrt{\text{Hz}}$ |
| e_n | Input Voltage Noise Density | $f = 100\text{kHz}$, Source Follower Configuration | 3 | $\text{nV}/\sqrt{\text{Hz}}$ |
| C_{IN} | Input Capacitance | $f = 10\text{kHz}$, Source Follower Configuration | 2 | pF |
| GBW | Gain Bandwidth Product | JP In ($C_{COMP} = 49\text{pF}$) | 70 | MHz |
| GBW | Gain Bandwidth Product | JP Out ($C_{COMP} = 10\text{pF}$) | 190 | MHz |
| GBW | Gain Bandwidth Product | JP Out, C7 Removed ($C_{COMP} = 0\text{pF}$) | 500 | MHz |
| BW | -3dB Bandwidth | With SFH213, $1\text{M}\Omega$ Gain, JP7 Out | 2 | MHz |
| V_{OUT} | Output Voltage Swing | Cathode Input, Integrator In | 0 to 10 | V |
| V_{OUT} | Output Voltage Swing | Cathode Input, Integrator Out | -0.4 to -10 | V |
| V_{OUT} | Output Voltage Swing | Anode Input, Integrator In | 0 to -10 | V |
| V_{OUT} | Output Voltage Swing | Anode Input, Integrator Out | -0.4 to -10 | V |
| I_{CC} | Supply Current | $V_S = \pm 12\text{V}$ | 17 | mA |
| I_{BIAS} | Input Bias Current | LT1793 + BF862 ¹ | 6 | pA |
| PSRR | Power Supply Rejection Ratio | $\pm 5\text{V}$ to $\pm 15\text{V}$, Integrator In | 95 | dB |

Note 1) BF862 has been obsoleted as of 2017. On-Semi 2SK932-22 has been substituted, with practically identical performance.

OPERATING PRINCIPLES

Composite amplifiers using single JFET inputs can be classified into two groups: common drain (or “source follower”) and common source (or “JFET in gain”). The standard jumper configuration of this board, as shipped and as indicated on the silkscreen, has the JFET as a source follower.

Another classification is DC accuracy. The LT1793 has been provided on board as an integrator to provide DC

accuracy, overriding the high 400mV or so V_{GS} of the JFET. The standard jumper configuration is “Integrator In”, so the TIA will be DC accurate to within the V_{OS} of the LT1793 (900 μ V max). With the integrator removed from the circuit, the DC error rises to 400mV or so.

The feedback resistor, which sets the TIA gain, is 1M Ω . So the output will respond at 1V per microamp of photocurrent.

QUICK START PROCEDURE

Demonstration circuit 1416 is shipped with the jumpers set for source follower operation with the integrator in. If the jumpers have been changed, restore them to the positions shown in the schematic. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. With power off, connect the +12V, -12V, and Com leads from the power supply to the V^+ , V^- , and GND terminals of the demo circuit, as shown in Figure 1.
2. With power off, connect the V_{OUT} of the demo circuit to an oscilloscope or DMM. You can use either the gold SMA connector or the turrets provided on board, or both. Set a high range such as 2V/DIV on the oscilloscope, or V_{DC} on the DMM.
3. Turn on the power supply.
4. You should now be able to wave your hand over the clear photodiode provided on the board (upper left of Figure 1) and see the effect in both DC signal and noise. With the photodiode in darkness, or removed from its socket, the output should sit near ground.
5. You can now connect an optical source to excite the photodiode in a more controlled manner. The easiest way is to drive an LED directly from a function generator, with the function generator’s internal 50 Ω source impedance as a current limiter. Any standard color or IR LED can be used, as the photodiode provided has a wide sensitivity. Be careful not to overdrive sensitive devices such as small lasers.
6. You can now decide whether to play with other configurations (JFET in gain, integrator out, more compensation, etc), or to replace the provided photodiode with the one you intend to use.

QUICK START PROCEDURE

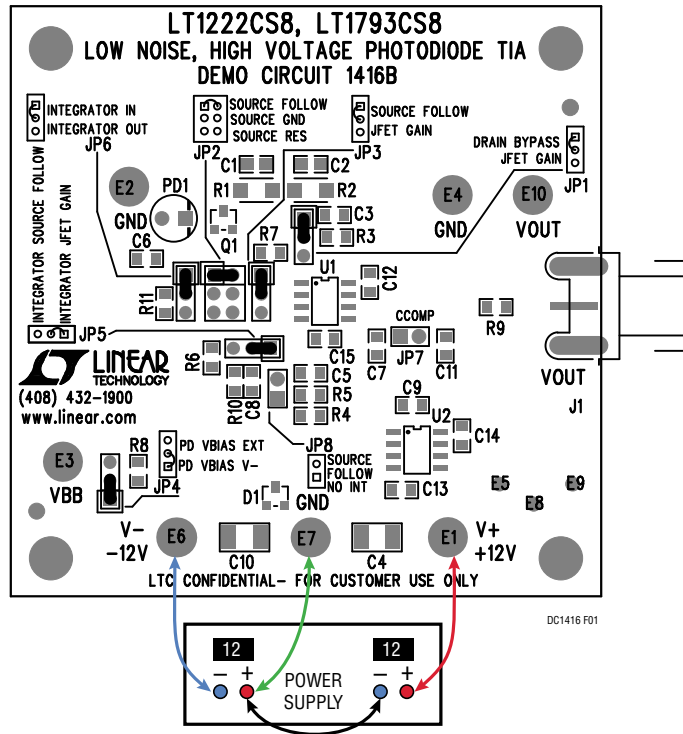


Figure 1. Proper Supply Connections. Board Is Shown for Source Follower with Integrator In (JP1 through JP6 Have Shunt in Position 1. JP7 and JP8 Are Open.)

Table 1. Jumper Settings for Various Configurations. Refer to Figures 2 and 3 for Qualitative Descriptions of the Configurations and to Figure 4 for the Complete Schematic.

| JUMPER | TYPE | CIRCUIT | SOURCE FOLLOWER INTEGRATOR IN | SOURCE FOLLOWER INTEGRATOR OUT | JFET IN GAIN INTEGRATOR IN | JFET IN GAIN INTEGRATOR OUT |
|--------|------|---------------------|-------------------------------|--------------------------------|----------------------------|-----------------------------|
| JP1 | 1x3 | JFET Drain | 1, 2 | 1, 2 | 2, 3 | 2, 3 |
| JP2 | 2x3 | JFET Source | 1, 2 | 1, 2 | 5, 6 | 3, 4 |
| JP3 | 1x3 | LT1222 -Input | 1, 2 | 1, 2 | 2, 3 | 2, 3 |
| JP4 | 1x3 | Photodiode Bias | 1, 2 | 1, 2 | 1, 2 | 1, 2 |
| JP5 | 1x3 | Integrator Output | 1, 2 | Out | 2, 3 | Out |
| JP6 | 1x3 | Integrator Input | 1, 2 | 2, 3 | 1, 2 | 2, 3 |
| JP7 | 1x2 | LT1222 Compensation | Out | Out | In | In |
| JP8 | 1x2 | LT1222 +Input | Out | In | Out | Out |

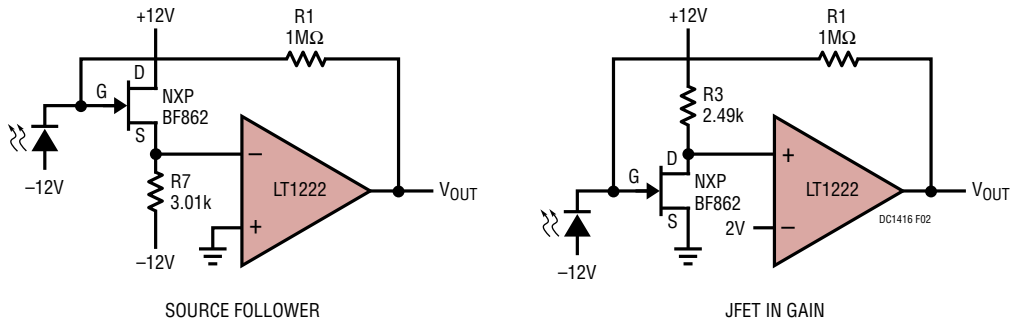


Figure 2. The Two Basic Types of JFET Configuration. The Left Shows the JFET as a Source Follower, Simply Buffering the Feedback Resistor to the Op Amp's Inverting Input. The Right Shows the JFET In Gain, with Source Grounded. Because the JFET Inverts, the Feedback Is Now Applied to the Op Amp's Non-Inverting Input. In Both Cases, the Effective Input Offset Voltage Is One JFET V_{GS} (About -400mV). The Source Follower Configuration Is the Simplest and Most Versatile, but the JFET In Gain Configuration Offers the Highest Achievable Gain-Bandwidth Product and the Lowest Voltage Noise. Output Noise at Low and Medium Frequencies (10kHz to 100kHz) Is $130nV/\sqrt{Hz}$, Dominated Entirely by the Feedback Resistor

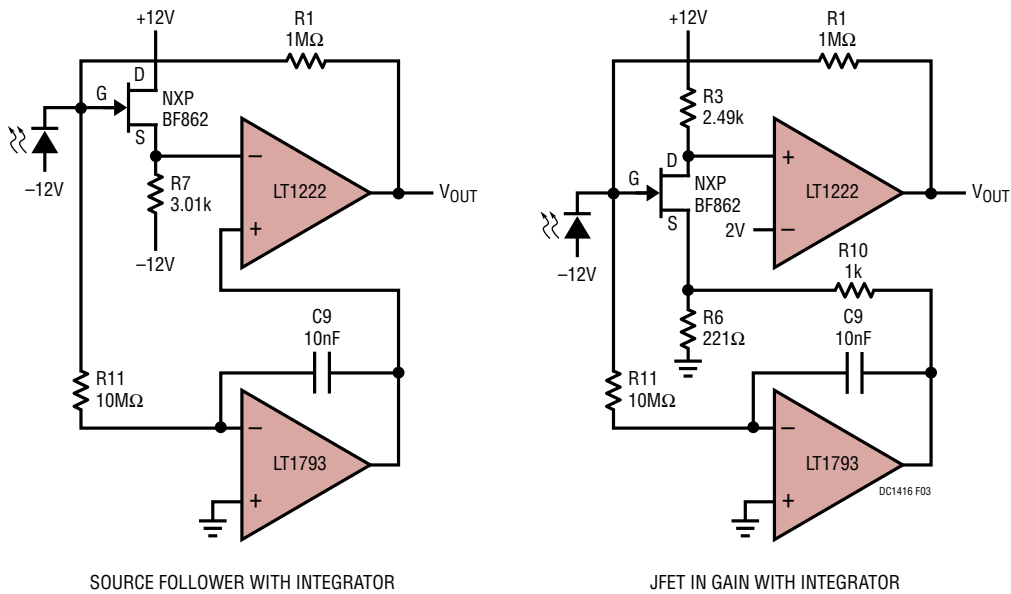


Figure 3. The Two Basic Types of JFET Configuration Again, but Shown with LT1793 Integrators which Zero Out the Overall Input Offset Voltage. On the Left, the JFET V_{GS} Is Forced to the LT1793 Non-Inverting Input. On the Right, the Integrator Puts JFET V_{GS} at the Source Directly. In both Cases, the 10M Sensing Resistor R11 Injects $40fA/\sqrt{Hz}$ of Current Noise, which Is Discernible but Relatively Small Compared to the $130fA/\sqrt{Hz}$ of the 1M Feedback Resistor. The Output Noise at Low to Medium Frequencies Is about $136nV/\sqrt{Hz}$

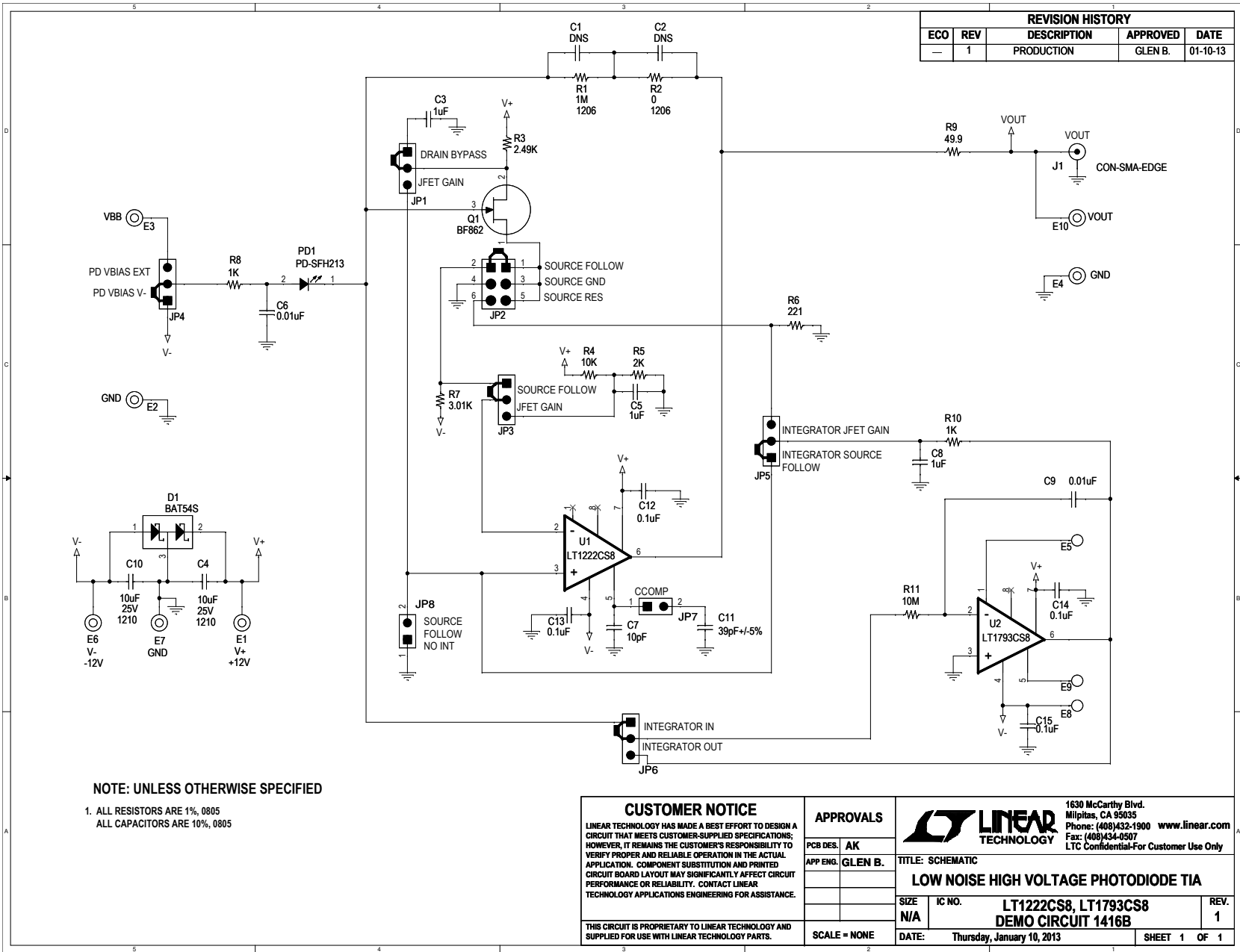


Figure 4. DC1416 Demo Circuit Schematic

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