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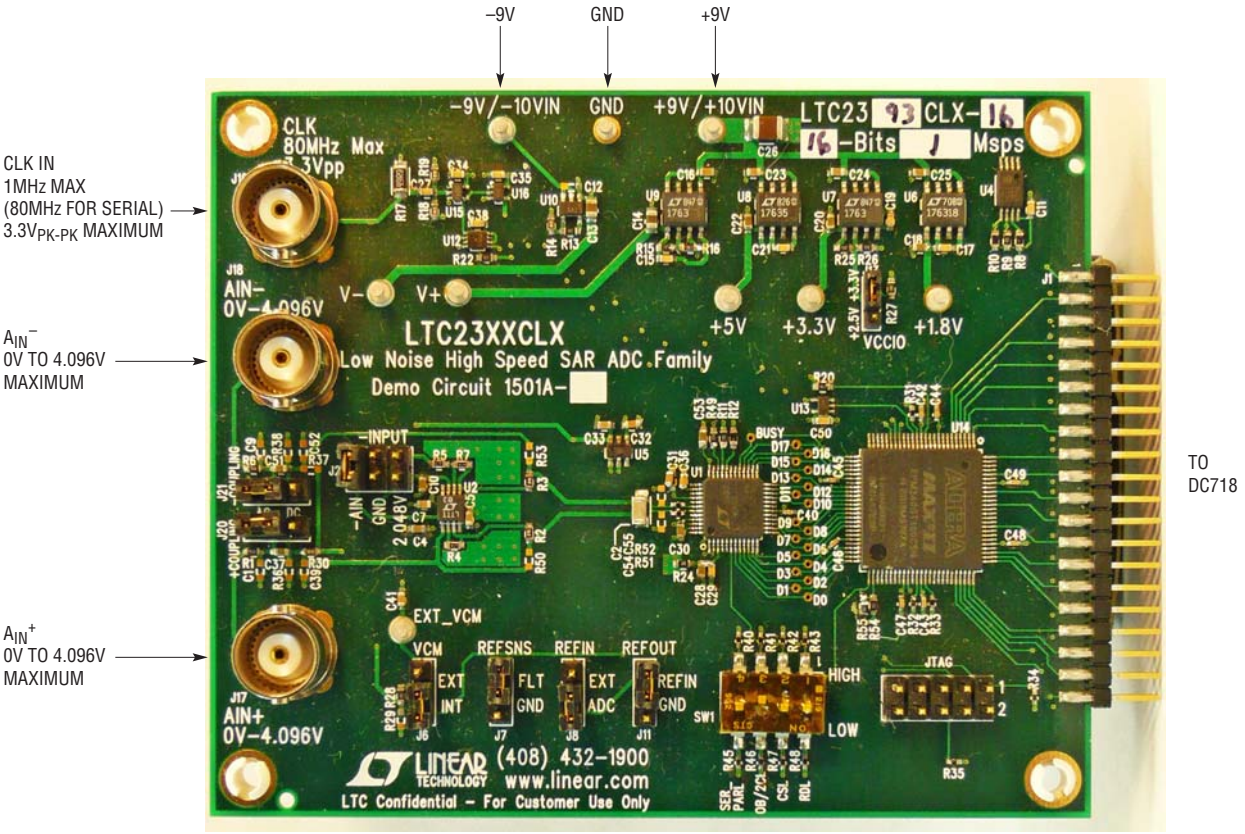
LTC2393-16/LTC2392-16/ LTC2391-16, 1MSPS, 0.5MSPS, 0.25MSPS Low Noise ADC

DESCRIPTION

The LTC2393-16 family are low noise high speed ADCs with both parallel and serial outputs that can operate from a single 5V supply. The LTC2393-16 family supports a large ±4.096V fully differential input range. This makes them ideal for high performance applications that require maximum dynamic range. Demonstration circuit 1501A provides the user a means of evaluating the performance of these ADCs in both parallel and serial modes and is intended to demonstrate recommended grounding, part placement, routing and bypassing for this family of parts. Also several suggested driver circuits for the analog inputs will be presented.

Design files for this circuit board are available at http://www.linear.com/demo.



DEMO BOARD	IC	MAX SAMPLE RATE	PARALLEL MAX CLK IN	SERIAL MAX CLK IN
DC1501A-A	LTC2393CLX-16	1Msps	1MHz	80MHz
DC1501A-B	LTC2392CLX-16	0.5Msps	0.5MHz	40MHz
DC1501A-C	LTC2391CLX-16	0.25Msps	0.25MHz	20MHz

Figure 1. DC1501A Connection Diagram

DC718B/C QUICK START PROCEDURE

Check to make sure that all switches and jumpers are set as shown in the connection diagram of Figure 1. The default connections configure the ADC for parallel operation with the output data in offset binary format. The analog input is AC-coupled and the internal reference of the ADC is used.

Connect DC1501A to a DC718B/C USB High Speed Data Collection Board using connector J1. Connect DC718B/C to a host PC with a standard USB A/B cable. Apply ±9V to the indicated terminals. Apply a low jitter signal source to J17. The default setup uses a single-ended to differential converter so that it is only necessary to apply an input signal to J17. Connect a low jitter 1MHz 3.3V_{P-P} sine wave or square wave to connector J16 for LTC2393-16. Apply 500kHz for LTC2392-16 and 250kHz for LTC2391-16. Note that J16 has a 50Ω termination resistor to ground.

Run the QuickEval-II software (Pscope.exe version K66 or later) supplied with DC718B/C or download it from www.linear.com.

Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

The Pscope software should recognize DC1501A and configure itself automatically.

Click the Collect button (See Figure 6) to begin acquiring data. The Collect button then changes to Pause, which can be clicked to stop data acquisition.

DC1501A SETUP

DC Power

DC1501 requires ±9VDC at approximately 100mA. Most of the supply current is consumed by the CPLD, op amps, regulators and discreet logic on the board. The ±9VDC input voltage powers the ADC through LT1763 regulators which provide protection against accidental reverse bias. Additional regulators provide power for the CPLD and op amps. See Figure 1 for connection details.

Clock Source

You must provide a low jitter 3.3V_{P-P} sine or square wave to J16. The clock input is AC-coupled so the DC level of the clock signal is not important. A generator like the HP8644 or similar is recommended. Even a good generator can start to produce noticeable jitter at low frequencies. Therefore it is recommended for lower sample rates to divide down a higher frequency clock to the desired sample rate. One way to accomplish this is by placing the ADC in the serial mode. This can be accomplished by setting the SER/PARL position of SW1 to the high position. In the serial mode the ratio of clock frequency to conversion rate is 80:1. This limits the max clock frequency of DC1501A-A to 80MHz in serial mode. DC1501A-B is limited to 40MHz and DC1501A-C is limited to 20MHz. In the parallel mode there is a 1:1 ratio of clock frequency to conversion rate. If the clock input is to be driven with logic, it is recommended that the 50Ω terminator (R17) be removed. Slow rising edges may compromise SNR of the converter in the presence of high-amplitude higher frequency input signals.

Data Output

Parallel data output from this board (0V to 3.3V default), if not connected to DC718, can be acquired by a logic analyzer, and subsequently imported into a spread-sheet, or mathematical package depending on what form of digital signal processing is desired. Alternatively, the data can be fed directly into an application circuit. Use pin 3 of J1 to latch the data. The data can be latched using either edge of this signal. The data output signal levels at J1 can also be reduced to 0V to 2.5V if the application circuit cannot tolerate the higher voltage. This is accomplished by moving J13 to the 2.5V position.

DC1501A SETUP

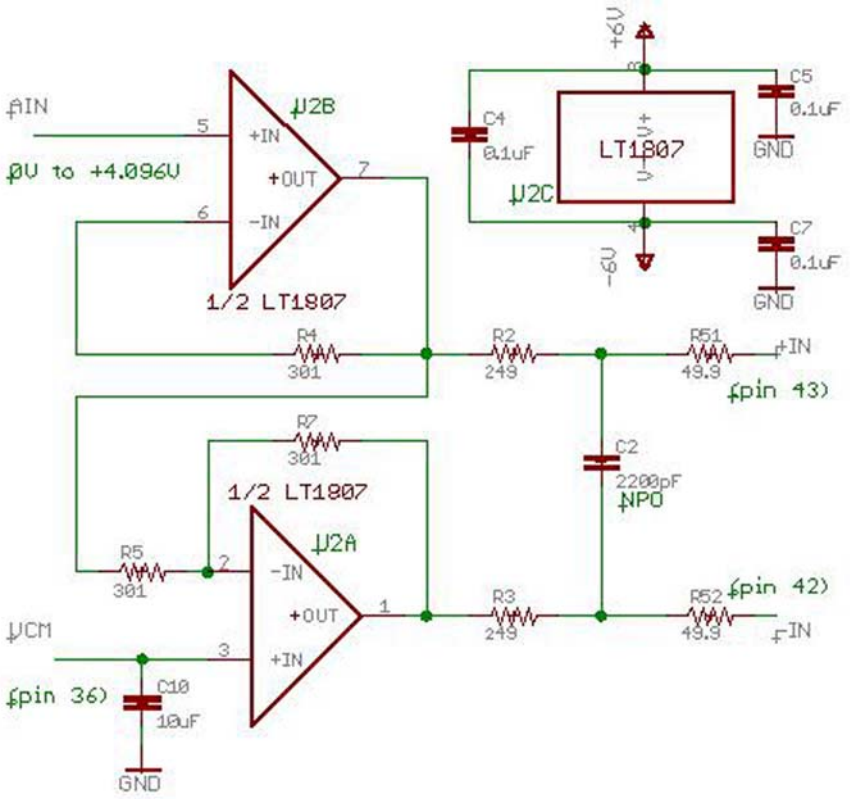


Figure 2. Single-Ended to Differential Converter

Reference

J7, J8 and J11 allow you to select an on chip reference or an external LT1790A-4.096 as the reference. The initial tolerance and drift specifications of the external reference are better than the on chip reference. To use the internal reference set J7 to FLT, J8 to ADC and J11 to REFIN. To use the LT1790A-4.096 set J7 and J11 to GND and J8 to EXT.

Analog Input

The default driver for the analog inputs of the LTC2393 family on DC1501A is shown in Figure 2. This circuit converts a single-ended 0V to 4.096V input signal applied at A_{IN} into a differential signal with a swing of ±4.096V between the $^{+}$IN and $^{-}$IN inputs of the ADC. In addition this circuit band limits the input frequencies to approximately 100kHz which is the useful bandwidth of these ADCs.

Alternatively, if your application circuit produces a differential signal which can drive the ADC but you need to level shift the input signal, the circuits of Figure 3 and Figure 4 can be used. The circuit of Figure 3 AC-couples the input signal and is usable down to about 10kHz. The lower frequency limit can be extended by increasing C37 and C51. The circuit of Figure 3 can be implemented on DC1501A by putting J20 and J21 in the AC position and moving R2 and R3 to the R50 and R53 positions. One of these RC pairs can be attached to the input of the circuit in Figure 2. This allows a single-ended input signal to be level shifted. This is the default condition for DC1501A. Figure 4's input driver allows the input voltage range to go below ground. It DC-couples and level shifts the analog input at the expense of attenuating the input level by a factor of 2. The circuit of Figure 4 can be implemented on DC1501A by setting V_{CM} to External and biasing the external pin to 4.096V replacing R1 and R6 with 1kΩ, putting J20 and J21 in the DC position and moving R2 and R3 to the R50 and R53 positions.

For SINAD, THD or SNR testing a low noise, low distortion generator such as the B&K Type 1051 or Stanford Research DS360 should be used.

DC1501A SETUP

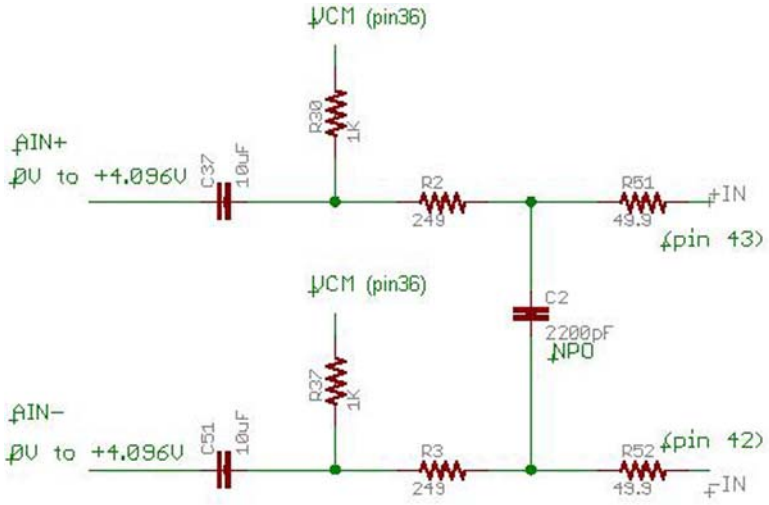


Figure 3. AC-Coupled Differential Driver

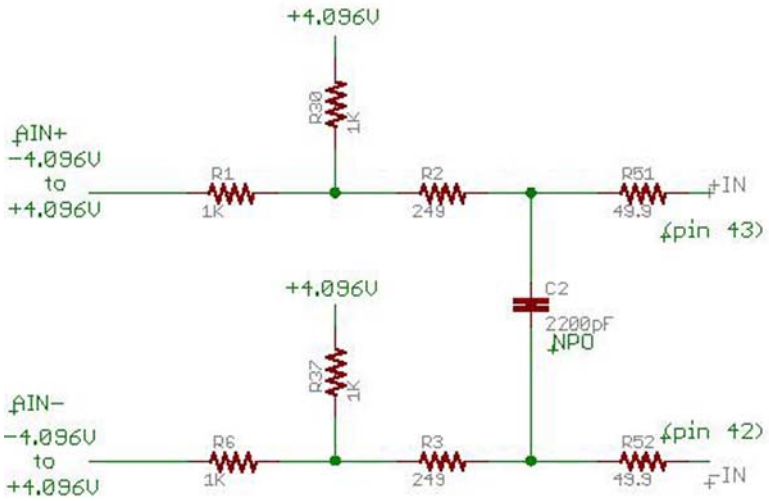


Figure 4. DC Coupled Differential Driver

Data Collection

This demo board is tested in house by duplicating the FFT plot shown in the ADC data sheet. This involves using a low jitter, 1MHz (500kHz for LTC2392-16, 250kHz for LTC2391-16) clock source for the encode clock, along with a low noise, low distortion sinusoidal generator at a frequency of 20kHz. The input signal level is approximately –1dBfs.

The input is filtered with a 20kHz single pole RC filter shown in Figure 5. The FFT shown in the data sheet is a 16384-point FFT. A typical FFT obtained with DC1501A is shown in Figure 6. Note that to get the real SNR, the signal level (–1dB) has to be added back to the SNR that PScope displays. With the example shown in Figure 6 this means that the actual SNR would be 94.061dB. Taking the RMS sum of the recalculated SNR and the THD yields a SINAD of 93.75dB which is fairly close to the typical value for this ADC.

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that is common is feeding the converter with a frequency, that is a sub-multiple of the sample rate, and which will only exercise a small subset of the possible output codes.

DC1501A SETUP

If you do not have a signal generator capable of ppm levels of frequency accuracy or if it cannot be slaved to the clock frequency, you can use an FFT with windowing to reduce the "leakage" or spreading of the fundamental, to get a close approximation of the performance parameters. If an amplifier or clock source with poor phase noise is used, the windowing will not improve the SNR.

The signal source typically used for in house testing is a B&K 1051. A low jitter RF oscillator such as the HP8644 is used as the clock source. As with any high performance ADC, this part is sensitive to layout. The area immediately surrounding the ADC on DC1501 should be used as a guideline for placement, and routing of the various components associated with the ADC. Note should also be taken of the ground plane used in the layout of this board.

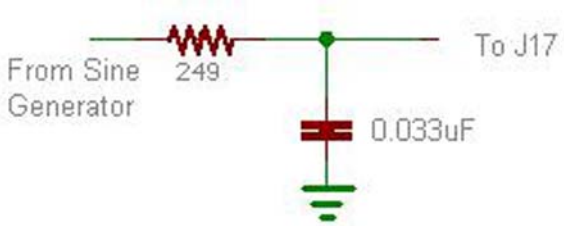


Figure 5. 20kHz RC filter

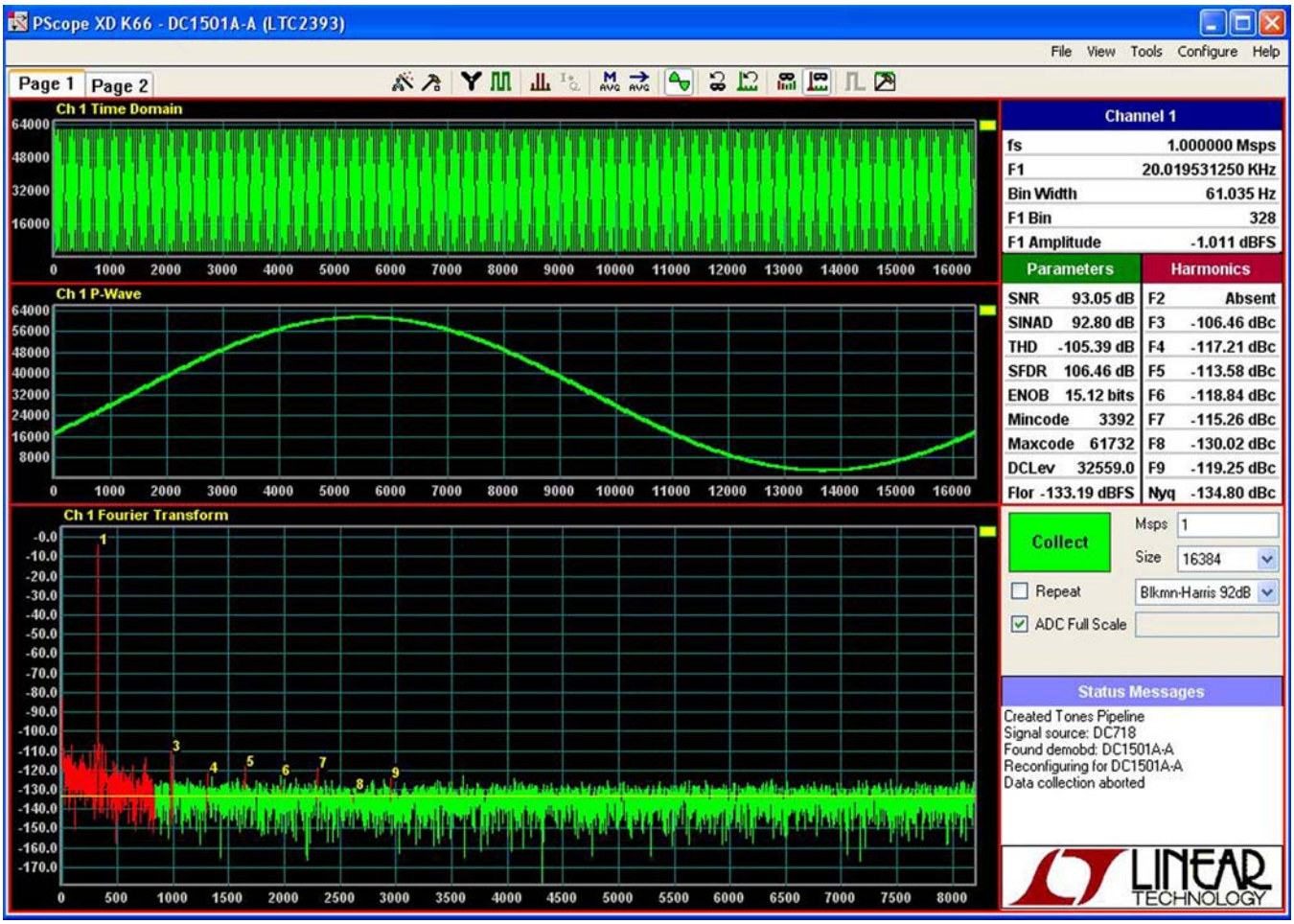


Figure 6. DC1501A FastDAACS Screenshot

DC1501A MISCELLANEOUS DIP SWITCHES AND JUMPERS

Definitions

J2- -INPUT sets the bias point for the –input of U2A. The default is $^{-}A_{IN}$.

J6- V_{CM} sets the DC bias for A_{IN}^{+} and A_{IN}^{-} when the inputs are AC-coupled. INT is the default position.

SW1-

SER_PARL- Selects serial or parallel operation. Default position is parallel. In parallel mode fs= fclk. In serial mode fs = fclk/80.

OB/2CL- Selects offset binary or two's complement data format for ADC output word. The default is offset binary.

CSL- This pin must be kept low for normal operation.

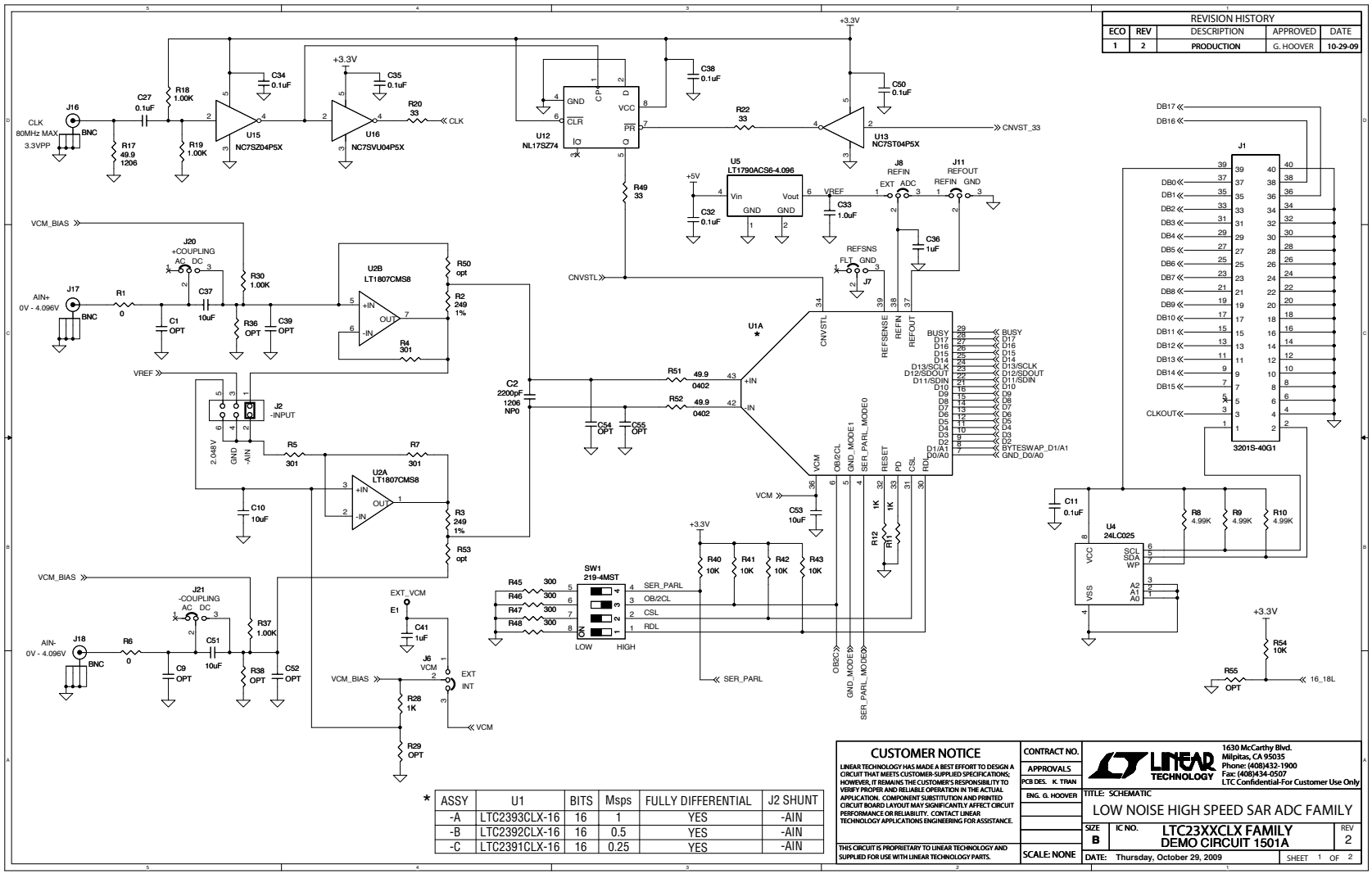
RDL- This pin must be kept low for normal operation.

PARTS LIST

ITEM	QUANTITY	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURERS PART NUMBER
			REQUIRED CIRCUIT COMPONENTS:	
1	0	C1, C9, C39, C52, C54, C55 (opt.)	CAP., 0603	
2	1	C2	CAP., NP0, 2200pF, 25V, 5% 1206	AVX, 12063A222JAT2A
3	11	C4, C5, C7, C12, C16, C23-C25, C33, C36, C41	CAP., X7R, 1µF, 16V, 10% 0603	AVX, 0603YC105KAT2A
4	9	C10, C18, C20, C22, C28, C30, C37, C51, C53	CAP., X5R, 10µF, 6.3V, 20% 0603	Taiyo Yuden, JMK107BJ106MA (2rls, PbF)
5	2	C13, C14	CAP., X5R, 10µF, 10V, 20% 0805	Taiyo Yuden, LMK212BJ106MG
6	9	C11, C27, C29, C31, C32, C34, C35, C38, C50	CAP., X7R, 0.1µF, 25V, 10% 0603	AVX, 06033C104KAT2A
7	4	C15, C17, C19, C21	CAP., X7R, 0.01µF, 50V, 10% 0603	AVX, 06035C103KAT2A
8	1	C26	CAP., X5R, 47µF, 16V, 20% 1210	Taiyo Yuden, EMK325BJ476MM
9	1	C40	CAP., X5R, 4.7µF, 4V, 20% 0402	Taiyo Yuden, AMK105BJ475MV-F
10	8	C42-C49	CAP., X5R, 0.1µF, 10V, 10% 0402	AVX, 0402ZD104KAT2A
11	9	E1-E9	Testpoint, Turret, .061" pbf	MILL-MAX, 2308-2-00-80-00-00-07-0
12	1	J1	Header, .1 × .1 CNTRS, 40-Pin	Samtec, TSW-120-07-L-S
13	1	JTAG	0.1" × 5 Double Row Header	Samtec, TSW-105-07-L-D
14	1	J2	0.1" × 3 Double Row Header	Samtec, TSW-103-07-L-D
15	6	J6, J7, J8, J11, J20, J21	3-Pin 0.1" Single Row Header	Samtec, TSW-103-07-L-S (PbF)
16	8	XJTAG, XJ2, XJ6-J8, XJ11, XJ19-J21	Shunt, 0.1" Center	Samtec, SNT-100-BK-G (PbF)
17	1	J13	3-Pin 2mm Single Row Header	Samtec, TMM103-02-L-S
18	1	XJ13	Shunt, 2mm Center	Samtec, 2SN-BK-G
19	3	J16, J17, J18	CONN, BNC, 5-Pins	Connex, 112404
20	2	R1, R6	RES., Chip, 0, 1/10W, 0603	Vishay, CRCW06030000Z0EA
21	2	R2, R3	RES., Chip, 249, 1/10W, 1% 0603	Vishay, CRCW0603249RFKEA
22	3	R4, R5, R7	RES., Chip, 301, 1/10W, 1% 0603	Vishay, CRCW0603301RFKEA
23	3	R8, R9, R10	RES., Chip, 4.99k, 1/10W, 1% 0603	Vishay, CRCW06034K99FKEA
24	3	R11, R12, R28	RES., Chip, 1k, 1/10W, 5% 0603	Vishay, CRCW06031K00JNEA
25	2	R15, R13	RES., Chip, 3.92k, 1/10W, 1% 0603	Vishay, CRCW06033K92FKEA
26	6	R14, R16, R18, R19, R30, R37	RES., Chip, 1.00k, 1/10W, 1% 0603	Vishay, CRCW06031K00FKEA
27	1	R17	RES., Chip, 49.9, 1/4W, 1% 1206	Vishay, CRCW120649R9FKEA
28	3	R20, R22, R49	RES., Chip, 33, 1/10W, 5% 0603	Vishay, CRCW060333R0JNEA
29	1	R24	RES., Chip, 1.0, 1/10W, 5% 0603	Vishay, CRCW06031R00JNEA
30	1	R25	RES., Chip, 1.69k, 1/10W, 1% 0603	Vishay, CRCW06031K69FKEA
31	1	R26	RES., Chip, 1.54k, 1/10W, 1% 0603	Vishay, CRCW06031K54FKEA
32	1	R27	RES., Chip, 2.80k, 1/10W, 1% 0603	Vishay, CRCW06032K80FKEA
33	0	R29, R36, R38, R50, R53, R55(opt)	RES., Chip, 0603	
34	4	R31, R32, R33, R34	RES., Chip, 1k, 1/16W, 5% 0402	Vishay, CRCW04021K00JNED
35	5	R35, R40, R41, R42, R43	RES., Chip, 10k, 1/16W, 5% 0402	Vishay, CRCW040210K0JNED
36	4	R45, R46, R47, R48	RES., Chip, 300, 1/16W, 5% 0402	Vishay, CRCW0402300RJNED

PARTS LIST

ITEM	QUANTITY	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURERS PART NUMBER
			REQUIRED CIRCUIT COMPONENTS:	
37	2	R51, R52	RES., Chip, 49.9, 1/16W, 1% 0402	Vishay, CRCW040249R9FKED
38	1	R54	RES., Chip, 10k, 1/10W, 5% 0603	Vishay, CRCW060310K0JNEA
39	1	SW1	Switch, 219-4MST,	CTS Electronic Components, 219-4MST
40	1	U2	IC., LT1807CMS8 MSOP-8	Linear Tech., LT1807CMS8#TRPBF
41	1	U4	IC., 24LC025 TSSOP-8	Microchip., 24LC025-T/ST
42	1	U5	IC., LT1790ACS6-4.096, SOT23-6	Linear Tech., LT1790ACS6-4.096#PBF
43	1	U6	IC., LT1763CS8-1.8, SO8	Linear Tech., LT1763CS8-1.8#PBF
44	2	U9, U7	IC., LT1763CS8, SO8	Linear Tech., LT1763CS8#PBF
45	1	U8	IC., LT1763CS8-5, SO8	Linear Tech., LT1763CS8-5#PBF
46	1	U10	IC., LT1964ES5-SD, SOT23-5	Linear Tech., LT1964ES5-SD#PBF
47	1	U12	IC., NL17SZ74, US8	On SEMI., NL17SZ74USG
48	1	U13	IC., NC7ST04P5X SC70-5	Fairchild, NC7ST04P5X
49	1	U14	IC., EPM240GT100C5N TQFP-100	Altera Corp., EPM240GT100C5N
50	1	U15	IC., NC7SZ04P5X SC70-5	Fairchild, NC7SZ04P5X
51	1	U16	IC., NC7SVU04P5X SC70-5	Fairchild, NC7SVU04P5X
52	4	(Stand-Off)	Stand-Off, Nylon 0.25”	Keystone, 8831(Snap On)
53	1		Fab, Printed Circuit Board	Demo Circuit 1501A
1		DC1501A-A		
1	1	DC1501A	General BOM	
2	1	U1	IC., LTC2393CLX-16, LQFP-7X7, 48-Pin	Linear Tech., LTC2393CLX-16#PBF
		DC1501A-B		
1	1	DC1501A	General BOM	
2	1	U1	IC., LTC2392CLX-16 LQFP-7X7, 48-Pin	Linear Tech,. LTC2392CLX-16#PBF
		DC1501A-C		
1	1	DC1501A-C	General BOM	
2	1	U1	IC., LTC2391CLX-16 LQFP-7X7, 48-Pin	Linear Tech,. LTC2391CLX-16#PBF


REVISION HISTORY
ECO | REV | DESCRIPTION | APPROVED | DATE
1 | 2 | PRODUCTION | G. HOOVER | 10-29-09
CUSTOMER NOTICE
LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.
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ENG. G. HOOVER
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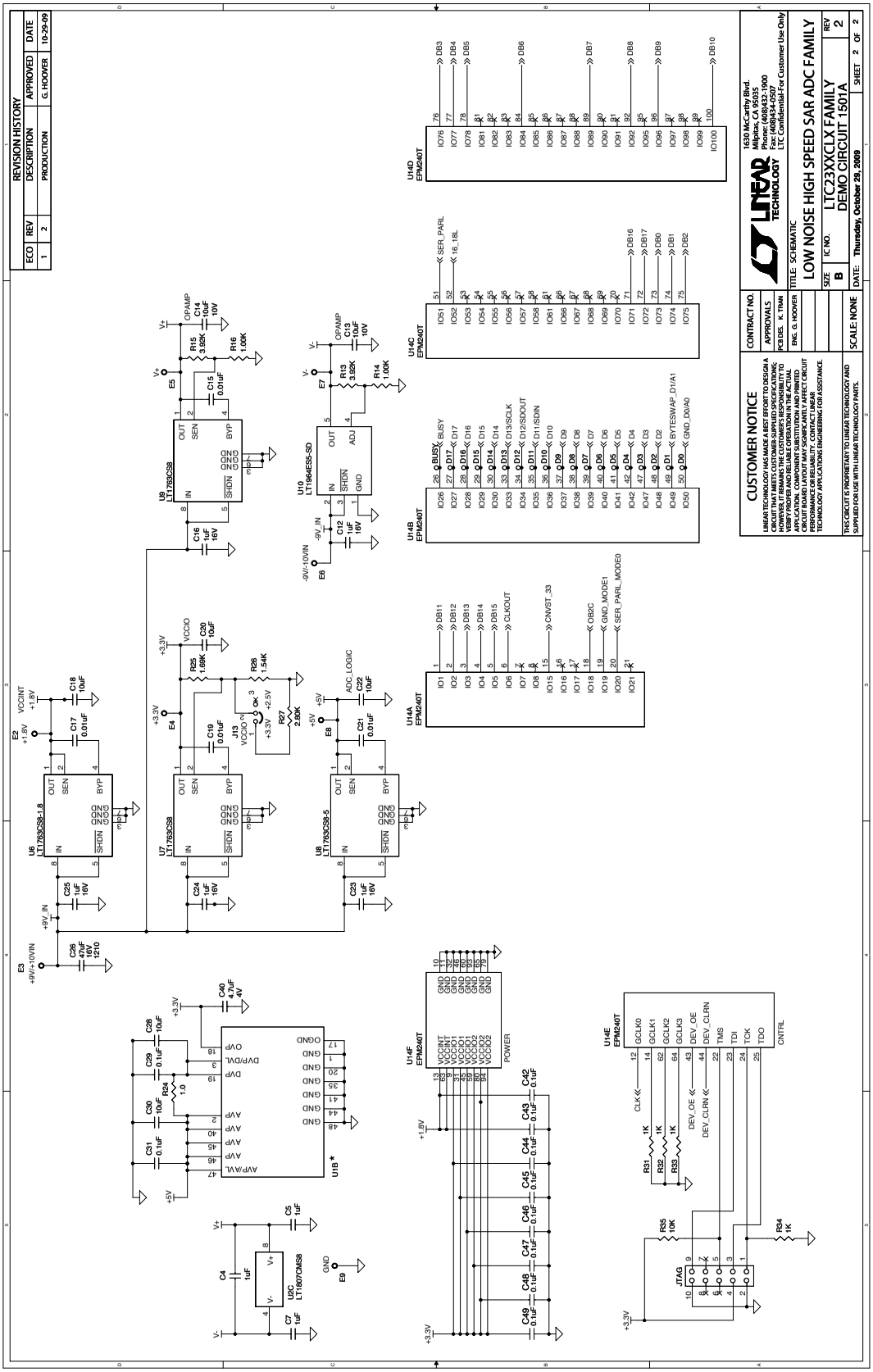
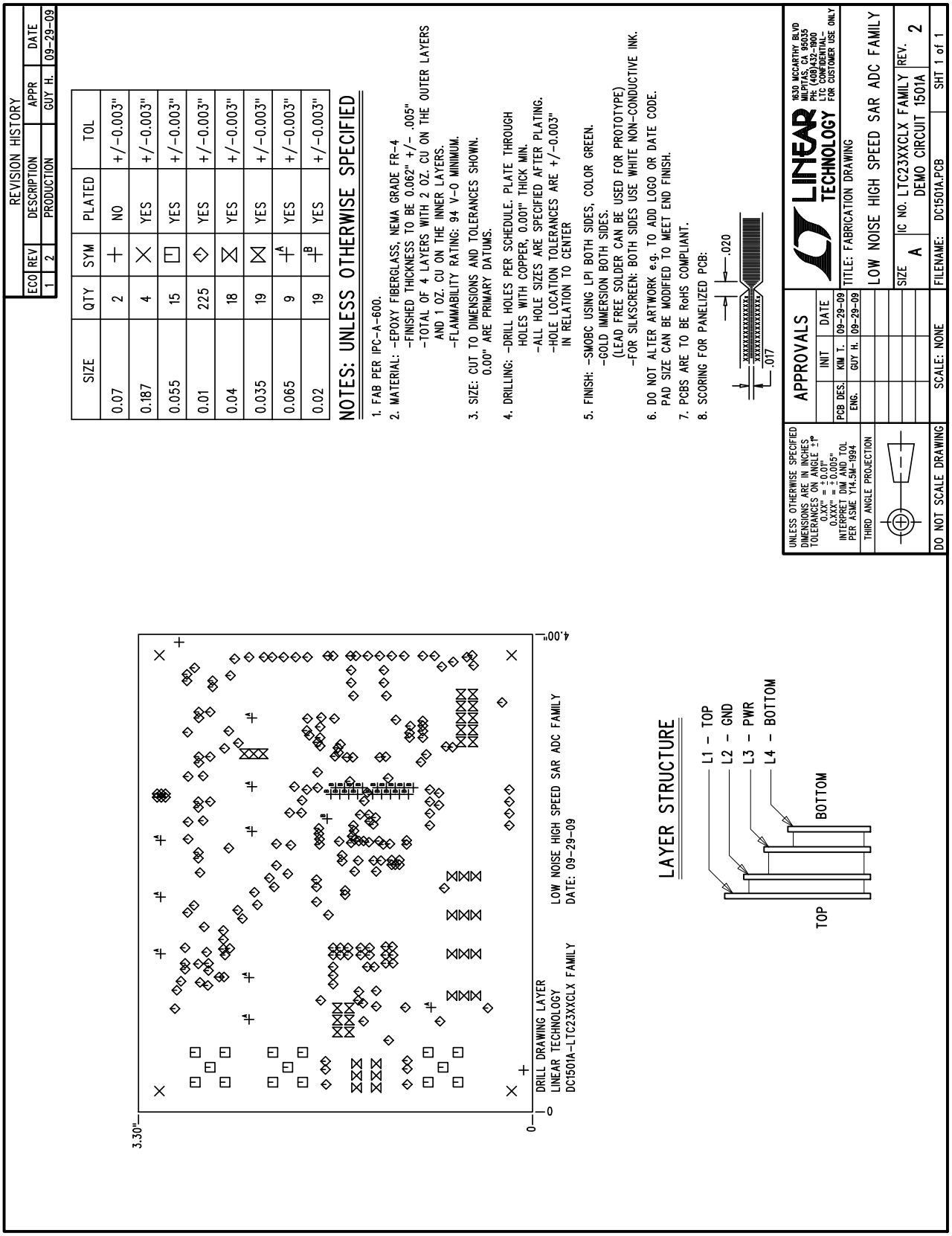
LINEAR TECHNOLOGY
1630 McCarthy Blvd.
Milpitas, CA 95035
Phone: (408)432-1900
Fax: (408)434-0507
LTC Confidential-For Customer Use Only
TITLE: SCHEMATIC
LOW NOISE HIGH SPEED SAR ADC FAMILY
SIZE B
IC NO. LTC23XXCLX FAMILY
DEMO CIRCUIT 1501A
REV 2
DATE: Thursday, October 29, 2009
SHEET 1 OF 2
* ASSY | U1 | BITS | Msps | FULLY DIFFERENTIAL | J2 SHUNT
-A | LTC2393CLX-16 | 16 | 1 | YES | -AIN
-B | LTC2392CLX-16 | 16 | 0.5 | YES | -AIN
-C | LTC2391CLX-16 | 16 | 0.25 | YES | -AIN

SCHEMATIC DIAGRAM

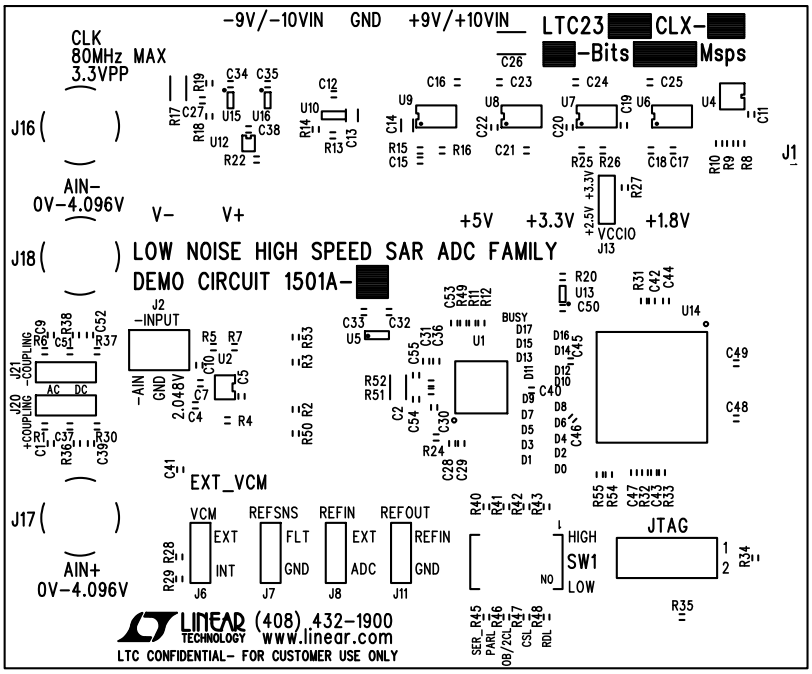


SCHEMATIC DIAGRAM

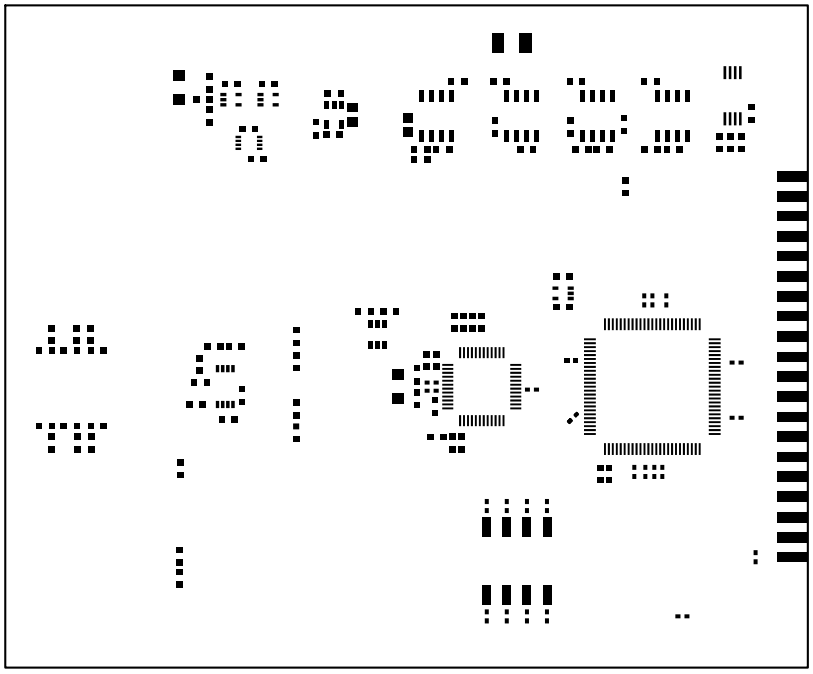


PCB LAYOUT AND FILM

Top Silkscreen

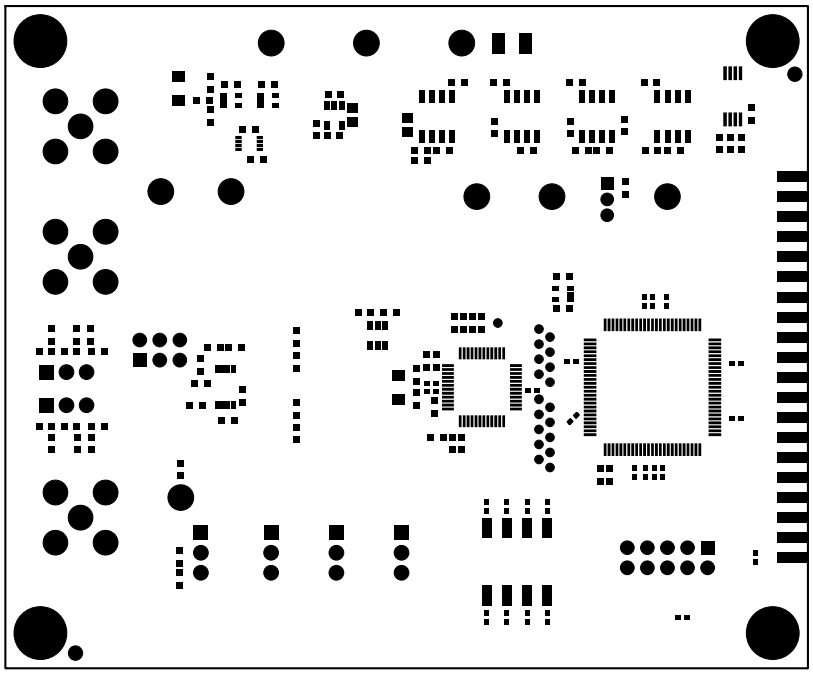


Top Solder Paste

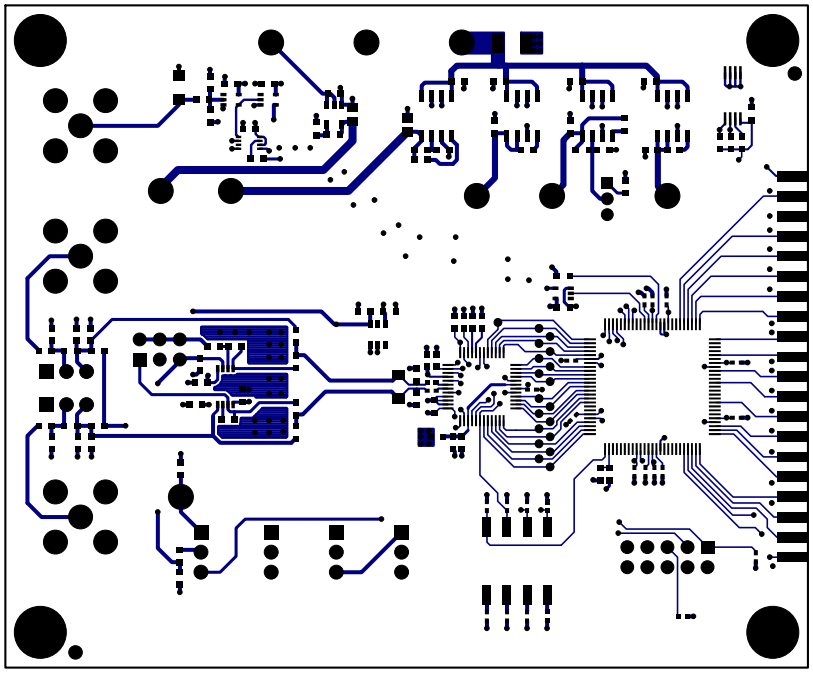


PCB LAYOUT AND FILM

Top Solder Mask

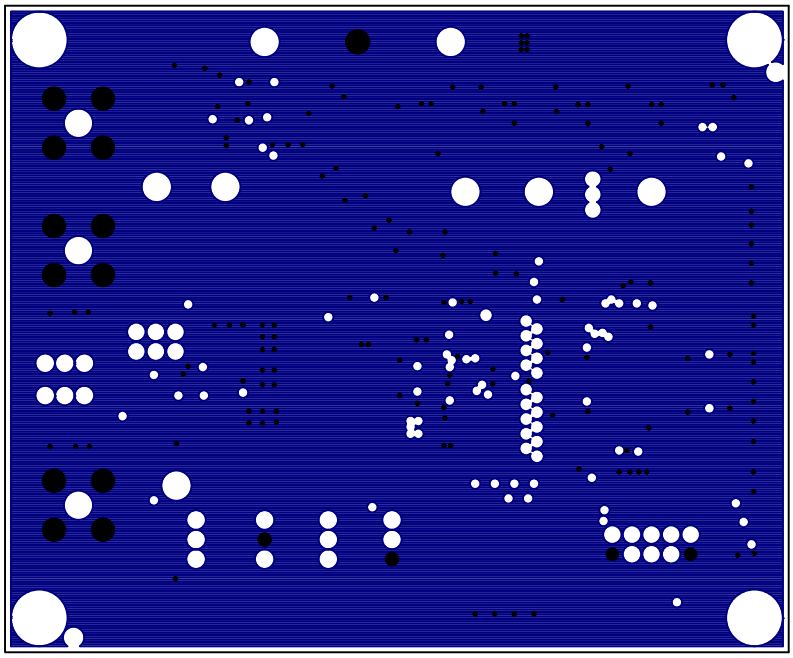


Layer 1 - Top Layer

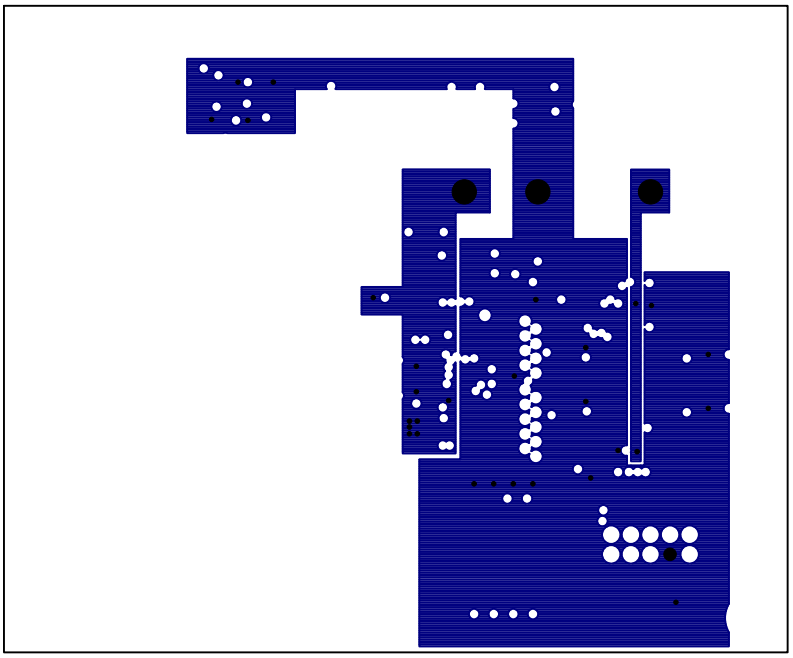


PCB LAYOUT AND FILM

Layer 2 - GND Plane 1

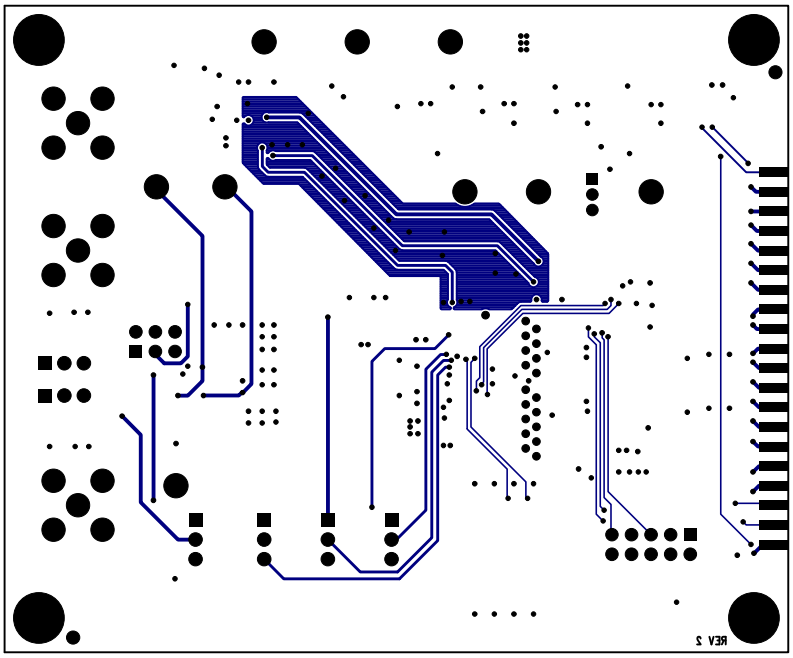


Layer 3 - GND Plane 2

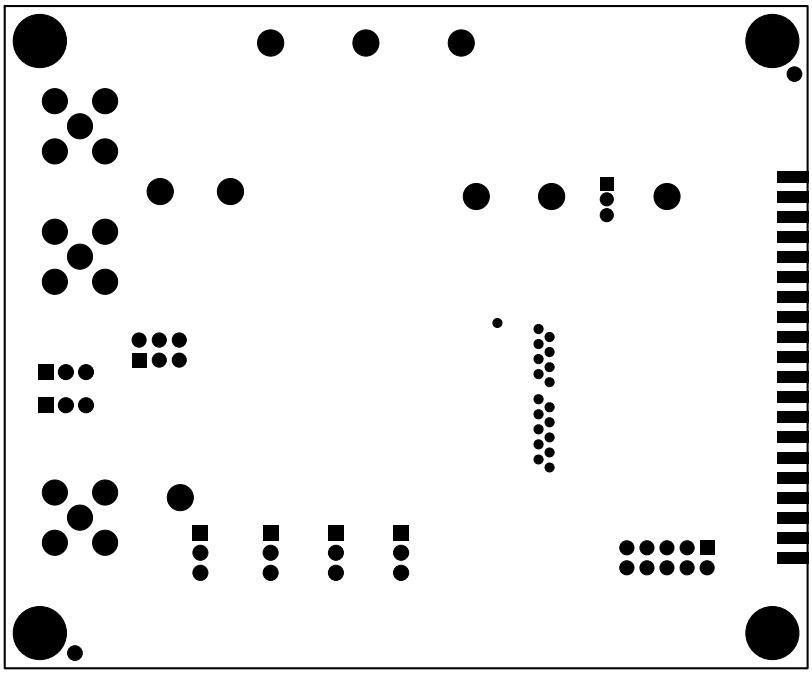


PCB LAYOUT AND FILM

Layer 4 - Bottom Layer



Bottom Solder Mask



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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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