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LTC2158-14, LTC2158-12, LTC2157-14, LTC2157-12, LTC2156-14, LTC2156-12, LTC2155-14, LTC2155-12
12-Bit/14-Bit, 170Msps to 310Msps Dual ADCs

DESCRIPTION

Demonstration circuit 1564A supports a family of 12-/14-bit 170Msps to 310Msps ADCs. Each assembly features one of the following devices: LTC®2158-14/ LTC2158-12, LTC2157-14/LTC2157-12, LTC2156-14/ LTC2156-12, LTC2155-14/LTC2155-12, high speed, dual ADCs.

The versions of the 1564A demo board are listed in Table 1. Depending on the required resolution and sample rate, the DC1564 is supplied with the appropriate ADC. The circuitry on the analog inputs is optimized for analog input frequencies from 5MHz to 140MHz. Refer to the data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at http://www.linear.com/demo

Table 1. DC1564A Variants

DC1564A VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1564A-A	LTC2157-14	14-Bit	250Msps	5MHz to 140MHz
1564A-B	LTC2156-14	14-Bit	210Msps	5MHz to 140MHz
1564A-C	LTC2155-14	14-Bit	170Msps	5MHz to 140MHz
1564A-D	LTC2157-12	12-Bit	250Msps	5MHz to 140MHz
1564A-E	LTC2156-12	12-Bit	210Msps	5MHz to 140MHz
1564A-F	LTC2155-12	12-Bit	170Msps	5MHz to 140MHz
1564A-G	LTC2158-14	14-Bit	310Msps	5MHz to 140MHz
1564A-H	LTC2158-12	12-Bit	310Msps	5MHz to 140MHz

PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage – DC1564A	Depending on Sampling Rate and the A/D Converter Provided, This Supply Must Provide Up to 500mA.	Optimized for 3.6V [3V⇔6.0V Min/Max]
Analog input range	Depending on SENSE Pin Voltage	$1.5V_{P-P}$ or $1.32V_{P-P}$
Logic Input Voltages	Minimum Logic High	1.3V
	Maximum Logic Low	0.6V
Logic Output Voltages (Differential)	Nominal Logic Levels (100Ω Load, 3.5mA Mode)	350mV/1.25V Common Mode
	Minimum Logic Levels (100Ω Load, 3.5mA Mode)	247mV/1.25V Common Mode
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Encode Clock Level	Differential Encode Mode (ENC^- Not Tied to GND)	0.2V to 1.9V
Resolution	See Table 1	

PERFORMANCE SUMMARY (T_A = 25°C)

Input Frequency Range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 1564A is easy to set up to evaluate the performance of the LTC2157 A/D converter family. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

Setup

If a DC1371 Data Acquisition and Collection System was supplied with the DC1564A demonstration circuit, follow the DC1371 Quick Start Guide to install the required software and for connecting the DC1371 to the DC1564A and to a PC.

DC1564A Demonstration Circuit Board Jumpers

The DC1564A demonstration circuit board should have the following jumper settings as default positions: (as per Figure 1)

JP1 – PAR/SER: Selects Parallel or Serial Programming Mode. (Default: Serial)

Applying Power and Signals to the DC1564A Demonstration Circuit

The DC1371 is used to acquire data from the DC1564A, the DC1371 must **first** be connected to a powered USB port and have 5V applied power **before** applying 3.6V to

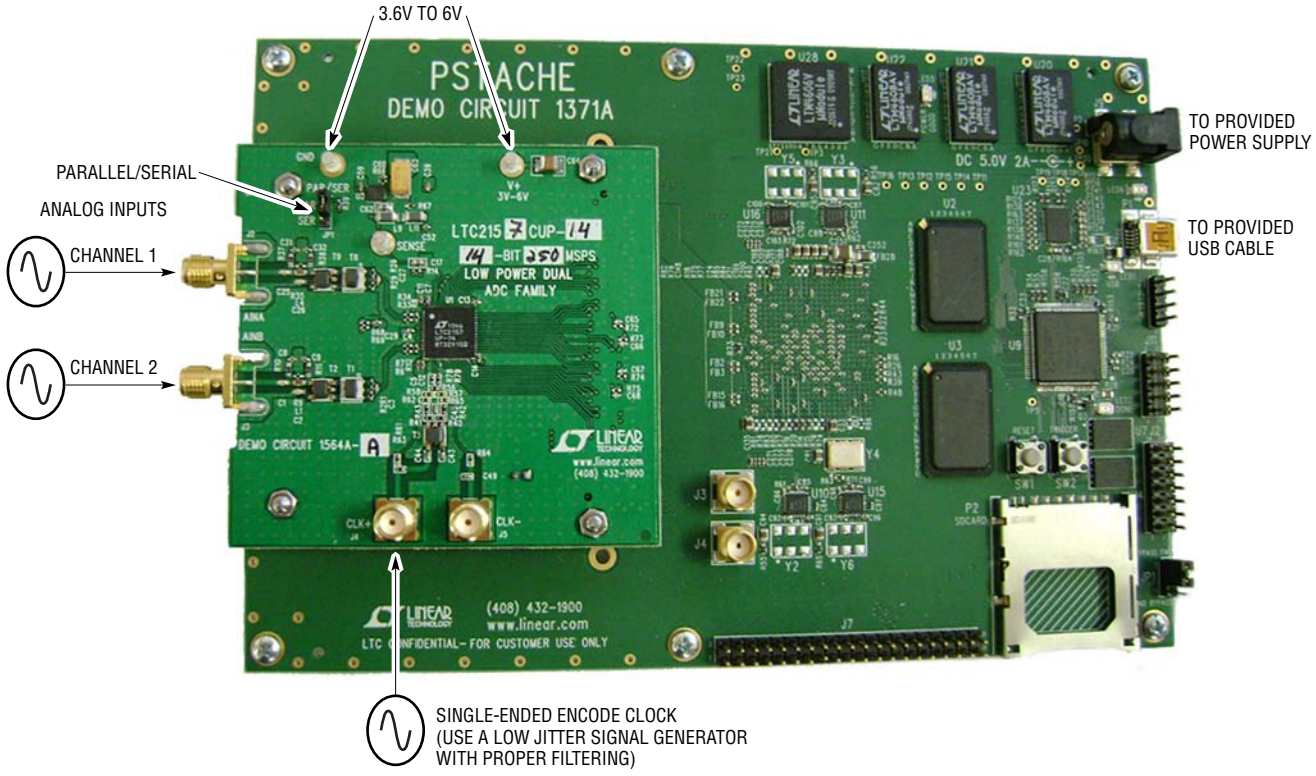


Figure 1. DC1564A Setup (Zoom for Detail)

QUICK START PROCEDURE

6.0V across the pins marked V+ and GND on the DC1564A. The DC1564 requires 3.6V for proper operation.

Regulators on the board produce the voltages required for the ADC. The DC1564A demonstration circuit requires up to 500mA depending on the sampling rate and the A/D converter supplied.

The DC1564A should not be removed, or connected to the DC1371 while power is applied.

Analog Input Network

For optimal distortion and noise performance the RC network on the analog inputs may need to be optimized for different analog input frequencies. For input frequencies above 140MHz, refer to the respective ADC data sheet for a proper input network. Other input networks may be more appropriate for input frequencies less that 5MHz.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

If your generator cannot deliver full-scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC-based operational amplifiers may be unable to deliver the combination of low noise figure and high IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.

Apply the analog input signal of interest to the SMA connectors on the DC1564A demonstration circuit board marked J2 AINA and J3 AINB. These inputs correspond with channels one and two of the ADC respectively. These inputs are capacitively coupled to Balun transformers ETC1-1-13 (lead free part number: MABA007159-000000).

Encode Clock

Note: Apply an encode clock to the SMA connector on the DC1564A demonstration circuit board marked J4 CLK+. As a default the DC1564A is populated to have a single-ended input.

For the best noise performance, the encode input must be driven with a very low jitter, sine wave source. The amplitude should be large, up to $3V_{P-P}$ or 13dBm.

Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. Data sheet FFT plots are taken with 10-pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used for both the clock input and the analog input.

Digital Outputs

The data outputs, data clock, and frame clock signals are available on J1 of the DC1564A. This connector follows the VITA-57/FMC standard, but all signals should be verified when using an FMC carrier card other than the DC1371.

Software

The DC1371 is controlled by the PScope™ system software provided or downloaded from the Linear Technology website at http://www.linear.com/software/.

To start the data collection software, if PScope.exe is installed (by default) in \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1564A demonstration circuit is properly connected to the DC1371, PScope should automatically detect the DC1564A, and configure itself accordingly.

If everything is hooked up properly, powered, and a suitable convert clock is present, clicking the Collect button will result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC1371 Quick Start Guide and in the online help available within the PScope program itself.

QUICK START PROCEDURE

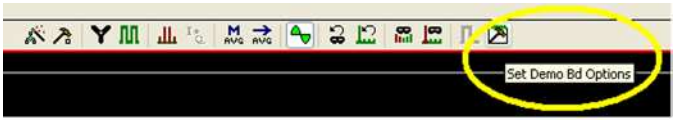


Figure 2. PScope Toolbar

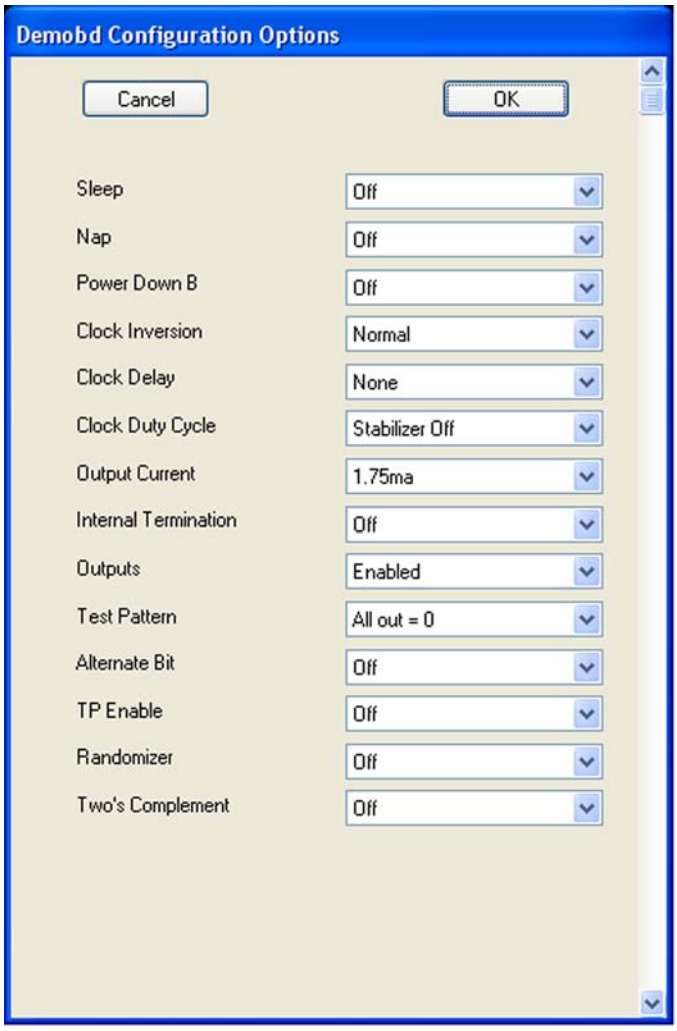


Figure 3. Demobd Configuration Options

Serial Programming

PScope has the ability to program the DC1564A board serially through the DC1371. There are several options available in the LTC2158 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the Set Demo Bd Options icon on the PScope toolbar (Figure 2).

This will bring up the menu shown in Figure 3.

This menu allows any of the options available for the LTC2158 family to be programmed serially. The LTC2158 family has the following options:

Sleep Mode – Selects between normal operation, sleep mode:

- Off (Default) – Entire ADC is powered and active
- On – The entire ADC is powered down

NAP – Selects between normal operation and nap mode.

- Off (Default) – Channel one is active
- On – Channel one is in nap mode

Power Down B – Selects between normal operation and putting channel B in nap mode.

- Off (Default) – Channel two is active
- On – Channel two is in nap mode

Clock Inversion – Selects the polarity of the CLKOUT signal:

- Normal (Default) – Normal CLKOUT polarity
- Inverted – CLKOUT polarity is inverted

Clock Delay – Selects the phase delay of the CLKOUT signal:

- None (Default) – No CLKOUT delay
- 45 deg – CLKOUT delayed by 45 degrees
- 90 deg – CLKOUT delayed by 90 degrees
- 135 deg – CLKOUT delayed by 135 degrees

Clock Duty Cycle – Enable or disables duty cycle stabilizer.

- Stabilizer off (Default) – Duty cycle stabilizer disabled
- Stabilizer on – Duty cycle stabilizer enabled

QUICK START PROCEDURE

Output Current – Selects the LVDS output drive current.

- 1.75mA (Default) – LVDS output driver current
- 2.1mA – LVDS output driver current
- 2.5mA – LVDS output driver current
- 3.0mA – LVDS output driver current
- 3.5mA – LVDS output driver current
- 4.0mA – LVDS output driver current
- 4.5mA – LVDS output driver current

Internal Termination – Enables LVDS internal termination.

- Off (Default) – Disables internal termination
- On – Enables internal termination

Outputs – Enables digital outputs

- Enabled (Default) – Enables digital outputs
- Disabled – Disables digital outputs

Test Pattern – Selects digital output test patterns.

- All out = 0 (default) – All digital outputs are 0
- All out = 1 – All digital outputs are 1
- Checkerboard – OF, and D13-D0 Alternate between 101 0101 1010 0101 and 010 1010 0101 1010 on alternating samples.
- Alternating – Digital outputs alternate between all 1's and all 0's on alternating samples

Alternate Bit – Alternate bit polarity mode.

- Off (Default) – Disables alternate bit polarity
- On – Enables alternate bit polarity (Before enabling ABP, be sure the part is in offset binary mode)

TP Enable – Selects Digital output test patterns. The desired test pattern can be entered into the text boxes provided.

- Off (default) – ADC input data is displayed
- On – Test pattern is displayed

Randomizer – Enables data output randomizer.

- Off (Default) – Disables data output randomizer
- On – Enables data output randomizer

Two's Complement – Enables two's complement mode.

- Off (Default) – Selects offset binary mode
- On – Selects two's complement mode

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1564 demo board.

PARTS LIST

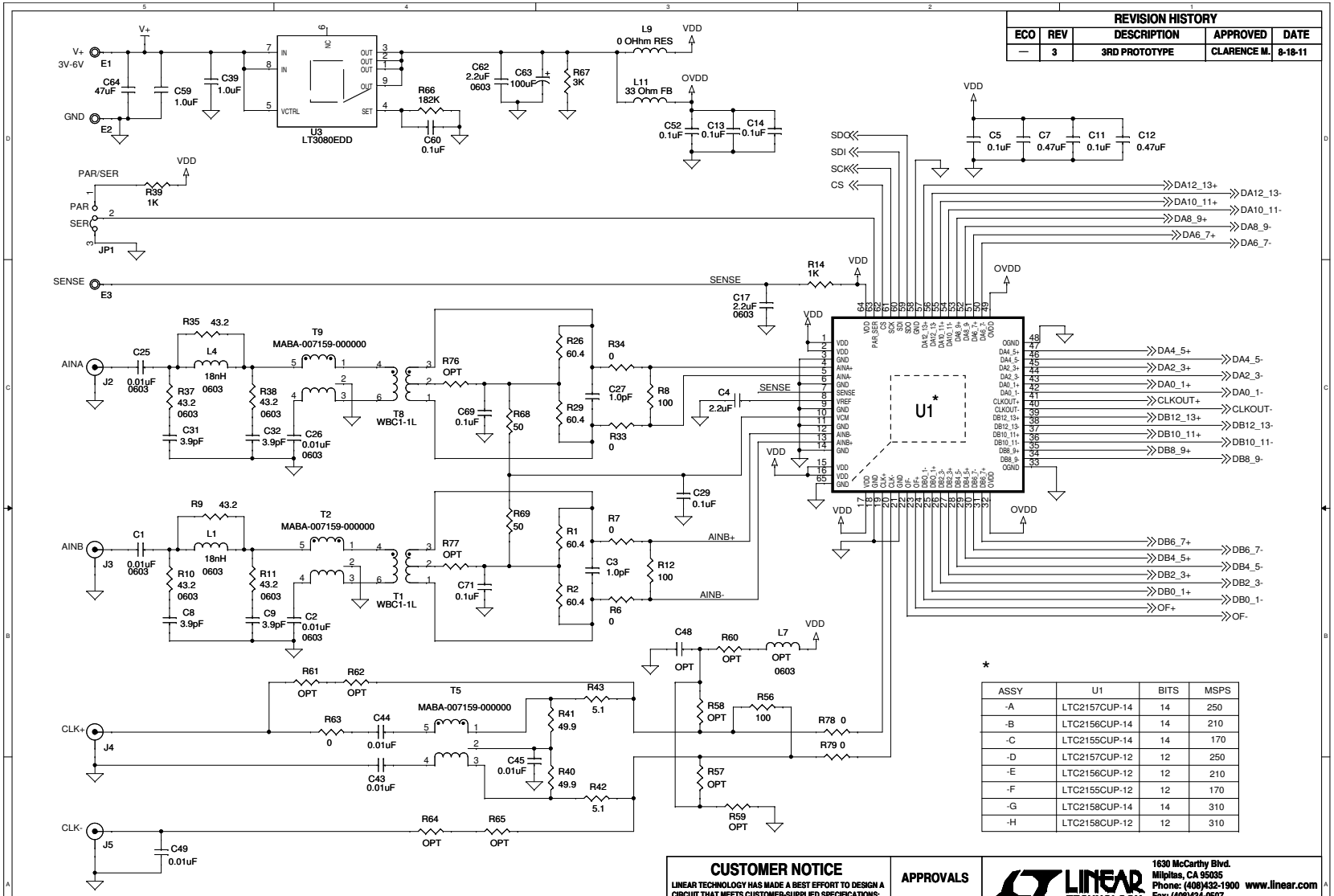
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
LTC215XCUPX Family				
1	4	C1, C2, C25, C26	CAP., X7R, 0.01µF, 50V, 10% 0603	AVX, 06035C103KAQ2A
2	2	C3, C27	CAP., C0G, 1pF, 50V, 5% 0402	AVX, 04025A1R0JAT2A
3	11	C4, C5, C7, C11, C12, C13, C14, C29, C52, C69, C71	CAP., X5R, 0.1µF, 10V, 10% 0402	AVX, 0402ZD104KAQ2A
4	4	C8, C9, C31, C32	CAP., C0G, 3.9pF, 50V, 5% 0402	AVX, 04025A3R9JAT2A
5	2	C17, C62	CAP., X5R, 2.2µF, 10V, 20% 0603	AVX, 0603ZD225MAT2A
6	3	C39, C59, C60	CAP., X5R, 1µF, 10V, 10% 0402	AVX, 0402ZD105KAT2A
7	4	C43, C44, C45, C49	CAP., X7R, 0.01µF, 16V, 10% 0402	AVX, 0402YC103KAQ2A
8	11	C48, R57, R58, R59, R60, R61, R62, R64, R65, R76, R77	OPT	402
9	1	C63	CAP., TANT, 100µF, 10% 6032	AVX, TAJW107K010R
10	1	C64	CAP., X7R, 47µF, 10V, 10%, 1210	MURATA, GRM32ER71A476KE15L
11	4	C65, C66, C67, C68	CAP., C0G, 47pF, 16V, 10% 0402	AVX, 0402YA470KA
12	3	E1, E2, E3	TESTPOINT, TURRET, 0.094"	MILL-MAX, 2501-2-00-80-00-00-07-0
13	1	JP1	3-PIN 0.079" SINGLE ROW HEADER	SAMTEC, TMM103-02-L-S
14	1	JP2	HEADER, 2-PIN 0.079" SINGLE ROW	SAMTEC, TMM-102-02-L-S
15			SHUNT, 0.079" CENTER	SAMTEC, 2SN-BK-G
16	1	J1	BGA CONNECTOR, 40x10	SAMTEC, SEAM-40-02.0-S-10-2-A
17	1	J1	UNUSED	CON-SEAM-10X40PIN
18	2	J2, J3	CON., SMA 50Ω EDGE-LANCH	E.F.JOHNSON, 142-0701-851
19	2	J4, J5	CON., SMA 50Ω STRAIGHT MOUNT	CONNEX., 132134
20	2	L1, L4	INDUCTOR, 18nH 0603	MURATA, LQP18MN18NG02D
21	1	L7	OPT, 0603	
22	2	L9, L11	FERRITE BEAD, 1206	MURATA, BLM31PG330SN1L
23	4	R1, R2, R26, R29	RES., CHIP, 33.2Ω, 1/16W, 1% 0402	VISHAY, CRCW040233R2FKED
24	4	R6, R7, R33, R34	RES., CHIP, 10Ω, 1/16W, 5% 0402	VISHAY, CRCW040210R0JNED
25	3	R8, R12, R56	RES., CHIP, 100Ω, 1/16W, 5% 0402	VISHAY, CRCW0402100RJNED
26	2	R9, R35	RES., CHIP, 43.2Ω, 1/16W, 1% 0402	VISHAY, CRCW040243R2FKED
27	4	R10, R11, R37, R38	RES., CHIP, 43.2Ω, 1/16W, 1% 0603	VISHAY, CRCW060343R2FNEA
28	6	R14, R39, R72, R73, R74, R75	RES., CHIP, 1k 1/16W, 1% 0402	VISHAY, CRCW04021K00FKED
29	3	R36, R44, R45	RES., CHIP, 5.1k 1/16W, 1%, 0402	VISHAY,CRCW04025K10FKED
30	2	R40, R41	RES., CHIP, 49.9Ω, 1/16W, 1% 0402	VISHAY, CRCW040249R9FKED
31	2	R42, R43	RES., CHIP, 5.1Ω, 1/16W, 5% 0402	VISHAY, CRCW04025R10JNED
32	3	R63, R78, R79	RES., CHIP, 0Ω, 1/16W, 0402	VISHAY, CRCW04020000Z0ED
33	1	R66	RES., CHIP, 182k, 1/16W, 1% 0402	VISHAY, CRCW0402182KFKED
34	1	R67	RES., CHIP, 3.01k 1/16W, 1%, 0402	VISHAY,CRCW04023K010FKED
35	2	R68, R69	RES., CHIP, 49.9Ω, 1/16W, 5% 0402	VISHAY, CRCW040249R9JNED
36	2	T1, T8	TRANSFORMER, WBC1-1L	COILCRAFT, WBC1-1L
37	3	T2, T5, T9	TRANSFORMER, MABA-007159-000000	M/A-COM, MABA-007159-000000
38	1	U3	I.C. LT3080EDD, DFN 3X3	LINEAR TECH., LT3080EDD
39	1	U6	I.C., Serial EEPROM TSSOP-8	MICROCHIP, 24LC32A-I/ST
40	4	(STAND-OFF)	STAND-OFF, NYLON 0.25"	KEYSTONE, 8831(SNAP ON)

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
LTC2157CUP-14/DC1564A-A				
1	1	DC1564A	GENERAL BOM	
2	1	U1	I.C. LTC2157CUP-14, 64-PIN QFN-9X9	LINEAR, LTC2157CUP-14
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1564A
LTC2156CUP-14/DC1564A-B				
1	1	DC1564A	GENERAL BOM	
2	1	U1	I.C. LTC2156CUP-14, 64-PIN QFN-9X9	LINEAR, LTC2156CUP-14
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1564A
LTC2155CUP-14/DC1564A-C				
1	1	DC1564A	GENERAL BOM	
2	1	U1	I.C. LTC2155CUP-14, 64-PIN QFN-9X9	LINEAR, LTC2155CUP-14
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1564A
LTC2157CUP-12/DC1564A-D				
1	1	DC1564A	GENERAL BOM	
2	1	U1	I.C. LTC2157CUP-12, 64-PIN QFN-9X9	LINEAR, LTC2157CUP-12
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1564A
LTC2156CUP-12/DC1564A-E				
1	1	DC1564A	GENERAL BOM	
2	1	U1	I.C. LTC2156CUP-12, 64-PIN QFN-9X9	LINEAR, LTC2156CUP-12
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1564A
LTC2155CUP-12/DC1564A-F				
1	1	DC1564A	GENERAL BOM	
2	1	U1	I.C. LTC2155CUP-12, 64-PIN QFN-9X9	LINEAR, LTC2157CUP-12
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1564A
LTC2158CUP-14/DC1564A-G				
1	1	DC1564A-A	GENERAL BOM	
2	1	U1	I.C. LTC2158CUP-14, 64-PIN QFN-9X9	LINEAR, LTC2158CUP-14
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1564A
LTC2158CUP-12/DC1564A-H				
1	1	DC1564A-A	GENERAL BOM	
2	1	U1	I.C. LTC2158CUP-12, 64-PIN QFN-9X9	LINEAR, LTC2158CUP-12
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1564A

DEMO MANUAL DC1564A

SCHEMATIC DIAGRAM



*

ASSY	U1	BITS	MSPS
-A	LTC2157CUP-14	14	250
-B	LTC2156CUP-14	14	210
-C	LTC2155CUP-14	14	170
-D	LTC2157CUP-12	12	250
-E	LTC2156CUP-12	12	210
-F	LTC2155CUP-12	12	170
-G	LTC2158CUP-14	14	310
-H	LTC2158CUP-12	12	310

NOTE: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN 0402
   ALL CAPACITORS ARE IN 0402

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APPROVALS

PCB DES.	AK
APP ENG.	CLARENCE M.

SCALE = NONE

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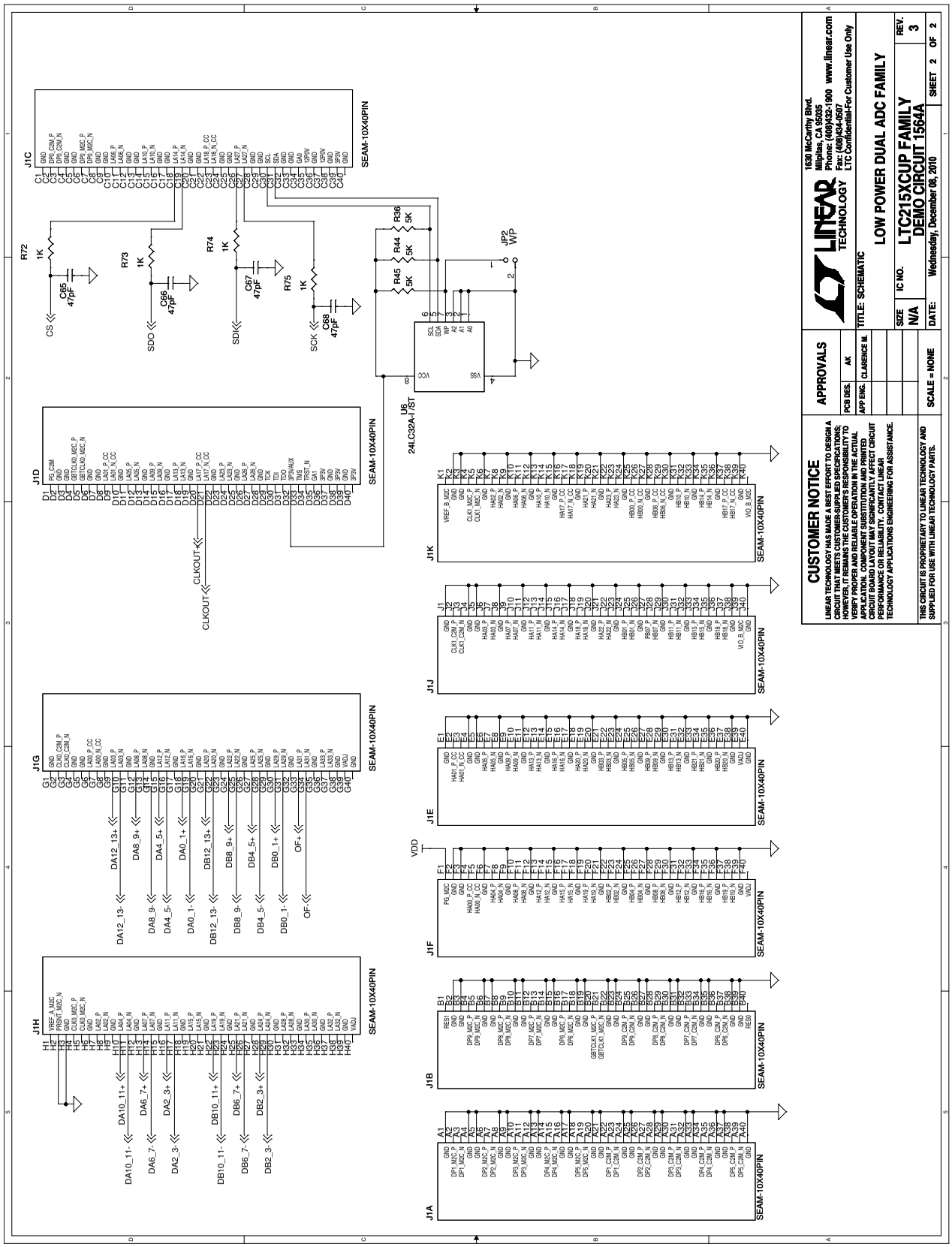
TITLE: SCHEMATIC

LOW POWER DUAL ADC FAMILY

SIZE	IC NO.		REV.
N/A		LTC215XCUP FAMILY DEMO CIRCUIT 1564A	3
DATE:	Thursday, August 18, 2011		SHEET 1 OF 2

SCHEMATIC DIAGRAM



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