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LTC2383-16/LTC2382-16/ LTC2381-16: 16-Bit, 1.0Msps/ 0.5Msps/0.25Msps Low Power, Low Noise ADCs

DESCRIPTION

The LTC®2383-16/LTC2382-16/LTC2381-16 are low power, low noise ADCs with serial outputs that can operate from a single 2.5V supply. The following text refers to the LTC2383-16 but applies to all three parts. The only difference being the maximum sample rates. The LTC2383-16 supports a ±2.5V fully differential input range with a 92dB SNR, consumes only 13mW and achieves ±2LSB INL max with no missing codes at 16-bits. The DC1571A demonstrates the DC and AC performance of the LTC2383-16 in conjunction with the DC590 QuickEval and DC718 Fast DAACS data collection boards. Use the DC590 to demonstrate DC performance such as peak-to-peak noise and DC linearity. Use the DC718 if precise sampling rates are required or to demonstrate AC performance such as SNR, THD, SINAD and SFDR. The demonstration circuit DC1571A is intended to demonstrate recommended grounding, component placement and selection, routing and bypassing for this ADC. Several suggested driver circuits for the analog inputs will also be presented.

Design files for this circuit board are available at http://www.linear.com/demo

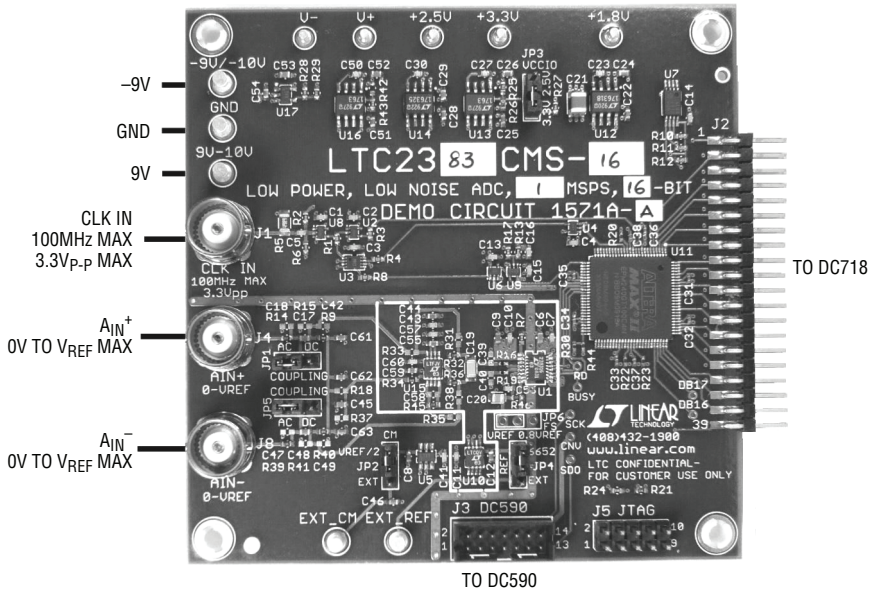

Figure 1. DC1571A Connection Diagram

Table 1. DC1571A Assembly Options

ASSEMBLY VERSION	U1 PART NUMBER	MAX CONVERSION RATE	MAX CLK IN FREQUENCY
DC1571A-A	LTC2383CMS-16	1Msps	80MHz
DC1571A-B	LTC2382CMS-16	0.5Msps	40MHz
DC1571A-C	LTC2381CMS-16	0.25Msps	20MHz

DC718 QUICK START PROCEDURE

Check to make sure that all switches and jumpers are set as shown in the connection diagram of Figure 1. The default connections configure the ADC to use the onboard reference and common mode voltages. The analog input is AC coupled. Connect the DC1571A to a DC718 USB High Speed Data Collection Board using connector J2. Connect the DC718 to a host PC with a standard USB A/B cable. Apply ±9V to the indicated terminals. Apply a low jitter signal source to J4. The default setup uses a single ended to differential converter so that it is only necessary to apply an input signal to J4. Connect a low jitter 80MHz 3.3Vpp sine wave or square wave to connector J1. Note that J1 has a 50Ω termination resistor to ground.

Run the QuickEval-II software (Pscope.exe version K68 or later) supplied with the DC718 or download it from www.linear.com.

Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

The Pscope software should recognize the DC1571A and configure itself automatically.

Click the Collect button (See Figure 6) to begin acquiring data. The Collect button then changes to Pause, which can be clicked to stop data acquisition.

DC590 SETUP

To use the DC590 with the DC1571A it is necessary to apply –9V and ground to the –9V and GND terminals or disable amplifier U15 by moving R32 and R36 to R31 and R38 respectively. If U15 is disabled, it is required that J4 and J8 are both driven. If U15 is not disabled then it is only necessary to drive J4. Connect the DC590 to a host PC with a standard USB A/B cable. Connect the DC1571A to a DC590 USB serial controller using the supplied 14-conductor ribbon cable. Apply a signal source to J4 or J4 and J8 depending on how the DC1571A is configured.

Run the evaluation software supplied with the DC590 or download it from www.linear.com. The correct control panel will be loaded automatically. Click the COLLECT button (Figure 7) to begin reading the ADC.

DC1571A SETUP

DC Power

The DC1571A requires ±9V_{DC} at approximately 100mA. Most of the supply current is consumed by the CPLD, op amps, regulators and discrete logic on the board. The ±9V_{DC} input voltage powers the ADC through LT®1763 regulators which provide protection against accidental reverse bias. Additional regulators provide power for the CPLD and op amps. See Figure 1 for connection details.

Clock Source

You must provide a low jitter 3.3V_{P-P} sine or square wave to J1. The clock input is AC coupled so the DC level of the clock signal is not important. A generator like the HP8644 or similar is recommended. Even a good generator can start to produce noticeable jitter at low frequencies. Therefore it is recommended for lower sample rates to divide down a higher frequency clock to the desired sample rate. The ratio of clock frequency to conversion rate is 80:1. If the clock input is to be driven with logic, it is recommended that the 50Ω terminator (R5) be removed. Slow rising edges may compromise the SNR of the converter in the presence of high amplitude higher frequency input signals.

Data Output

Parallel data output from this board (0V to 3.3V default), if not connected to the DC718, can be acquired by a logic analyzer, and subsequently imported into a spreadsheet, or mathematical package depending on what form of digital signal processing is desired. Alternatively, the data can be fed directly into an application circuit. Use Pin 3 of J2 to

DC1571A SETUP

latch the data. The data can be latched using either edge of this signal. The data output signal levels at J2 can also be reduced to 0V to 2.5V if the application circuit cannot tolerate the higher voltage. This is accomplished by moving JP3 to the 2.5V position.

Reference

JP4 selects between an on-board LTC6652 2.5V reference and an external reference. If an external reference is used it must settle quickly in the presence of glitches on the REF pin.

Analog Input

The default driver for the analog inputs of the LTC2383-16 on the DC1571A is shown in Figure 2. This circuit converts a single-ended 0V to 2.5V input signal applied at A_{IN}^+ into a differential signal with a swing of ±2.5V between the +IN and –IN inputs of the ADC. In addition, this circuit band limits the input frequencies to approximately 500kHz which is the useful linear bandwidth of the LTC2383-16.

Alternatively, if your application circuit produces a differential signal which can drive the ADC but you need to level shift the input signal, the circuit of Figure 3 can be used. The circuit of Figure 3 AC couples the input signal and is usable down to about 10kHz. The lower frequency limit can be extended by increasing C17 and C48. The circuit of Figure 3 can be implemented on the DC1571A by putting JP1 and JP5 in the AC position and moving R32 and R36 to the R31 and R38 positions. At this point it will be necessary to drive both A_{IN}^+ and A_{IN}^-. One of these RC pairs can be attached to the input of the circuit in Figure 2. This allows a single-ended input signal to be level shifted. This is the default condition for the DC1571A. One of the most asked for ADC driver circuits is one that allows the input voltage to go below ground with a single supply ADC. Figure 4's input driver allows an input voltage range of ±10V. The circuit of Figure 4 can be implemented on the DC1571A by replacing R9 and R45 with 2k, R15 and R39 with 16k and putting JP5 in the DC position.

Data Collection

For SINAD, THD or SNR testing, a low noise, low distortion generator such as the B & K Type 1051 or Stanford Research DS360 should be used. A low jitter RF oscillator such as the HP8644 is used as the clock source.

This demo board is tested in house by attempting to duplicate the FFT plot shown on the front page of the LTC2383-16 data sheet. This involves using a 80MHz clock source, along with a sinusoidal generator at a frequency of 20kHz. The input signal level is approximately –1dBfs. The input is filtered with a 20kHz single-pole RC filter shown in Figure 5. The FFT shown in the data sheet is a 32k point FFT. A typical FFT obtained with DC1571A is shown in Figure 6.

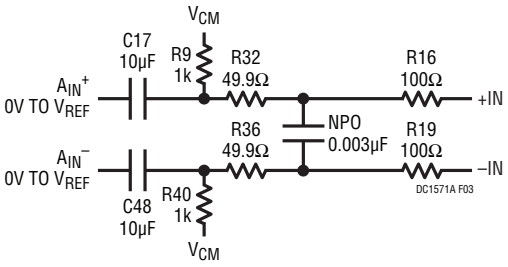

Figure 3. AC-Coupled Differential Driver

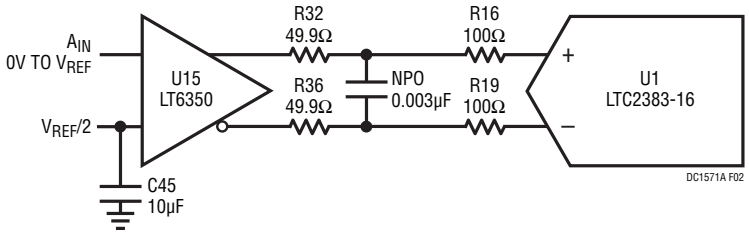

Figure 2. Single Ended to Differential Converter

DC1571A SETUP

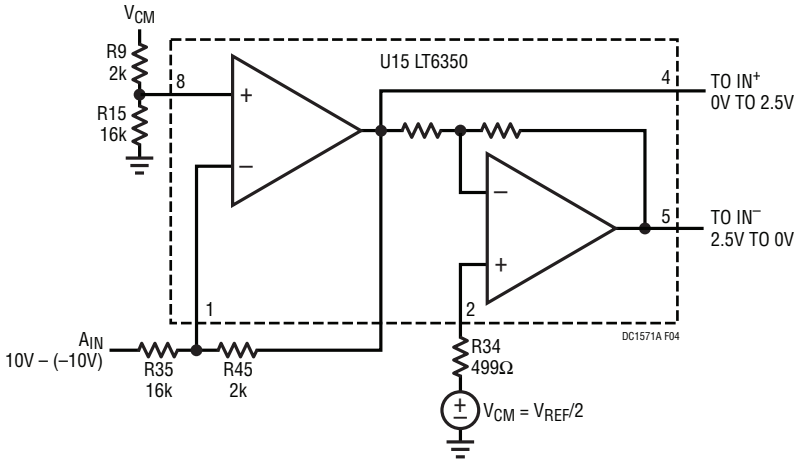

Figure 4. DC Coupled Single-Ended to Differential Driver

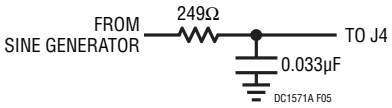

Figure 5. 20kHz RC Filter

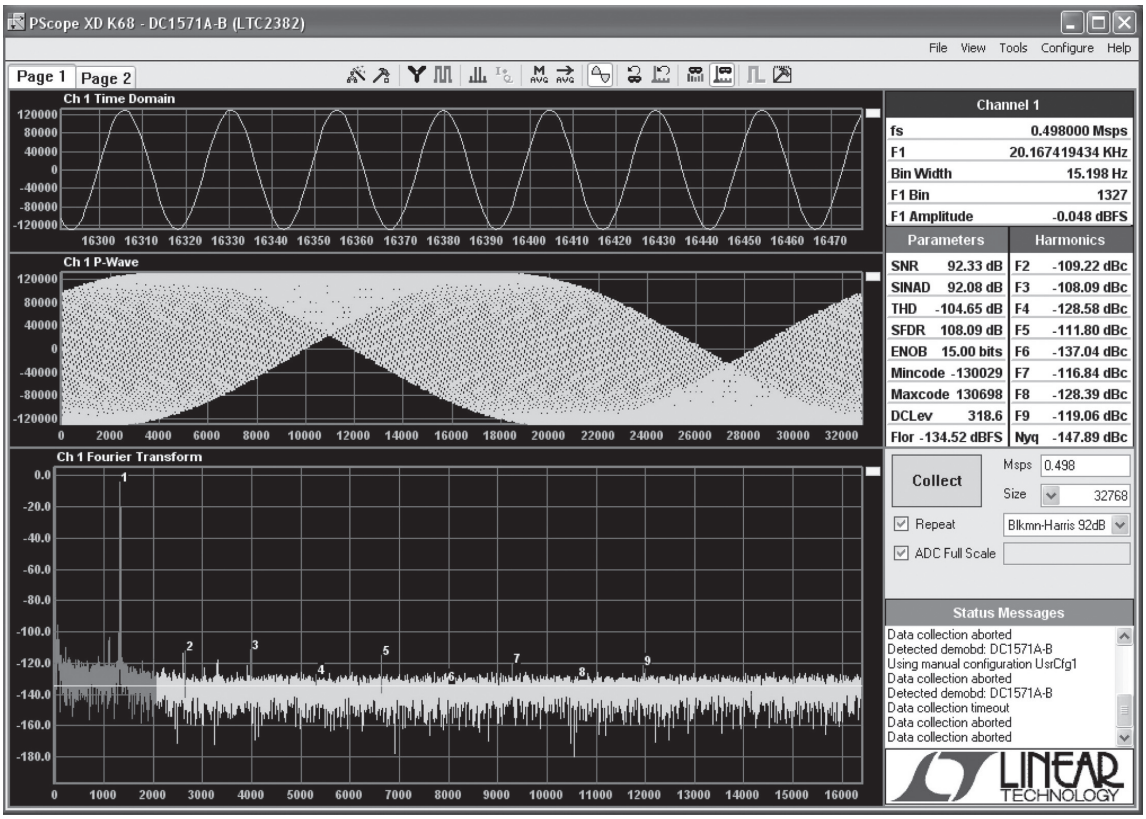

Figure 6. Pscope Screen Shot

DC1571A SETUP

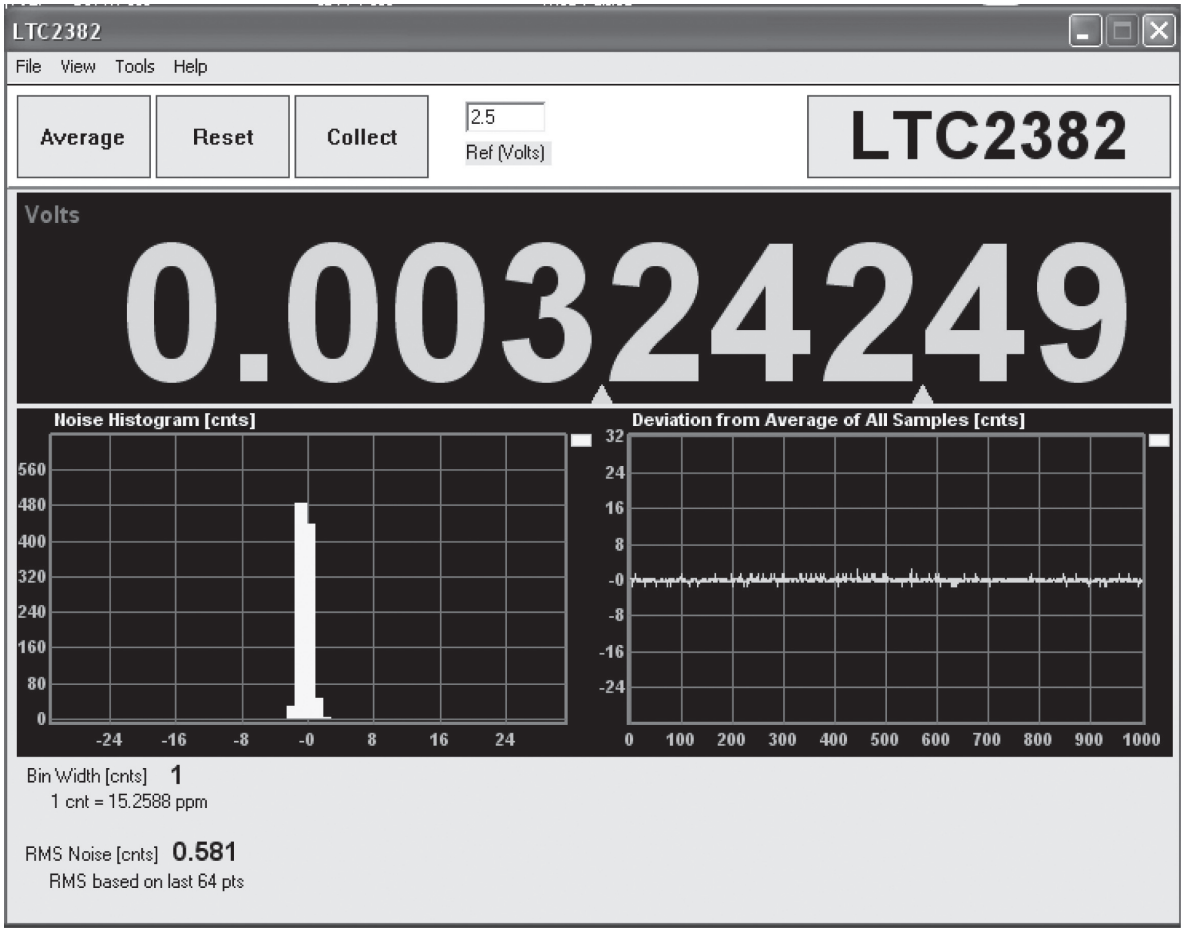

Figure 7. QuikEval Screen Shot

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that is common is feeding the converter with a frequency, that is a sub-multiple of the sample rate, which will only exercise a small subset of the possible output codes. The proper method is to pick an M/N frequency for the input sine wave frequency. N is the number of samples in the FFT. M is a prime number between one and N/2. Multiply M/N by the sample rate to obtain the input sine wave frequency. Another scenario that can yield poor results is if you do not have a signal generator capable of ppm frequency accuracy or if it cannot be locked to the clock frequency. You can use an FFT with windowing to reduce the "leakage" or spreading of the fundamental, to get a close approximation of the ADC performance. If an amplifier or clock source with poor phase noise is used, the windowing will not improve the SNR.

Layout

As with any high performance ADC, this part is sensitive to layout. The area immediately surrounding the ADC on the DC1571A should be used as a guideline for placement, and routing of the various components associated with the ADC. Here are some things to remember when laying out a board for the LTC2383-16. A ground plane is necessary to obtain maximum performance. Keep bypass capacitors as close to supply pins as possible. Use individual low impedance returns for all bypass capacitors. Use of a symmetrical layout around the analog inputs will minimize the effects of parasitic elements. Shield analog input traces with ground to minimize coupling from other traces. Keep traces as short as possible.

DC1571A SETUP

Component Selection

When driving a low noise, low distortion ADC such as the LTC2383-16, component selection is important so as to not degrade performance. Resistors should have low values to minimize noise and distortion. Metal film resistors are recommended to reduce distortion caused by self heating. Because of their low voltage coefficients, to further reduce distortion. NPO or silver mica capacitors should be used. Any buffer used to drive the LTC2383-16 should have low distortion, low noise and a fast settling time such as the LT6350.

DC1571A JUMPERS

Definitions

JP1: Selects AC or DC coupling of A_{IN}^+. The default setting is AC.

JP2: V_{CM} sets the DC bias for A_{IN}^+ and A_{IN}^- when the inputs are AC coupled. $V_{REF}/2$ is the default setting.

JP3: V_{CCIO} sets the output levels at J2 to either 3.3V or 2.5V. Use 3.3V to interface to DC718 which is the default setting.

JP4: Ref selects between the LTC6652 2.5V reference and an external reference. LTC6652 is the default setting.

JP5: Selects AC or DC coupling of A_{IN}^-. The default setting is AC.

PARTS LIST

LTC23XXCMS Family

ITEM	QTY	REFERENCE-DESCRIPTION	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	16	C1-C5, C7, C10, C11, C13-C16, C43, C56, C57, C60	CAP., X5R, 0.1µF, 16V,10%	AVX, 0603YD104KAT
2	12	C6, C9, C17, C24, C26, C29, C45, C48, C52, C53, C61, C63	CAP., X5R, 10µF 6.3V,20%,0603	TDK, C1608X5R0J106MT
3	12	C8, C12, C22, C25, C28, C44, C46, C51, C54, C55, C59, C62	CAP., X7R, 1µF 16V,10%,0603	TDK, C1608X7R1C105K
4	0	C18, C39, C40, C41, C47, C49, C58	CAP., 0603	OPT
5	1	C19	CAP., C0G, 3300pF, 50V, 10%, 1206	AVX, 12065A332KAT2A
6	1	C20	CAP., X5R, 47µF 6.3V,20%,0805	TAIYO YUDEN, JMK212BJ476MG-T
7	1	C21	CAP., X5R, 22µF 16V,20%,1210	TAIYO YUDEN, EMK325BJ226MM-T
8	4	C23, C27, C30, C50	CAP., X7R, 0.01µF, 16V,10%	AVX, 0603YC103KAT
9	8	C31-C38	CAP., X7R, 0.1µF, 16V,10%	TDK, C1005X7R1C104KT
10	1	C42	CAP., C0G, 15pF, 50V, 10%, 0603	AVX, 06035A150KAT2A
11	5	E1, E4, E6, E7, E10	TP, TURRET, 0.094"	MILL-MAX, 2501-2-00-80-00-00-07-0
12	5	E2, E3, E5, E8, E9	TP, TURRET, 0.064"	MILL-MAX, 2308-2-00-80-00-00-07-0
13	3	J1, J4, J8	CONN., BNC-5PINS	CONNEX, 112404
14	1	J2	CONN., 40PINS SMT, CON-EDGE40-100	SAMTEC, TSW-120-07-L-D
15	1	J3	HEADER, 2X7, 0.079"	MOLEX, 87831-1420
16	1	J5	HEADER, 2X5, 0.100", HD2X5-100	SAMTEC, TSW-105-07-L-D
17	5	JP1-JP5	JMP., 1X3, 0.100", HD1X3-100	SAMTEC, TSW-103-07-L-S
18	0	JP6	JMP., 1X3, 0.100", HD1X3-100	OPT
19	4	R1,R3,R4,R8	RES., CHIP 33, 1%, 0603	NIC, NRC06F33R0TRF
20	9	R2, R6, R7, R9, R13, R24, R29, R40, R43	RES., CHIP 1k, 1%, 0603	NIC, NRC06F1001TRF
21	1	R5	RES., CHIP 49.9, 1%, 1206	NIC, NRC12F49R9TRF
22	3	R10, R11, R12	RES., CHIP 4.99k, 1%, 0603	NIC, NRC06F4991TRF
23	6	R14, R33, R34, R39, R45, R46	RES., CHIP 0, 1%, 0603	NIC, NRC06F0000TRF
24	3	R15, R18, R37	RES., CHIP 1k, 1%, 0603	NIC, NRC06F1001TRF
25	2	R16, R19	RES., CHIP 100Ω, 1%, 0402	NIC, NRC04F100RTRF
26	2	R17, R28	RES., CHIP 2k, 1%, 0603	NIC, NRC06F2001TRF
27	3	R20, R22, R23	RES., CHIP 1k, 1%, 0402	NIC, NRC04F1001TRF
28	1	R21	RES., CHIP 10k, 1%, 0603	NIC, NRC06F1002TRF
29	1	R25	RES., CHIP 1.69k, 1%, 0603	NIC, NRC06F1691TRF
30	1	R26	RES., CHIP 1.54k, 1%, 0603	NIC, NRC06F1541TRF
31	1	R27	RES., CHIP 2.80k, 1%, 0603	NIC, NRC06F2801TRF
32	1	R30	RES., CHIP 10k, 1%, 0402	NIC, NRC04F1002TRF
33	0	R31, R35, R38, R41	RES., 0603	OPT
34	2	R32, R36	RES., CHIP 49.9Ω, 1%, 0603	NIC, NRC06F49R9TRF
35	1	R42	RES., CHIP 5.62k, 1%, 0603	NIC, NRC06F5621TRF
36	0	R44	RES., CHIP 300Ω, 1%, 0402	OPT
37	2	U2,U4	IC, TINYLOGIC ULP-A UNBUFFERED INVERTER,SC70-5	FAIRCHILD, NC7SVU04P5X
38	1	U3	IC, SINGLE D FLIP FLOP, US8	ON SEMI., NL17SZ74
39	0	U5	IC., LT1790ACS6-1.25, SOT23-6	OPT

PARTS LIST

LTC23XXCMS Family

ITEM	QTY	REFERENCE-DESCRIPTION	PART DESCRIPTION	MANUFACTURER/PART NUMBER
40	1	U6	IC, SINGLE SPST BUS SWITCH, SC70-5	FAIRCHILD, NC7SZ66P5X
41	1	U7	IC, SERIAL EEPROM, TSSOP	MICROCHIP, 24LC025-I/ST
42	2	U8, U9	IC, TINYLOGIC UHS INVERTER, SC70-5	FAIRCHILD, NC7SZ04P5X
43	1	U10	IC., LTC6652AHMS8-2.5, MS8	LINEAR TECH., LTC6652AHMS8-2.5
44	1	U11	IC, MAX II FAMILY, TQFP100	ALTERA, EPM240GT100C5N
45	1	U12	IC., LT1763CS8-1.8, SO8	LINEAR TECH., LT1763CS8-1.8
46	2	U13,U16	IC., LT1763CS8, SO8	LINEAR TECH., LT1763CS8
47	1	U14	IC., LT1763CS8-2.5, SO8	LINEAR TECH., LT1763CS8-2.5
48	1	U15	IC., LT6350CMS8, MS8	LINEAR TECH., LT6350CMS8
49	1	U17	IC., LT1964ES5-SD, SOT23-5	LINEAR TECH., LT1964ES5-SD
50	4	MTG1, MTG2, MTG3, MTG4	STAND-OFF, NYLON (SNAP ON), 0.25" TALL	KEYSTONE, 8831(SNAP ON)
51	5	SHUNTS AS SHOWN ON ASSY DWG (JP1-JP5)	SHUNT, 0.100" CENTER	SAMTEC, SNT-100-BK-G
52	1	STENCIL FOR TOP SIDE		DC1571A-3
53	1	FROM JP2 PIN 1 TO E5	3" 24 GAUGE WIRE	WURTH, WE2403-5

LTC2383CMS-16

ITEM	QTY	REFERENCE-DESCRIPTION	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	1	DC1571A-3	GENERAL BOM	
2	1	U1	IC, LTC2383CMS-16, MS16	LINEAR TECH., LTC2383CMS-16

LTC2382CMS-16

ITEM	QTY	REFERENCE-DESCRIPTION	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	1	DC1571A-3	GENERAL BOM	
2	1	U1	IC, LTC2382CMS-16, MS16	LINEAR TECH., LTC2382CMS-16

LTC2381CMS-16

ITEM	QTY	REFERENCE-DESCRIPTION	PART DESCRIPTION	MANUFACTURER/PART NUMBER
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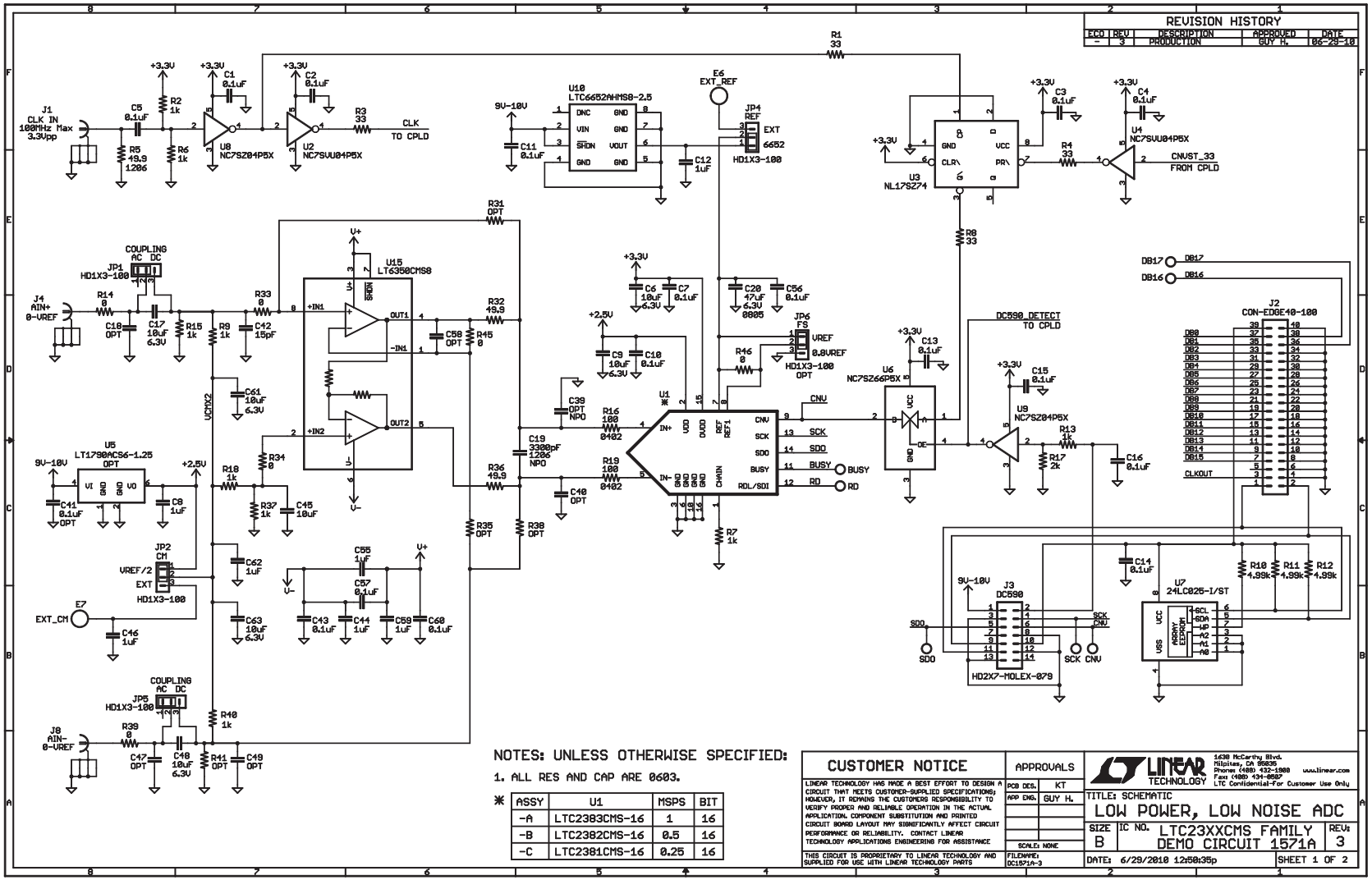
2	1	U1	IC, LTC2381CMS-16, MS16	LINEAR TECH., LTC2381CMS-16


REVISION HISTORY
ECO | REV | DESCRIPTION | APPROVED | DATE
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1. ALL RES AND CAP ARE 0603.
ASSY | U1 | MSPS | BIT
-A | LTC2383CMS-16 | 1 | 16
-B | LTC2382CMS-16 | 0.5 | 16
-C | LTC2381CMS-16 | 0.25 | 16
CUSTOMER NOTICE
APPROVALS
PCB DES. KT
APP ENG. GUY H.
LINEAR TECHNOLOGY
1630 McCarthy Blvd.
Milpitas, CA 95035
Phone (408) 432-1900 www.linear.com
Fax (408) 434-0507
LTC Confidential-For Customer Use Only
TITLE: SCHEMATIC
LOW POWER, LOW NOISE ADC
SIZE B
IC NO. LTC23XXCMS FAMILY
DEMO CIRCUIT 1571A
REV: 3
SCALE: NONE
FILENAME: DC1571A-3
DATE: 6/29/2010 12:50:35p
SHEET 1 OF 2
THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS
LINEAR TECHNOLOGY CORPORATION DOES NOT ASSUME ANY RESPONSIBILITY FOR USE OF ANY CIRCUITRY DESCRIBED, NO PATENT LICENSES ARE IMPLIED AND LINEAR TECHNOLOGY RESERVES THE RIGHT TO CHANGE CIRCUITRY AND SPECIFICATIONS AT ANY TIME WITHOUT NOTICE.
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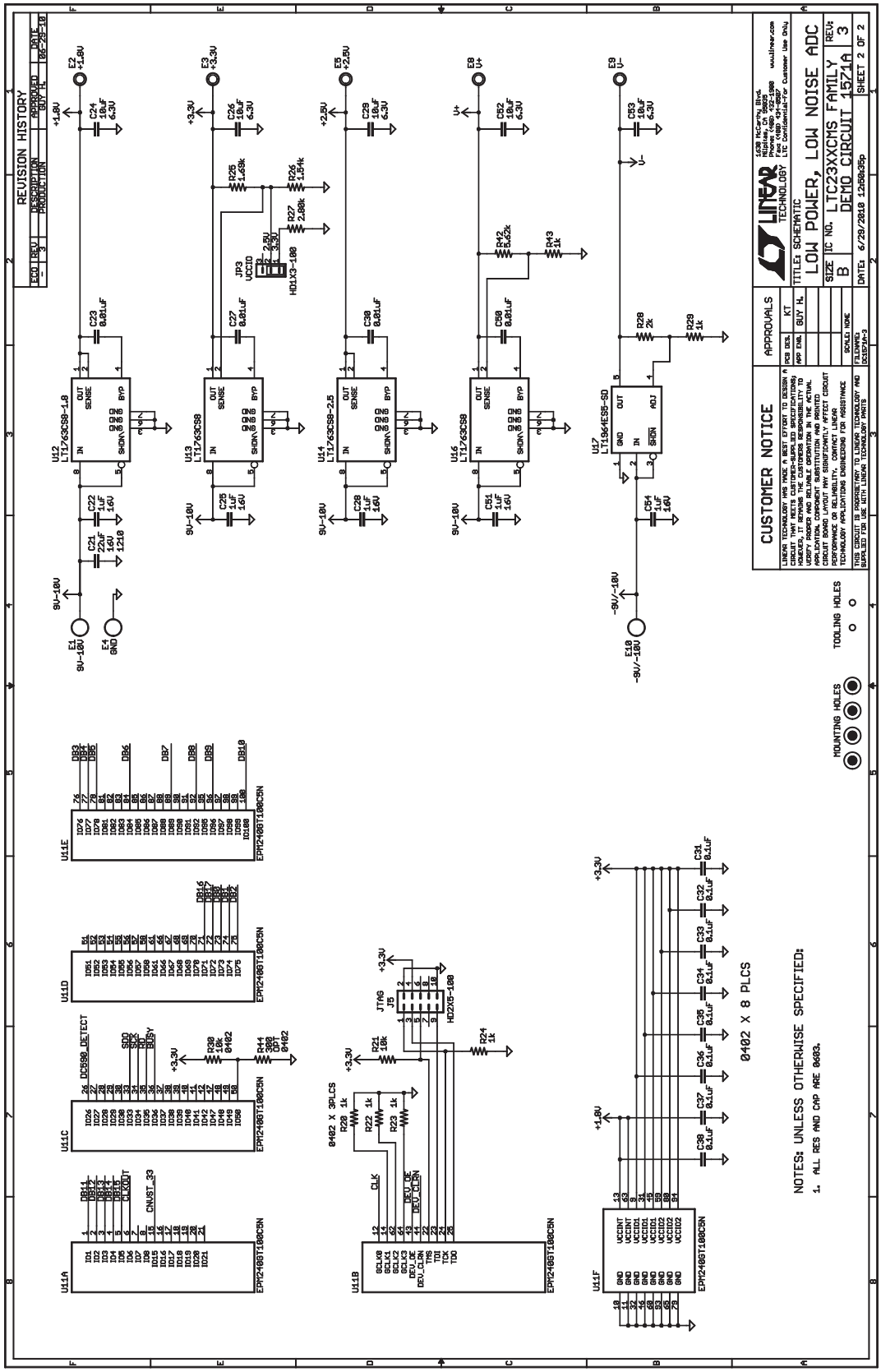
SCHEMATIC DIAGRAM



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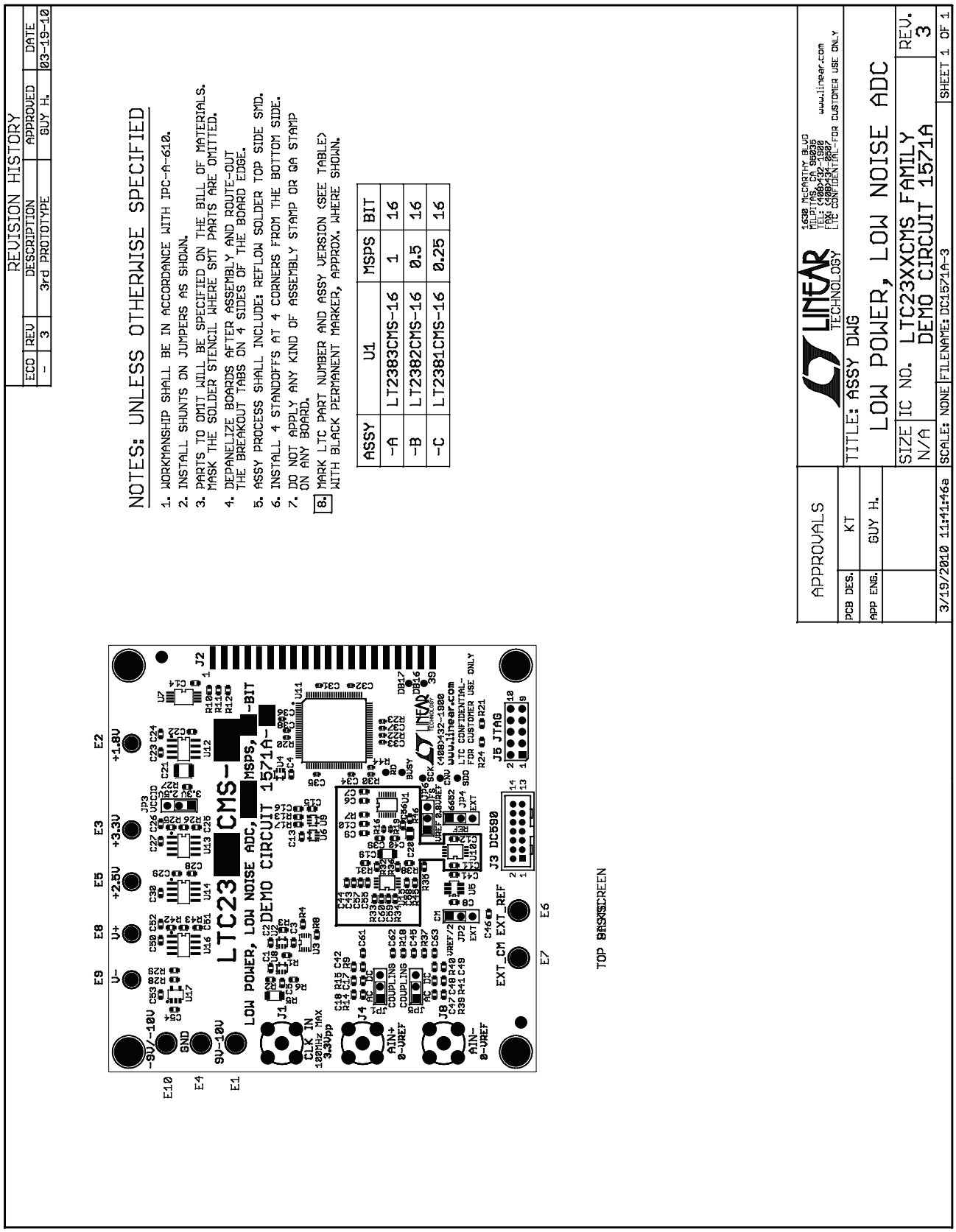

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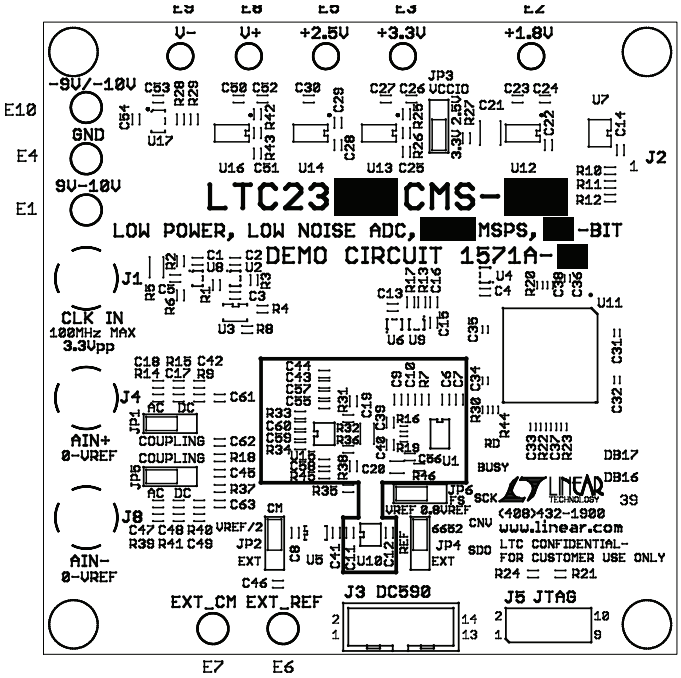

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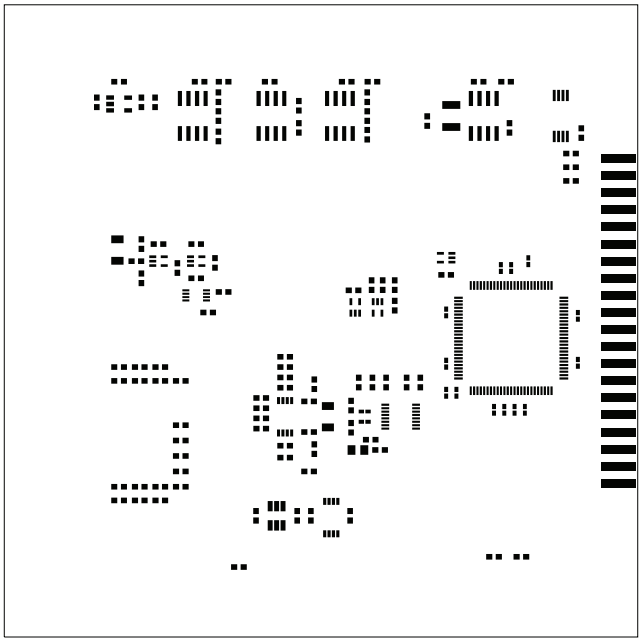

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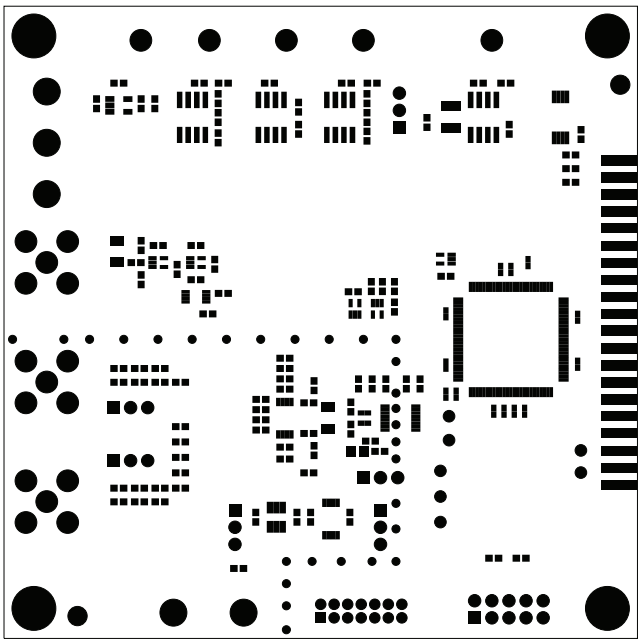

PCB LAYOUT AND FILM

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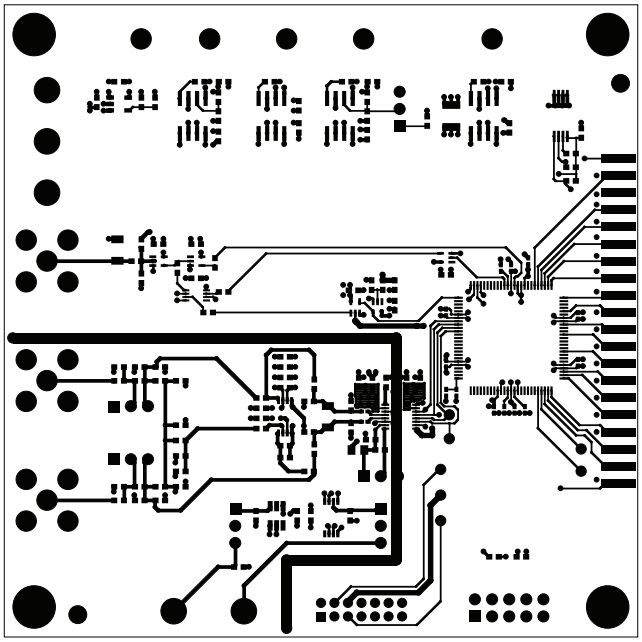

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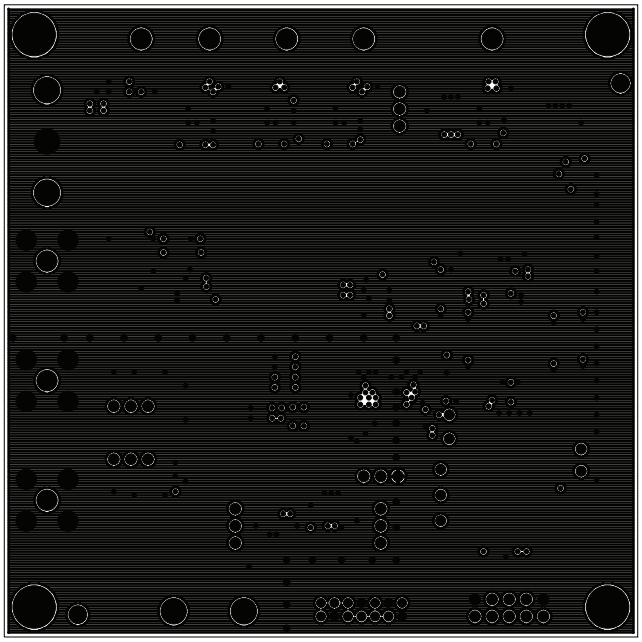
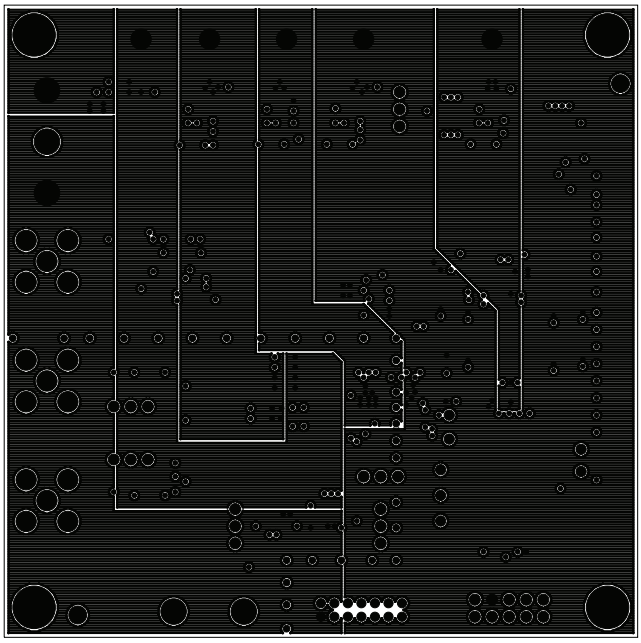
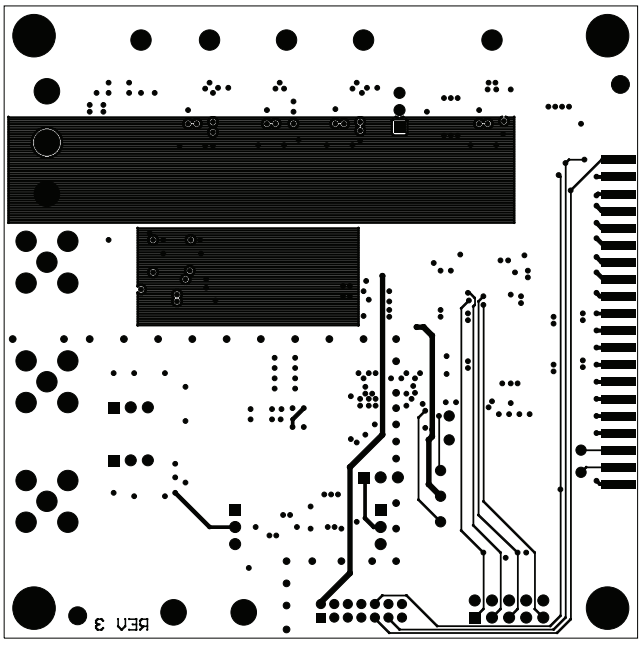


Layer 3-PWR Plane

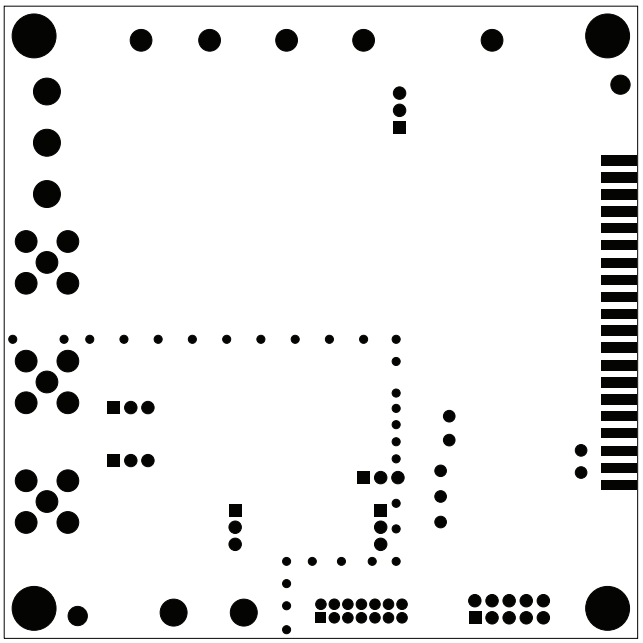


PCB LAYOUT AND FILM

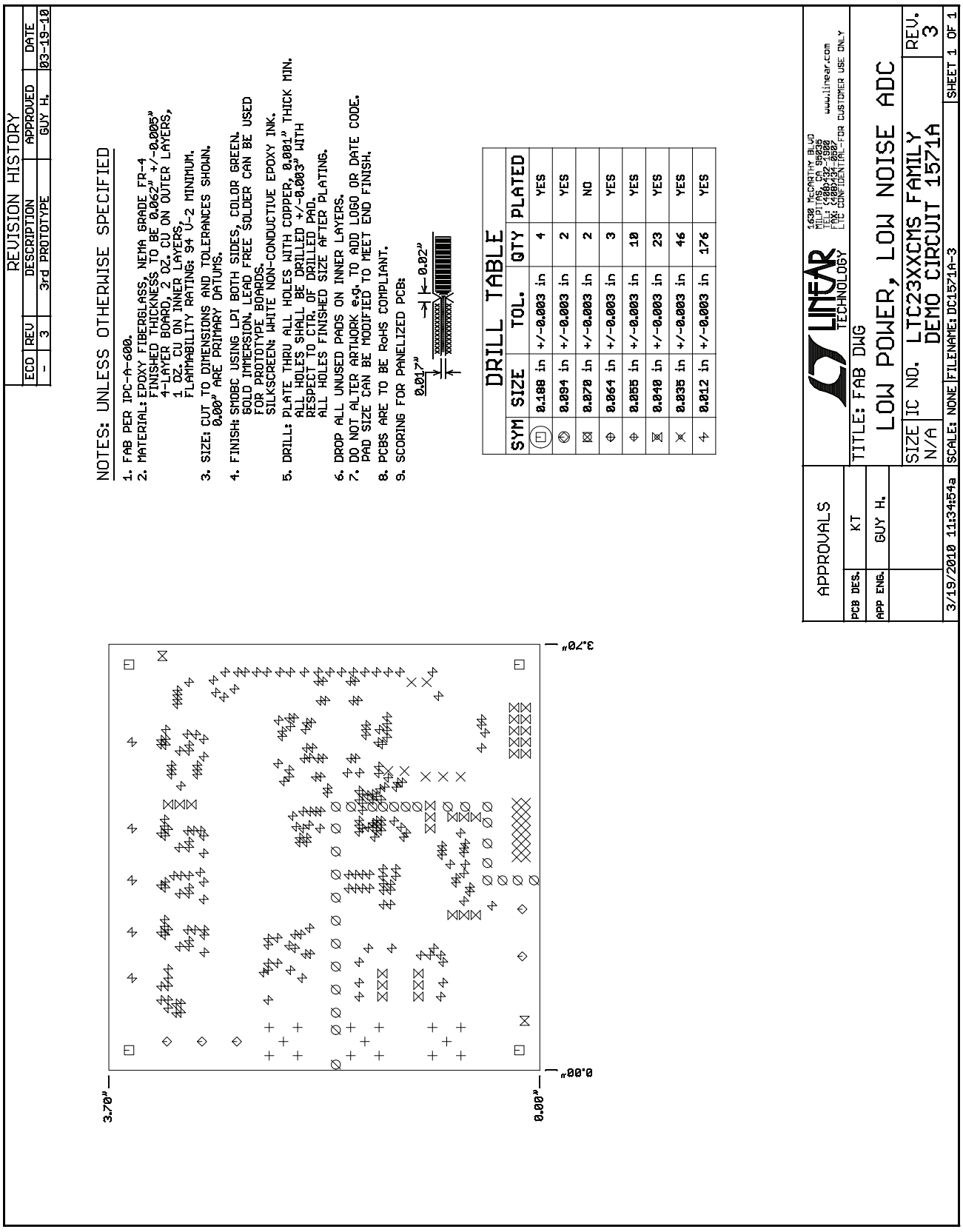
Layer 4-Bottom Layer



Bottom Mask



FAB DRAWING



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