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LTC2378-20/LTC2377-20/LTC2376-20
20-Bit, 1Msps/500ksps/250ksps, Low Power, SAR ADCs with 104dB SNR

DESCRIPTION

The LTC®2378-20, LTC2377-20 and LTC2376-20 are 20-bit, low power, low noise SAR ADCs with serial outputs that operate from a single 2.5V supply. The following text refers to the LTC2378-20 but applies to all parts in the family, the only difference being the maximum sample rate. The LTC2378-20 supports a ±5V fully differential input range with a 104dB SNR, consumes only 21mW and achieves ±2ppm INL max with no missing codes at 20 bits. The DC1925A demonstrates the DC and AC performance of the LTC2378-20 in conjunction with the DC590 QuikEval™ and DC890 PScope™ data collection boards. Use the DC590 to demonstrate DC performance such as peak-to-peak noise and DC linearity. Use the DC890 if precise sampling rates are required or to demonstrate AC performance such as SNR, THD, SINAD and SFDR. The demonstration circuit 1925A is intended to show recommended grounding, component placement and selection, routing and bypassing for this ADC.

Design files for this circuit board are available at http://www.linear.com/demo or scan the QR code on the back of the board.

BOARD PHOTO

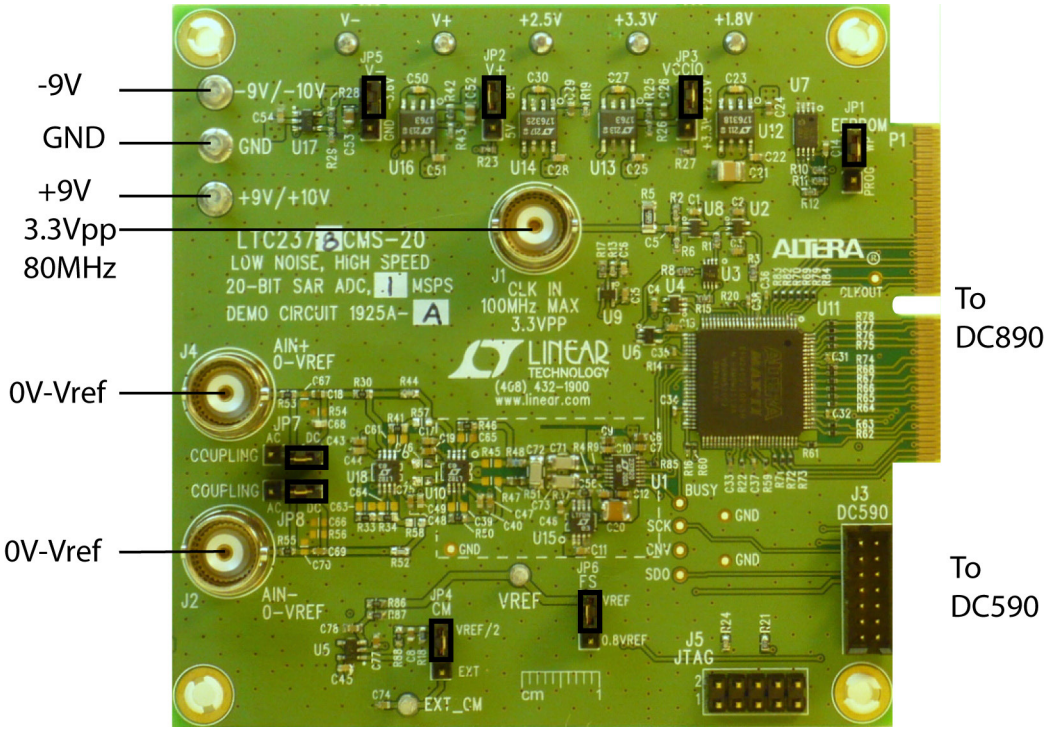


Figure 1. DC1925A Connection Diagram

ASSEMBLY OPTIONS

Table 1. DC1925A Assembly Options

ASSEMBLY VERSION	U1 PART NUMBER	MAX CONVERSION RATE	NUMBER OF BITS	MAX CLK IN FREQUENCY
DC1925A-A	LTC2378CMS-20	1Msps	20	80MHz
DC1925A-B	LTC2377CMS-20	500ksps	20	40MHz
DC1925A-C	LTC2376CMS-20	250ksps	20	20MHz

DC890 QUICK START PROCEDURE

Check to make sure that all switches and jumpers are set as shown in the connection diagram of Figure 1. In particular make sure that VCCIO (JP3) is set to the 2.5V position. Operating the DC1925A with the DC890 while JP3 is in the 3.3V position will cause noticeable performance degradation in SNR and THD. The default connections configure the ADC to use the onboard reference and regulators to generate the required common mode voltages. The analog input is DC coupled. Connect the DC1925A to a DC890 USB high speed data collection board using connector P1. Then, connect the DC890 to a host PC with a standard USB A/B cable. Apply ±9V to the indicated terminals. Then apply a low jitter differential sine source to J2 and J4. Connect a low jitter 80MHz 2.5V_{P-P} sine wave or square wave to connector J1. Note that J1 has a 50Ω termination resistor to ground.

Run the PScope software (PScope.exe version K73 or later) supplied with the DC890 or download it from www.linear.com/software.

Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

The PScope software should recognize the DC1925A and configure itself automatically.

Click the Collect button (See Figure 5) to begin acquiring data. The Collect button then changes to Pause, which can be clicked to stop data acquisition.

DC590 SETUP

IMPORTANT! To avoid damage to the DC1925A, make sure that VCCIO (JP6) of the DC590 is set to 3.3V before connecting the DC590 to the DC1925A.

VCCIO (JP3) of the DC1925A should be in the 3.3V position for DC590 operation. To use the DC590 with the DC1925A, it is necessary to apply –9V and ground to the –9V and GND terminals. Connect the DC590 to a host PC with a standard USB A/B cable. Connect the DC1925A to a DC590 USB serial controller using the supplied 14-conductor ribbon cable. Apply a signal source to J4 and J2 or J4 depending on how the DC1925A is configured.

Run the QuikEval software (version K92-01 or later) supplied with the DC590 or download it from www.linear.com/software. The correct control panel will be loaded automatically. Click the Collect button (See Figure 6) to begin reading the ADC.

DC1925A SETUP

DC Power

The DC1925A requires ±9VDC and draws approximately 100mA. Most of the supply current is consumed by the CPLD, op amps, regulators and discrete logic on the board. The +9VDC input voltage powers the ADC through LT1763 regulators which provide protection against accidental reverse bias. Additional regulators provide power for the CPLD and op amps. See Figure 1 for connection details.

Clock Source

You must provide a low jitter 2.5V_{P-P} (if VCCIO is in the 3.3V position, the clock amplitude should be 3.3V_{P-P}) sine or square wave to J1. The clock input is AC coupled so the DC level of the clock signal is not important. A clock generator like the Rohde & Schwarz SMB100A or the DC1216A-C is recommended. Even a good clock generator can start to produce noticeable jitter at low frequencies. Therefore it is recommended for lower sample rates to divide down a higher frequency clock to the desired input frequency. The ratio of clock frequency to conversion rate is 80:1. If the clock input is to be driven with logic, it is recommended that the 50Ω terminator (R5) be removed. Slow rising edges may compromise the SNR of the converter in the presence of high amplitude higher frequency input signals.

Data Output

Parallel data output from this board (0V to 2.5V default), if not connected to the DC890, can be acquired by a logic analyzer, and subsequently imported into a spreadsheet, or mathematical package depending on what form of digital signal processing is desired. Alternatively, the data can be fed directly into an application circuit. Use Pin 50 of P1 to latch the data. The data can be latched using either edge of this signal. The data output signal levels at P1 can also be changed to 0V to 3.3V if the application circuit requires a higher voltage. This is accomplished by moving VCCIO (JP3) to the 3.3V position.

Reference

The default reference is a LTC6655 5V reference. If an external reference is used it must settle quickly in the presence of glitches on the REF pin. To use an external reference, unsolder R37 and apply the reference voltage to the VREF terminal.

Analog Input

The default driver for the analog inputs of the LTC2378-20 on the DC1925A is shown in Figure 2. This circuit buffers a fully differential 0V to 5V input signal applied at AIN+ and AIN–. In addition, this circuit bandlimits the input frequencies to approximately 1.2MHz.

Alternatively, if your application circuit requires a single-ended signal to drive the ADC, the circuit shown in Figure 3 can be used. The circuit of Figure 3 converts a single-ended signal to the fully-differential signal required by the ADC. Additionally, this circuit further bandlimits the input frequencies to 100kHz which is the bandwidth limit of the ADC for low distortion performance.

The single-ended-to-differential circuit results in reduced THD performance, (approximately –112dB) due to the slight phase shift of the inverting op amp. The circuit in Figure 3 can be implemented on the DC1925A by removing R44 and R52 and adding R57 and R58. At this point it will only be necessary to drive AIN+ (J4).

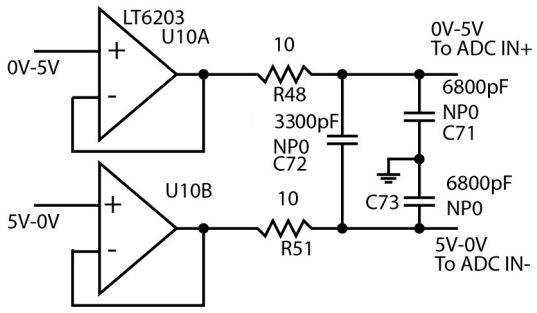


Figure 2. Fully-Differential Driver

DC1925A SETUP

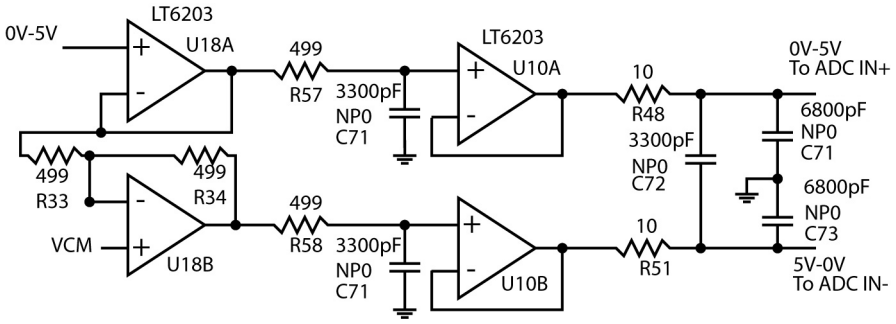


Figure 3. Single-Ended-to-Differential Driver

Data Collection

For SINAD, THD or SNR testing a low noise, low distortion differential output sine generator such as the Stanford Research DS360 should be used. A low jitter RF oscillator such as the Rohde & Schwarz SMB100A or DC1216A-C is used as the clock source.

This demo board is tested in house by attempting to duplicate the FFT plot shown in the typical performance characteristics of the LTC2378-20 data sheet. This involves using an 80MHz clock source, along with a differential output sinusoidal generator at a frequency of 2.0kHz. The input signal level is approximately –1dBfs. The input is level shifted and filtered with the circuit shown in Figure 4. A typical FFT obtained with DC1925A is shown in Figure 5. Note that to calculate the real SNR, the signal level (F1 amplitude = –0.998dB) has to be added back to the SNR that PScope displays. With the example shown in Figure 5 this means that the actual SNR would be 103.668dB instead of the 102.67dB that PScope displays. Taking the RMS sum of the recalculated SNR and the THD yields a SINAD of 103.62dB which is fairly close to the typical number for this ADC.

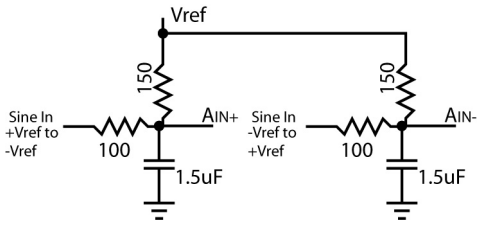


Figure 4. Differential Level Shifter

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that is common is feeding the converter with a frequency, that is a submultiple of the sample rate, and which will only exercise a small subset of the possible output codes. The proper method is to pick an M/N frequency for the input sine wave frequency. N is the number of samples in the FFT. M is a prime number between one and N/2. Multiply M/N by the sample rate to obtain the input sine wave frequency. Another scenario that can yield poor results is if you do not have a sine generator capable of ppm frequency accuracy or if it cannot be locked to the clock frequency. You can use an FFT with windowing to reduce the "leakage" or spreading of the fundamental, to get a close approximation of the ADC performance. If windowing is required, the Blackman-Harris 92dB window is recommended. If an amplifier or clock source with poor phase noise is used, windowing will not improve the SNR.

Layout

As with any high performance ADC, this part is sensitive to layout. The area immediately surrounding the ADC on the DC1925A should be used as a guideline for placement, and routing of the various components associated with the ADC. Here are some things to remember when laying out a board for the LTC2378-20. A ground plane is necessary to obtain maximum performance. Keep bypass capacitors as close to supply pins as possible. Use low impedance returns directly to the ground plane for each bypass capacitor. Use of a symmetrical layout around the analog inputs will minimize the effects of parasitic elements. Shield analog

DC1925A SETUP

input traces with ground to minimize coupling from other traces. Keep traces as short as possible.

Component Selection

When driving a low noise, low distortion ADC such as the LTC2378-20, component selection is important so as to not degrade performance. Resistors should have low values to minimize noise and distortion. Metal film resistors are recommended to reduce distortion caused by self heating. Because of their low voltage coefficients, to further reduce distortion NPO or silver mica capacitors should be used. Any buffer used to drive the LTC2378-20 should have low distortion, low noise and a fast settling time such as the LT6203.

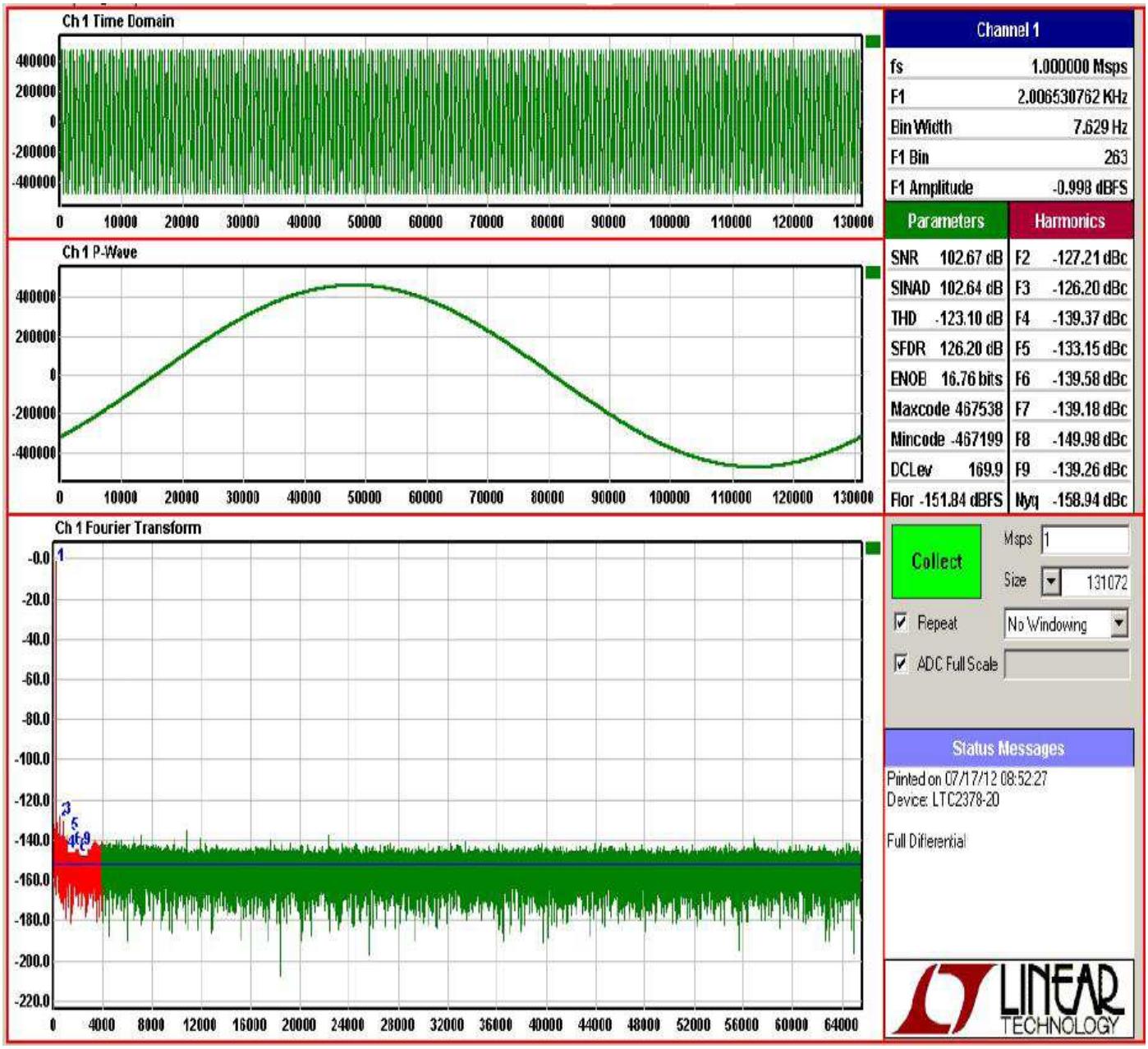


Figure 5. PScope Screen Shot

DC1925A SETUP

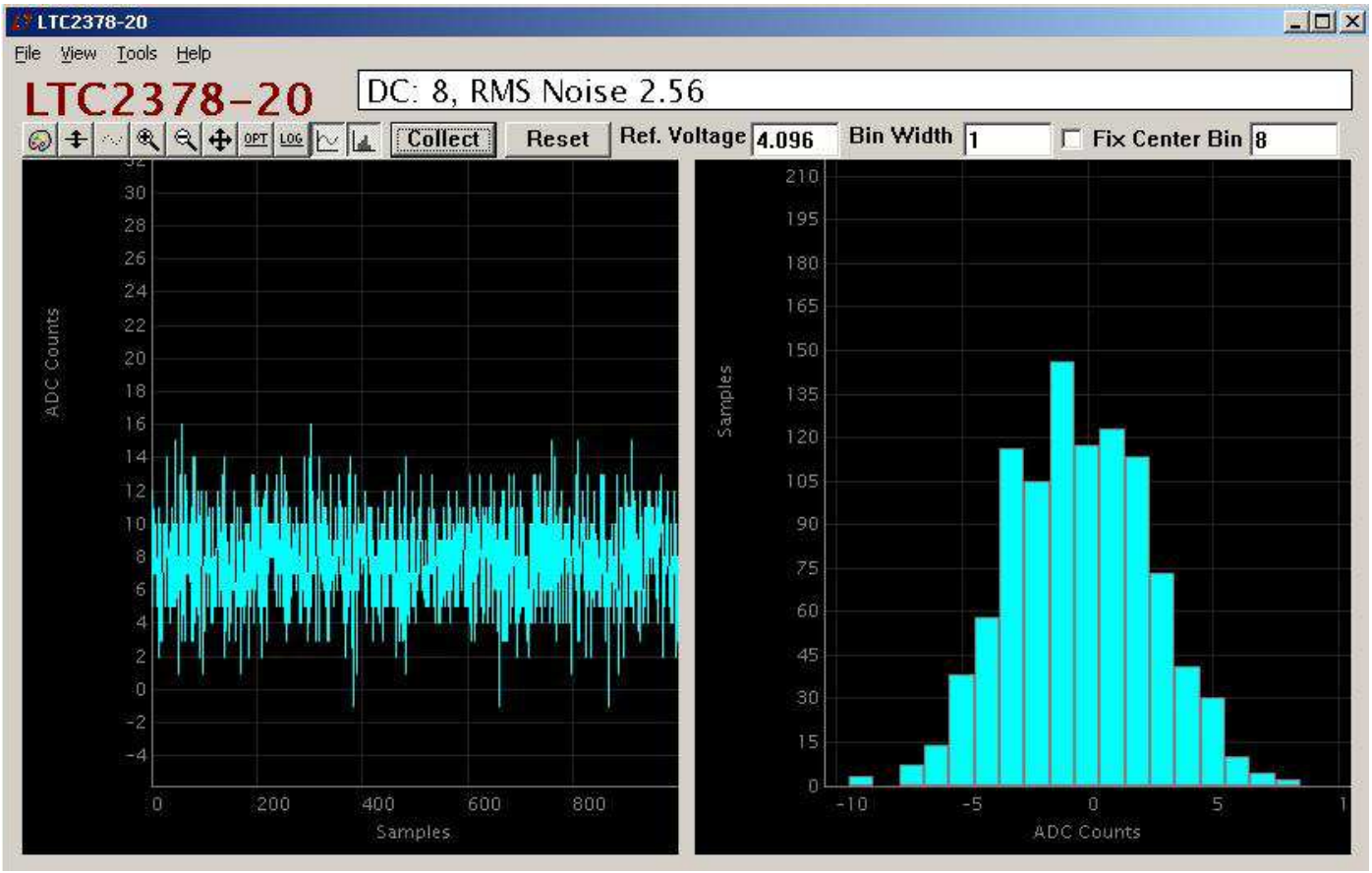


Figure 6. QuikEval Screen Shot

DC1925A JUMPERS

Definitions

JP1 – EEPROM is for factory use only. Leave this in the default WP position.

JP2 – V+ Selects 8V or 5V for V+. The default is position is 8V. Setting V+ to 5V is useful for evaluating single 5V supply operation of the buffer when operating the ADC with Digital Gain Compression turned on.

JP3 – VCCIO sets the output levels at P1 to either 3.3V or 2.5V. Use 2.5V to interface to the DC890 which is the default setting. Use 3.3V to interface to the DC590.

JP4 – VCM sets the DC bias for AIN+ and AIN– if the single ended to differential mode is enabled, and the inputs are AC coupled. $V_{REF}/2$ is the default setting.

JP5 – V– Selects –3.6V or ground for V–. The default setting is –3.6V. Setting V– to ground is useful for evaluating single supply operation of the buffer when operating the ADC with Digital Gain Compression turned on.

JP6 – FS selects whether the Digital Gain Compression is on or off. In the VREF position, Digital Gain Compression is off and the analog input range at $A_{IN}+$ and $A_{IN}–$ is 0V to V_{REF}. In the 0.8VREF position, Digital Gain Compression is turned on and the analog input range at $A_{IN}+$ and $A_{IN}–$ is $0.1V_{REF}$ to $0.9V_{REF}$. The default setting is off.

JP7 – Coupling selects AC or DC coupling of $A_{IN}+$. The default setting is DC.

JP8 – Coupling selects AC or DC coupling of $A_{IN}–$. The default setting is DC.

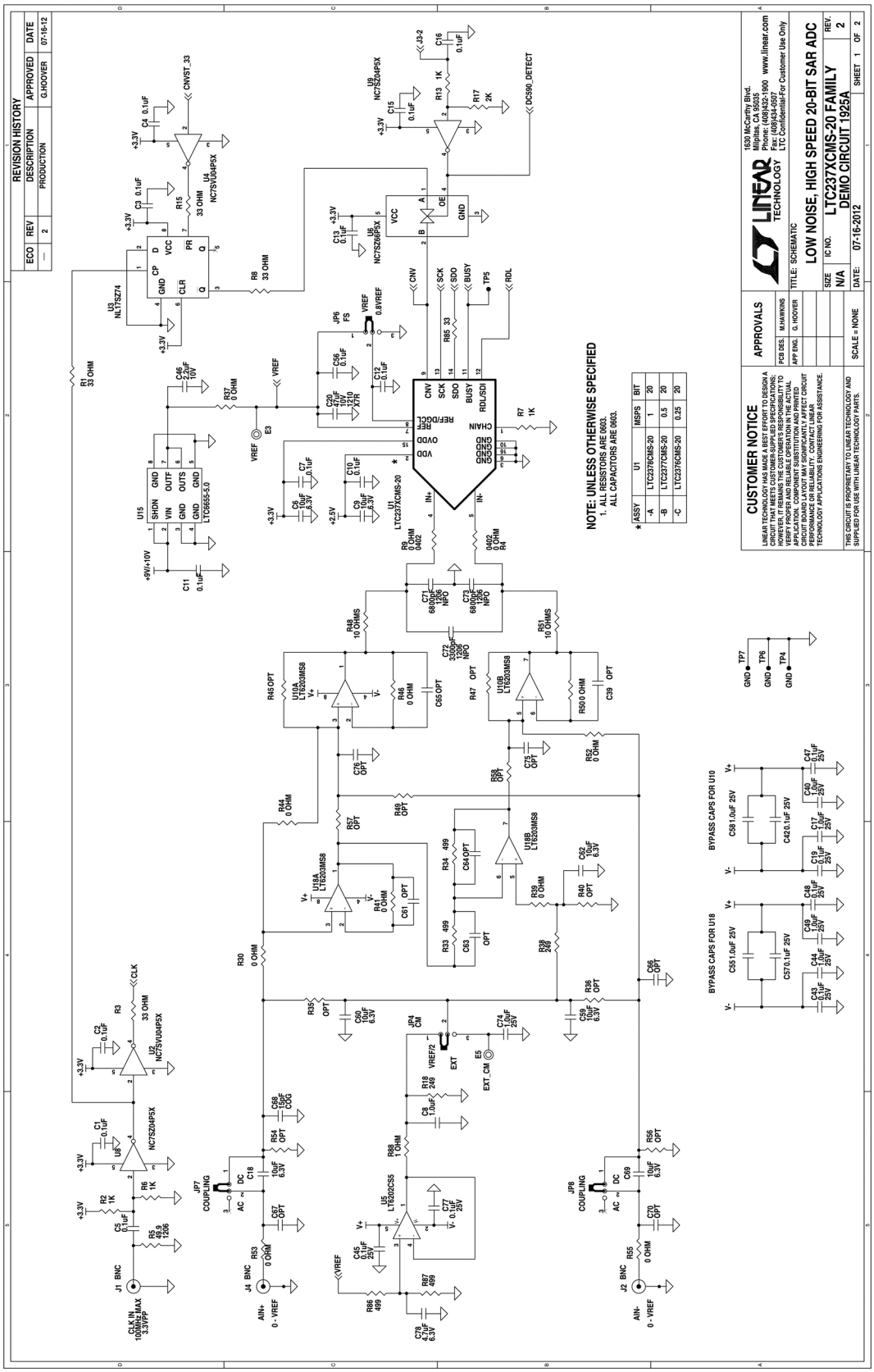
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC1925A General BOM				
1	13	C1-C5, C7, C10, C11, C13-C16, C56	CAP., X7R, 0.1µF, 16V 10% 0603	AVX, 0603YC104KAT2A
2	10	C6, C9, C18, C24, C26, C29, C59, C60, C62, C69	CAP., X5R, 10µF, 6.3V 20% 0603	AVX, 06036D106MAT2A
3	1	C8	CAP., X7R, 1µF, 16V 10% 0603	AVX, 0603YC105KAT2A
4	9	C12, C19, C42, C43, C45, C47, C48, C57, C77	CAP., X7R, 0.1µF, 25V 20% 0603	AVX, 06033C104MAT2A
5	12	C17, C22, C25, C28, C40, C44, C49, C51, C54, C55, C58, C74	CAP., X5R, 1µF, 25V 10% 0603 X5R OK	AVX, 06033D105KAT2A
6	1	C20	CAP., X7R, 47µF, 10V 10% 1210	MURATA, GRM32ER71A476KE15L
7	1	C21	CAP., X5R, 22µF, 25V 20% 1210	AVX, 12103D226MAT2A
8	4	C23, C27, C30, C50	CAP., X7R, 0.01µF, 25V 10% 0603	AVX, 06033C103KAT2A
9	8	C31, C32, C33, C34, C35, C36, C37, C38	CAP., X7R, 0.1µF, 16V 10% 0402	AVX, 0402YC104KAT2A
10	0	C39, C61, C63-C67, C70, C75, C76	CAP., OPT, 0603	OPTION
11	1	C46	CAP., X5R, 2.2µF, 10V 10% 0603	AVX, 0603ZD225KAT2A
12	2	C52 ,C53	CAP., X5R, 10µF, 25V 10% 0805	AVX, 08053D106KAT2A
13	1	C68	CAP., COG, 15pF, 50V 10% 0603	AVX, 06035A150KAT2A
14	2	C71, C73	CAP., NPO, 6800pF, 50V 5% 1206	MURATA, GRM3195C1H682JA01D
15	1	C72	CAP., NPO, 3300pF, 50V 10% 1206	AVX, 12065A332KAT2A
16	1	C78	CAP., X5R, 4.7µF, 6.3V 20% 0603	AVX, 06036D475MAT2A
17	7	E1, E2, E3, E4, E5, E9, E10	TEST POINT, TURRET, 0.061	MILL MAX, 2308-2-00-80-00-00-07-0
18	3	E6, E7, E8	TESTPOINT, TURRET, 0.094, PBF	MILL MAX, 2501-2-00-80-00-00-07-0
19	8	JP1-JP8	HEADER, 3-PIN SINGLE ROW 0.100	SAMTEC, TSW-103-07-L-S
20	3	J1, J2, J4	CONNECTOR, BNC	CONNEX, 112404
21	1	J3	CONN HEADER 14-POS 2MM VERT GOLD	MOLEX, 87831-1420
22	1	J5	HEADER, 2X5, 0.100"	SAMTEC, TSW-105-07-L-D
23	4	MH1, MH2, MH3, MH4	STANDOFF, NYLON 0.25"	KEYSTONE, 8831 (SNAP ON)
24	4	R1, R3, R8, R15	RES., CHIP, 33Ω, 1/10W, 5% 0603	YAGEO, RC0603JR-0733RL
25	8	R2, R6, R7, R13, R19, R24, R29, R43	RES., CHIP, 1k, 1/10W, 1% 0603	YAGEO, RC0603JR-071KL
26	2	R4, R9	RES., CHIP, 0Ω, 1/16W, 0402	YAGEO, RC0402JR-070RL
27	1	R5	RES., CHIP, 49.9Ω, 1/4W, 1% 1206	YAGEO, RC1206FR-0749R9L
28	4	R10, R11, R12, R81	RES., CHIP, 4.99k, 1/10W, 1% 0603	YAGEO, RC0603FR-74K99L
29	24	R14, R61-R79, R82, R83, R84, R85	RES., CHIP, 33Ω, 1/16W, 5% 0402	YAGEO, RC0402JR-0733RL
30	1	R16	RES., CHIP, 300Ω, 1/16W, 5% 0402	YAGEO, RC0402JR-07300RL
31	1	R17	RES., CHIP, 2k, 1/10W, 5% 0603	YAGEO, RC0603JR-072KL
32	2	R18, R38	RES., CHIP, 249Ω, 1/10W, 1% 0603	YAGEO, RC0603FR-07249RL
33	3	R20, R22, R59	RES., CHIP, 1k, 1/16W, 5% 0402	YAGEO, RC0402JR-071KL
34	1	R21	RES., CHIP, 10k, 1/10W, 5% 0603	YAGEO, RC0603JR-0710KL
35	1	R23	RES., CHIP, 6.49k, 1/10W, 1% 0603	YAGEO, RC0603FR-076K49L
36	1	R25	RES., CHIP, 1.69k, 1/10W, 1% 0603	YAGEO, RC0603FR-071K69L
37	1	R26	RES., CHIP, 1.54k, 1/10W, 1% 0603	YAGEO, RC0603FR-071K54L

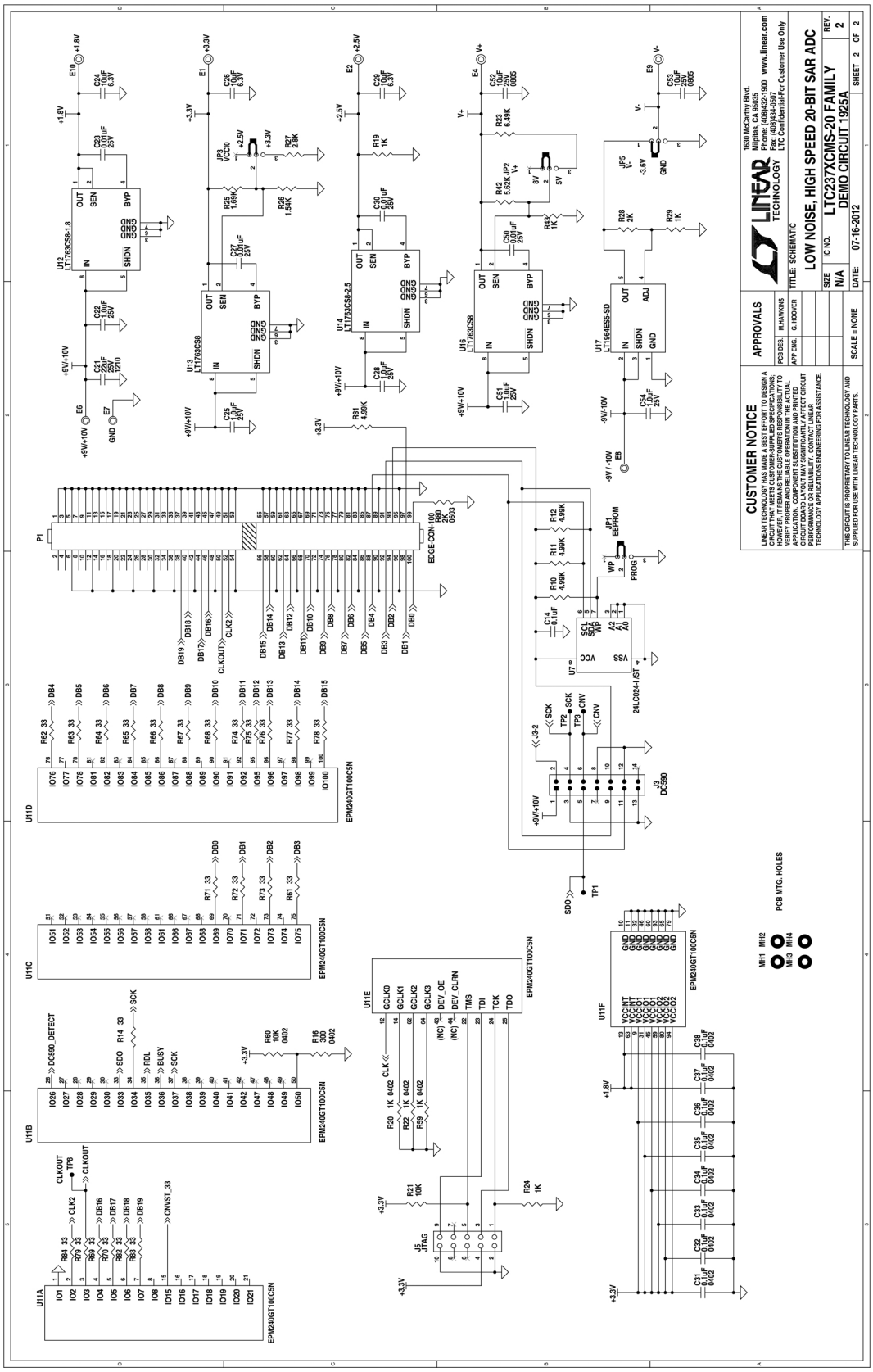
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
38	1	R27	RES., CHIP, 2.8k, 1/10W, 1% 0603	YAGEO, RC0603FR-072K8L
39	2	R28, R80	RES., CHIP, 2k, 1/10W, 1% 0603	YAGEO, RC0603FR-072KL
40	10	R30, R37, R39, R41, R44, R46, R50, R52, R53, R55	RES., CHIP, 0Ω, 1/10W, 0603	YAGEO, RC0603JR-070RL
41	4	R33, R34, R86, R87	RES., CHIP, 499Ω, 1/10W, 1% 0603	VISHAY, CRCW0603499RFKEA
42	10	R35, R36, R40, R45, R47, R49, R54, R56, R57, R58	RES., CHIP, OPT, 0603	OPTION
43	1	R42	RES., CHIP, 5.62k, 1/10W, 1% 0603	YAGEO, RC0603FR-075K62L
44	2	R48,R51	RES., CHIP, 10Ω, 1/10W, 1% 0603	YAGEO, RC0603FR-0710RL
45	1	R60	RES., CHIP, 10k, 1/16W, 5% 0402	YAGEO, RC0402JR-0710KL
46	1	R88	RES., CHIP, 1Ω, 1/10W, 5% 0603	YAGEO, RC0603JR-071RL
47	2	U2, U4	IC, UNBUFFERED INVERTER, SC70-5	FAIRCHILD, NC7SVU04P5X
48	1	U3	IC, D FLIP-FLOP, US8	ON SEMI., NL17SZ74USG
49	1	U5	IC, OP AMP, LOW NOISE, TSOT-23	LINEAR TECH., LT6202CS5#PBF
50	1	U6	IC, SINGLE SPST BUS SWITCH, SC70-5	FAIRCHILD, NC7SZ66P5X
51	1	U7	IC, SERIAL EEPROM, TSSOP	MICROCHIP, 24LC024-I/ST
52	2	U8, U9	IC, UHS INVERTER, SC70-5	FAIRCHILD, NC7SZ04P5X
53	2	U10, U18	IC, DUAL OP AMP, MS8	LINEAR TECH., LT6203CMS8#PBF
54	1	U11	IC, MAX II CPLD, TQFP100	ALTERA, EPM240GT100C5N
55	1	U12	IC, MICROPOWER REGULATOR, SO-8	LINEAR TECH., LT1763CS8-1.8#PBF
56	2	U13, U16	IC, MICROPOWER REGULATOR, SO-8	LINEAR TECH., LT1763CS8#PBF
57	1	U14	IC, MICROPOWER REGULATOR, SO-8	LINEAR TECH., LT1763CS8-2.5#PBF
58	1	U15	IC, VOLTAGE REFERENCE, MSOP	LINEAR TECH., LTC6655BHMS8-5#PBF
59	1	U17	IC, MICROPOWER NEG. REGULATOR	LINEAR TECH., LT1964ES5-SD#PBF
60	8	XJP1-XJP8	SHUNT, 0.100 CENTERS	SAMTEC, SNT-100-BK-G
61	2		STENCIL, (TOP & BOTTOM)	STENCIL DC1925A
DC1925A-A				
1	1		GENERAL BOM	DC1925A
2	1	U1	IC, HIGH SPEED, LOW NOISE SAR ADC	LINEAR TECH., LTC2378CMS-20#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1925A-2
DC1925A-B				
1	1		GENERAL BOM	DC1925A
2	1	U1	IC, HIGH SPEED, LOW NOISE SAR ADC	LINEAR TECH., LTC2377CMS-20#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1925A-2
DC1925A-C				
1	1		GENERAL BOM	DC1925A
2	1	U1	IC, HIGH SPEED, LOW NOISE SAR ADC	LINEAR TECH., LTC2376CMS-20#PBF
3	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1925A-2

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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If this evaluation kit does not meet the specifications recited in the DEMO BOARD manual the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY THE SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THIS INDEMNITY, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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