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LTC6430 and LTC2158
15dB Differential Amplifier
and 14-Bit, 310Msps Dual ADC

DESCRIPTION

Demonstration circuit 1946A supports the LTC®6430 and the LTC2158 high speed ADC. It was specially designed for applications that include an LTC6430, a high speed amplifier with 15dB of gain.

The circuitry on the analog inputs is optimized for analog input frequencies from 50MHz up to 1GHz. Refer to the data sheet for proper input networks for different input frequencies

Design files for this circuit board are available at http://www.linear.com/demo

Table 1. DC1946A

DEMONSTRATION CIRCUIT	ADC PART NUMBER	AMPLIFIER PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1946A	LTC2158-14	LTC6430-15	14-BIT	310Msps	50-1000MHz

Table 2. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage – ADC (V⁺)	This Supply Must Provide Up to 800mA.	3.0		6	V
Supply Voltage – Amplifier (+5V)	This Supply Must Provide Up to 500mA. This Pin Is Unregulated	4.75	5	5.25	V
Analog Input Range				400	mV_{P-P}
Logic Input Voltages	Minimum Logic High	1.2			V
	Maximum Logic Low			0.6	V
Logic Output Voltages (Differential)	Nominal Logic Levels (100Ω Load, 3.5mA Mode, 1.25V Common Mode)		350		mV
	Minimum Logic levels (100Ω Load, 3.5mA Mode, 1.25V Common Mode)		247		mV
Sampling Frequency (Encode Clock Frequency)		10		310	MHz
Encode Clock Level (Single-Ended at J2)	Minimum Logic Levels (ENC⁻ Tied to GND)	0			V
	Maximum Logic Level (ENC⁻ Tied to GND)			3.6	V
Encode Clock Level (Differential at J2)	Minimum Logic Levels (ENC⁻ Not Tied to GND, 1.2V Common Mode)	0.2			V

QUICK START PROCEDURE

Demonstration circuit 1946A is easy to set up to evaluate the performance of the LTC2158 A/D converter. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

SETUP

The DC1371 USB demonstration circuit was supplied with the DC1946A global demonstration circuit, follow the DC1371 Quick Start Guide to install the required software and for connecting the DC1371 to the DC1946A and to a PC.
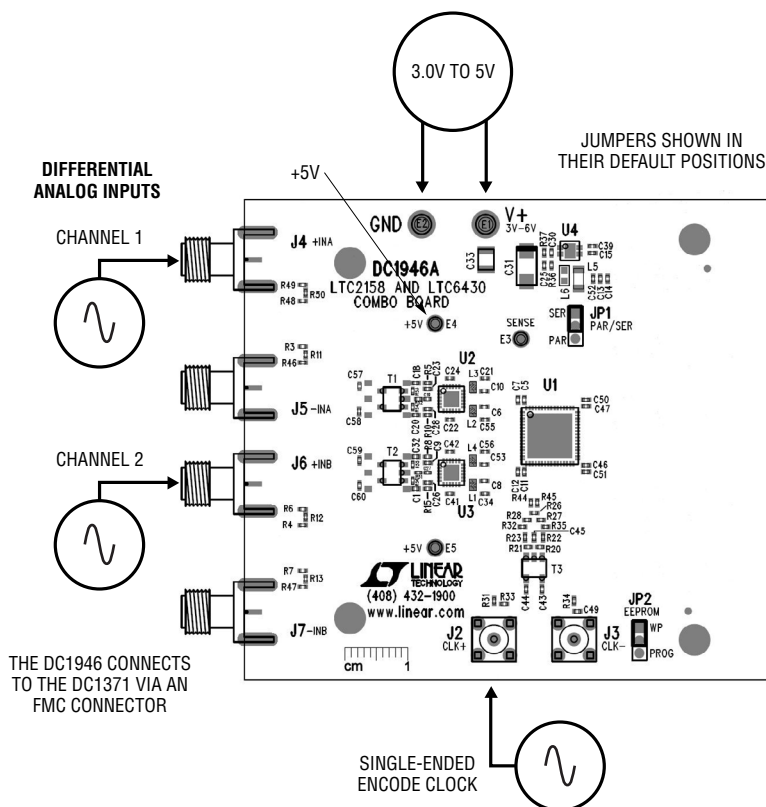
Figure 1. DC1946A Setup (Zoom for Detail)

dc1946af

QUICK START PROCEDURE

HARDWARE SETUP

SMAs

J4 & J5: Channel 1 Analog Inputs: As a default the DC1946A is populated to accept a single-ended input. Apply a single-ended signal to J4. For use with a differential signal remove R3 and populate R11 with a 0Ω resistor. Apply a differential signal to these SMA connectors from a differential driver. These SMAs are positioned 0.8" apart to accommodate LTC differential driver boards.

J6 & J7: Channel 2 Analog Inputs. As a default the DC1946A is populated to accept a single-ended input. Apply a single-ended signal to J6. For use with a differential signal remove R7 and populate R13 with a 0Ω resistor. Apply a differential signal to these SMA connectors from a differential driver. These SMAs are positioned 0.8" apart to accommodate LTC differential driver boards.

J2 CLK+: Positive Encode Clock Input. As a default the demo board is populated to accept a single-ended clock input from a low jitter signal generator. For other population options see the encode clock section of this manual.

J3 CLK–: Negative Encode Clock Input. As a default this input port is grounded to accommodate the single-ended clock drive. For other population options see the encode clock section of this manual.

Turrets

V+ : Positive input voltage for the ADC and digital buffers. This voltage feeds a regulator that supplies the proper voltages for the ADC and buffers. The voltage range for this turret is 3.3V to 5V.

+5V: Positive input voltage for the LTC6430. Apply a 5V signal to this turret to power the LTC6430. This turret is connected to the amplifier directly and is not regulated. There is a resistor on the back of the board R14 that will connect the power pins of the two amplifiers. By removing this resistor each amplifier can be powered independently.

SENSE: Optional Reference Voltage. This pin is connected directly to the SENSE pin of the ADC. Connect SENSE to a 1.25V external reference and the external reference mode is automatically selected. The external reference must be 1.25V ±25mV for proper operation. If no external voltage is supplied, this pin will be pulled up to V_{DD} through a weak pull-up resistor.

GND: Ground Connection. This demo board only has a single ground plane. This turret should be tied to the GND terminal of the power supply being used.

Jumpers

The DC1946A demonstration circuit should have the following jumper settings as default positions (per Figure 1) which configure the ADC in serial programming mode. In the default configuration JP1-JP2 should be left in the default locations. This will pull PAR/SER low putting the part in serial configuration mode.

JP1-PAR/SER: Selects Parallel or Serial Programming Mode (Default: Serial). The DC1946A will not work in parallel programming mode unless a custom FPGA load is used.

JP2-EEPROM: EEPROM Write Protect. For factory use only. Should be left in the enable (PROG) position.

APPLYING POWER AND SIGNALS TO THE DC1946A DEMONSTRATION CIRCUIT

If a DC1371 is used to acquire data from the DC1946A, the DC1371 must FIRST be connected to a powered USB port and provided an external 5V BEFORE applying +3V to +5.0V across the pins marked V+ and GND on the DC1946A. The 5V for the LTC6430 should be applied after the ADC is powered. DC1946A requires 3V for proper operation. Regulators on the board produce the voltages required for the ADC. The power for the LTC6430 is unregulated. The DC1946A demonstration circuit requires up to 800mA on V+ and 500mA on +5V. The DC1946A should not be removed or connected to the DC1371 while power is applied.

QUICK START PROCEDURE

ANALOG INPUT NETWORK

The input network of the DC1946A can be modified to accommodate various applications. In the default setup J4 and J6 are used as single-ended inputs. Onboard transformers are used to do a single-ended-to-differential translation to drive the LTC6430 differentially. If differential drive is desired both of the inputs are brought out to SMA connectors so the demo board can be driven with a differential source. To drive the demo board with a differential source simply remove R3 and R7 and populate R11 and R13 with 0Ω resistors. Then remove T1 and T2 and jump over the pads with 0Ω resistors. This will allow the board to be driven differentially from a differential source. The inputs SMA connectors for the input signals are 0.8" apart to accommodate LTC differential driver boards.

In almost all cases, off board filters will be required on the analog input of the differential driver to produce data sheet SNR.

The off board filters should be located close to the inputs of the differential driver to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

Apply the analog input signal of interest to the SMA connectors on the DC1946A marked J4 and J6.

ENCODE CLOCK

Apply an encode clock to the SMA connector on the DC1946A demonstration circuit board marked J2. As a default the DC1946A is populated to have a single-ended clock input. It is possible to modify the demo board.

For the best noise performance, the encode input must be driven with a very low jitter signal source. The amplitude should be as large as possible up to $2V_{P-P}$ or 10dBm.

Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1946A, a bandpass filter used for the clock should be used prior to the DC1075A. Data sheet FFT plots are taken with 10-pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, nonharmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used with TTE bandpass filters for both the clock input and the analog input.

When using a PECL or LVDS clock you can drive the DC1946A differentially through J2 and J3. From the default population, remove the resistors in the R33, R22 and R23 positions and populate 0Ω resistors in the R31, R32, R34, and R35 positions. Add the appropriate termination for your clock signal. R27, R28, R29, R30 and R26 are available to provide the proper termination for LVDS, PECL, or CML signaling. Blocking capacitors can be installed in the R44 and R45 positions if the common mode voltage of the clock is not compatible with the LTC2158.

SOFTWARE

The DC1371 is controlled by the PScope™ system software provided or downloaded from the Linear Technology website at http://www.linear.com/software/. If a DC1371 was provided, follow the DC1371 Quick Start Guide and the instructions below.

To start the data collection software if "PScope.exe", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1946A demonstration circuit is properly connected to the DC1371, PScope should automatically detect the DC1946A, and configure itself accordingly. If necessary the procedure below explains how to manually configure PScope.

Under the "Configure" menu, go to "ADC Configuration...." Check the "Config Manually" box and use the following configuration options, see Figure 2:

Manual Configuration settings:

Bits: 14

Alignment: 16

FPGA Ld: S2157

Channs: 2

QUICK START PROCEDURE

Figure 2: ADC Configuration

Bipolar: Unchecked

Positive-Edge Clk: Unchecked

If everything is hooked up properly, powered and a suitable encode clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC1371 Quick Start Guide and in the online help available within the PScope program itself.

SERIAL PROGRAMMING

PScope has the ability to program the DC1946A board serially through the DC1371. There are several options available for the LTC2158 that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the "Set Demo Bd Options" icon on the PScope toolbar (Figure 3).
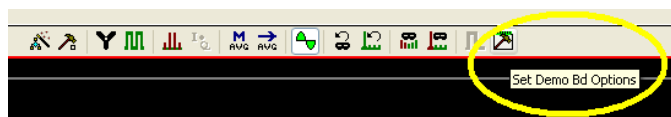
Figure 3: PScope Toolbar

This will bring up the menu shown in Figure 4.

This menu allows any of the options available for the LTC2158 to be programmed serially. The LTC2158 family has the following options:
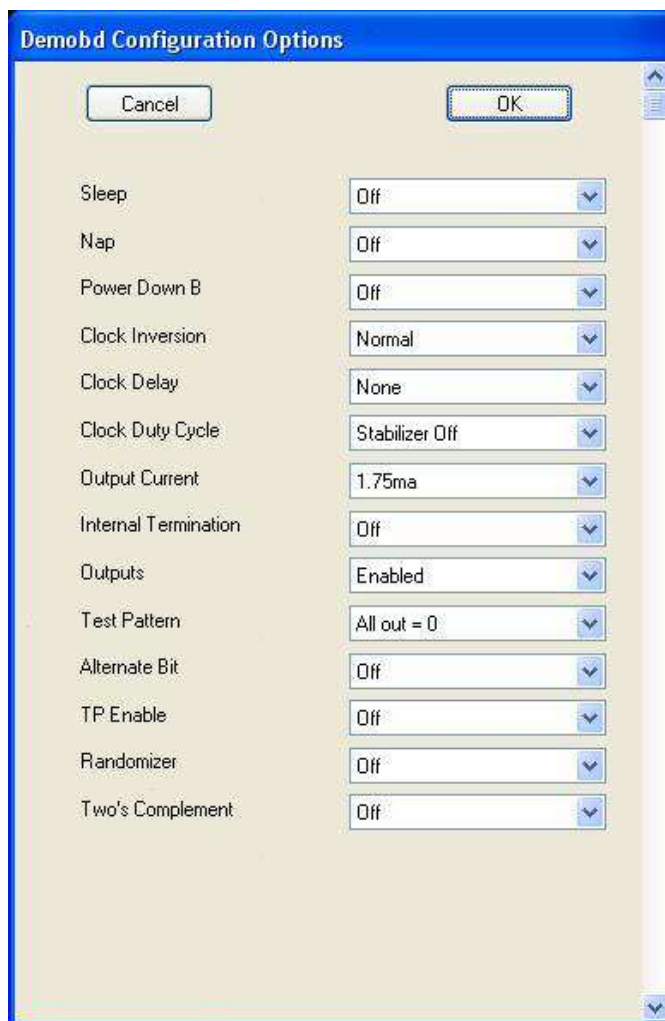
Figure 4: Demobd Configuration Options

Sleep Mode – Selects between normal operation, sleep modes:

   Off (Default): ADC is powered and active

   On: ADC is powered down

Nap Mode – ADC core powers down while references stay active:

   Off (Default): ADC is powered and active

   On: ADC is put into nap mode

Power Down B – Powers down channel 2 while references stay active:

   Off (Default): ADC is powered and active

   On: Channel 2 of ADC is powered down

dc1946af

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QUICK START PROCEDURE

Clock Invert – Selects the polarity of the CLKOUT signal:

Disable (Default): Normal CLKOUT polarity

Enable: CLKOUT polarity is inverted

Clock Delay – Selects the phase delay of the CLKOUT signal:

None (Default): No CLKOUT delay

45 deg: CLKOUT delayed by 45 degrees

90 deg: CLKOUT delayed by 90 degrees

135 deg: CLKOUT delayed by 135 degrees

Clock Duty Cycle – Enables or disables duty cycle stabilizer:

Stabilizer off (Default): Duty cycle stabilizer disabled

Stabilizer on: Duty cycle stabilizer enabled

Output Current – Selects the LVDS output drive current:

1.75mA (Default): LVDS output driver current

2.1mA: LVDS output driver current

2.5mA: LVDS output driver current

3.0mA: LVDS output driver current

3.5mA: LVDS output driver current

4.0mA: LVDS output driver current

4.5mA: LVDS output driver current

Internal Termination – Enables LVDS internal termination:

Off (Default): Disables internal termination

On: Enables internal termination

Outputs – Enables digital outputs:

Enabled (Default): Enables digital outputs

Disabled: Disables digital outputs

Test Pattern – Selects Digital output test patterns:

Off (Default): ADC data presented at output

All out = 1: All digital outputs are 1

All out = 0: All digital outputs are 0

Checkerboard: OF and D13-D0 Alternate between 1 01 0101 1010 0101 and 0 10 1010 0101 1010 on alternating samples.

Alternating: Digital outputs alternate between all 1's and all 0's on alternating samples.

ABP – Alternate bit polarity (ABP) mode

Off (Default): Disables alternate bit polarity

On: Enables alternate bit polarity (Before enabling ABP, be sure the part is in offset binary mode)

TP Enable – Enables test patterns

Disabled (Default): Disables test patterns, ADC data presented at output

Enabled: Enables the test pattern

Randomizer – Enables data output randomizer

Off (Default): Disables data output randomizer

On: Enables data output randomizer

Two's Complement – Enables two's complement mode

Off (Default): Selects offset binary mode

On: Selects two's complement mode

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC1946A demo board.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	14	C1, C3, C6, C8, C10, C16, C18, C20, C22, C24, C32, C41, C42, C53	CAP., NPO, 1000pF, 50V 5% 0402	MURATA, GRM1555C1H102JA01D
2	16	C2, C5, C11, C13, C14, C21, C25, C29, C34, C40, C50, C51, C52, C54, C55, C56	CAP., X5R, 0.1µF, 10V 10% 0402	AVX, 0402ZD104KAT2A
3	3	C4, C17, C30	CAP., X5R, 2.2µF, 10V 20% 0402	TAIYO YUDEN, LMK105BJ225MV-F
4	4	C7, C12, C46, C47	CAP., X5R, 0.47µF, 10V 10% 0402	TDK, C1005X5R1A474K
5	4	C9, C23, C26, C28	CAP., NPO, 68pF, 16V 5% 0402	TDK, C1005C0G1H680J
6	2	C15, C39	CAP., X5R, 1.0µF, 10V 10% 0402	AVX, 0402ZD105KAT2A
7	0	C19, C27, C48, C57, C58, C59, C60	CAP., OPT, 0402	OPTION
8	1	C31	CAP., TANT., 100µF 16V 10% 6032	KEMET, T491C107K016ZT
9	1	C33	CAP., X5R, 47µF, 16V 20% 1210	TAIYO YUDEN, EMK325BJ476MM-T
10	4	C35, C36, C37, C38	CAP., X7R, 47pF, 16V 10% 0402	AVX, 0402YC470KAT2A
11	4	C43, C44, C45, C49	CAP., X5R, 0.01µF, 16V 10% 0402	AVX, 0402YC103KAT2A
12	2	E1, E2	TEST POINT, TURRET, 0.094, PBF	MILL-MAX, 2501-2-00-80-00-00-07-0
13	3	E3, E4, E5	TEST POINT, TURRET, 0.061, PBF	MILL-MAX, 2308-2-00-80-00-00-07-0
14	2	JP1, JP2	HEADER, 3 PIN, 0.079	SULLINS, NRPN031PAEN-RC
15	1	J1	BGA CONNECTOR, 40X10	SAMTEC, SEAM-40-02.0-S-10-2-A-K-TR
16	2	J2, J3	CON., SMA JACK, STRAIGHT, THRU-HOLE	AMPHENOL CONNEX, 132134
17	4	J4, J5, J6, J7	CON., SMA 50Ω EDGE-LAUNCH	EMERSON, 142-0701-851
18	4	L1, L2, L3, L4	INDUCTOR, CER. CHIP, 560nH, 2%, 0603	COILCRAFT, 0603LS-561XGLB
19	1	L5	FERRITE BEAD, 33Ω @ 100MHz, 1206	MURATA, BLM31PG330SN1L
20	1	L6	RES., CHIP, 0Ω, 1/10W, 0603	VISHAY, CRCW06030000Z0EA
21	0	L7 (OPT)	INDUCTOR, OPTION, 0603	OPTION
22	2	L8, L9	INDUCTOR, CER. CHIP, 120nH, 2%, 0402	COILCRAFT, 0402CS-R12XGLU
23	8	R1, R2, R16, R17, R20, R21, R38, R39	RES., CHIP, 49.9Ω, 1/16W, 1% 0402	VISHAY, CRCW040249R9FKED
24	7	R3, R7, R12, R33, R44, R45, R50	RES., CHIP, 0Ω, 1/16W, 0402	VISHAY, CRCW04020000Z0ED
25	0	R4, R6, R11, R13, R27, R28, R29, R30, R31, R32, R34, R35, R46, R47, R48, R49, R51, R52	RES., CHIP, OPT, 0402	OPTION
26	4	R5, R8, R10, R15	RES., CHIP, 348Ω, 1/16W, 1% 0402	VISHAY, CRCW0402348RFKED
27	2	R9, R37	RES., CHIP, 3k, 1/16W, 1% 0402	VISHAY, CRCW04023K00FKED
28	1	R14	RES., CHIP, 0Ω, 1/8W, 0805	VISHAY, CRCW08050000Z0EA
29	3	R18, R24, R25	RES., CHIP, 4.99k, 1/16W, 1% 0402	VISHAY, CRCW04024K99FKED
30	5	R19, R40, R41, R42, R43	RES., CHIP, 1k, 1/16W, 1% 0402	VISHAY, CRCW04021K00FKED
31	2	R22, R23	RES., CHIP, 5.1Ω, 1/16W, 1% 0402	VISHAY, CRCW04025R10FKED
32	1	R26	RES., CHIP, 100Ω, 1/16W, 1% 0402	VISHAY, CRCW0402100RFKED
33	1	R36	RES., CHIP, 182k, 1/16W, 1% 0402	VISHAY, CRCW0402182KFKED
34	4	R53, R54, R55, R56	RES., CHIP, 150Ω, 1/16W, 1%, 0402	VISHAY, CRCW0402150RFKED

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
35	3	T1, T2, T3	TRANSFORMER, RF,SMT, 1:1BALUN	MACOM, MABA-007159-000000
36	0	T4, T5 (OPT)	OPTION: TRANSFORMER, RF,SMT, 1:1BALUN	MINI-CIRCUTS, ADTL2-18+
37	1	U1	IC, DUAL 14-BIT ADC, QFN64	LINEAR TECH., LTC2158CUP-14#PBF
38	2	U2, U3	IC, 50Ω IF AMPLIFIER, QFN	LINEAR TECH., LTC6430AIUF-15#PBF
39	1	U4	I.C., LOW DROPOUT REGULATOR, 3X3MM, DFN	LINEAR TECH., LT3080EDD-1#PBF
40	1	U5	IC, SERIAL EEPROM, TSSOP	MICROCHIP TECH., 24LC32A-I/ST
41	2	XJP1, XJP2	SHUNT, 2MM	SAMTEC, 2SN-BK-G

REVISION HISTORY

ECO	REV	DESCRIPTION	APPROVED	DATE
-	3	PRODUCTION	C.MAYOTT	10/18/2013

V+ 3V-6V E1
V+
GND E2

C33 47uF 1210
C15 1.0uF
C39 1.0uF

U4 LT3080EDD-1
VIN 7
VIN 8
VOUT 3
VOUT 2
VOUT 1
VCTRL 5
SET 4
PAD

0 OHM RES. L6 VDD
C30 2.2uF
C31 100uF 6032
R37 3K
L5 OVDD
FERRITE BEAD, 33 OHMS 1206
C52 0.1uF
C13 0.1uF
C14 0.1uF

R36 182K
R19 1K VDD
C25 0.1uF

JP1 PAR/SER
SER 1
2
PAR 3

SENSE E3
R9 3K VDD
C17 2.2uF VDD

SDO
SDI
SCK
CS

DA12_13+ DA12_13-
DA10_11+ DA10_11-
DA8_9+   DA8_9-
DA6_7+   DA6_7-

AIN1+
R16 49.9
C40 0.1uF
R17 49.9
AIN1-
C4 2.2uF

AIN2+
R38 49.9
R39 49.9
C29 0.1uF
R1 49.9
C2 0.1uF
R2 49.9
AIN2-

U1 LTC2158-14
GND PAD

VDD
VDD
GND
AINA+
GND
AINA-
SENSE
VREF
GND
VCM
GND
AINB-
AINB+
GND
VDD
VDD
GND

OGND
DA4_5+
DA4_5-
DA2_3+
DA2_3-
DA0_1+
DA0_1-
CLKOUT+
CLKOUT-
DB12_13+
DB12_13-
DB10_11+
DB10_11-
DB8_9+
DB8_9-
OGND

DA4_5+ DA4_5-
DA2_3+ DA2_3-
DA0_1+ DA0_1-
CLKOUT+ CLKOUT-
DB12_13+ DB12_13-
DB10_11+ DB10_11-
DB8_9+ DB8_9-

OVDD

DB6_7+ DB6_7-
DB4_5+ DB4_5-
DB2_3+ DB2_3-
DB0_1+ DB0_1-
OF+   OF-

C48 OPT
R30 OPT
L7 OPT 0603
R31 OPT R32 OPT
R33 0 OHMS
C44 0.01uF
T3 MABA-007159-000000
R23 5.1
R21 49.9
R28 OPT
R26 100
R44 0 OHMS
VDD
OVDD
C5 0.1uF C7 0.47uF C11 0.1uF C12 0.47uF C50 0.1uF C47 0.47uF C51 0.1uF C46 0.47uF

CLK+ J2
CLK- J3
C43 0.01uF
C45 0.01uF
R20 49.9
R22 5.1
R34 OPT R35 OPT
R27 OPT
R45 0 OHMS
R29 OPT
C49 0.01uF

NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS AND CAPACITORS ARE 0402

APPROVALS
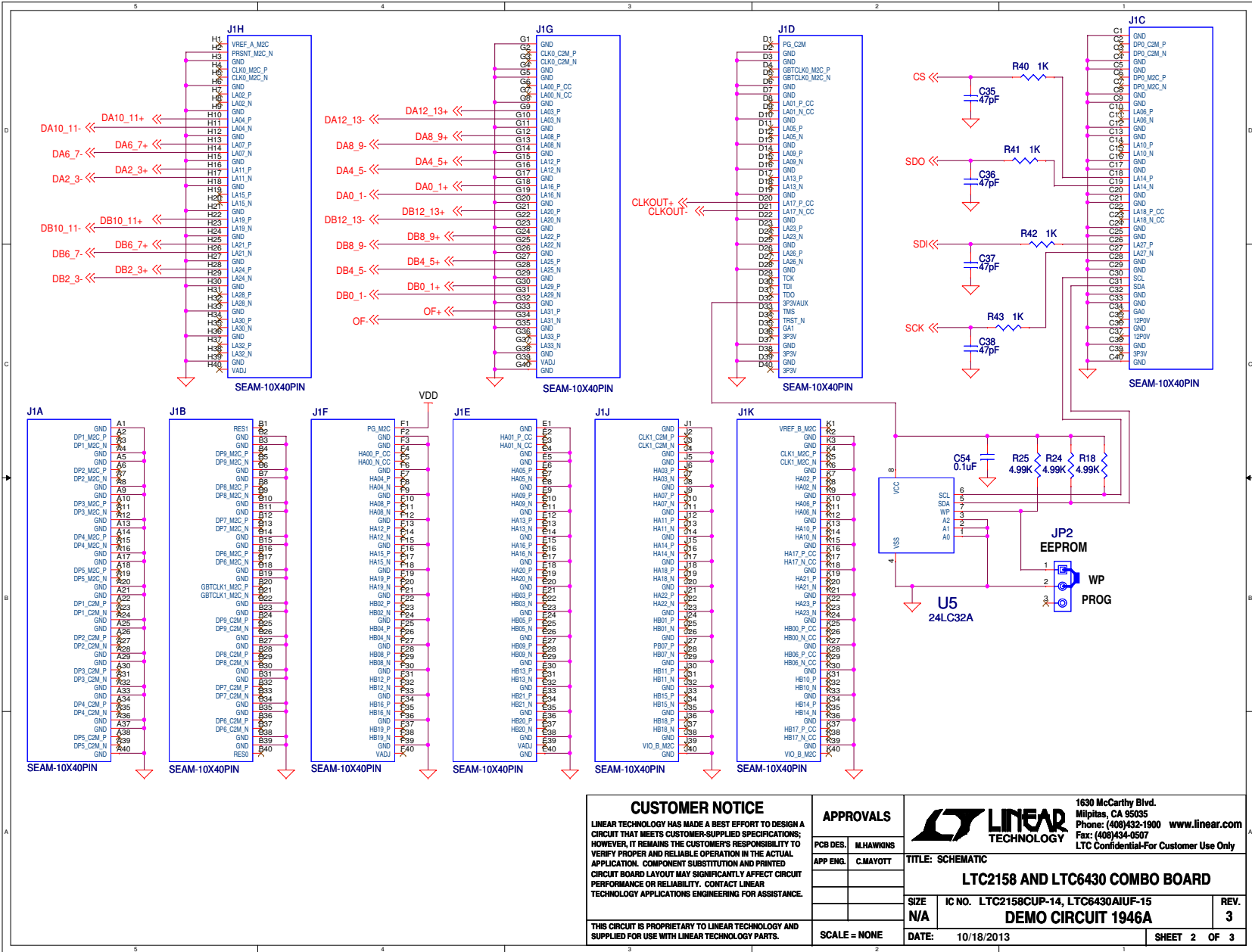PCB DES. M.HAWKINS
APP ENG. C.MAYOTT

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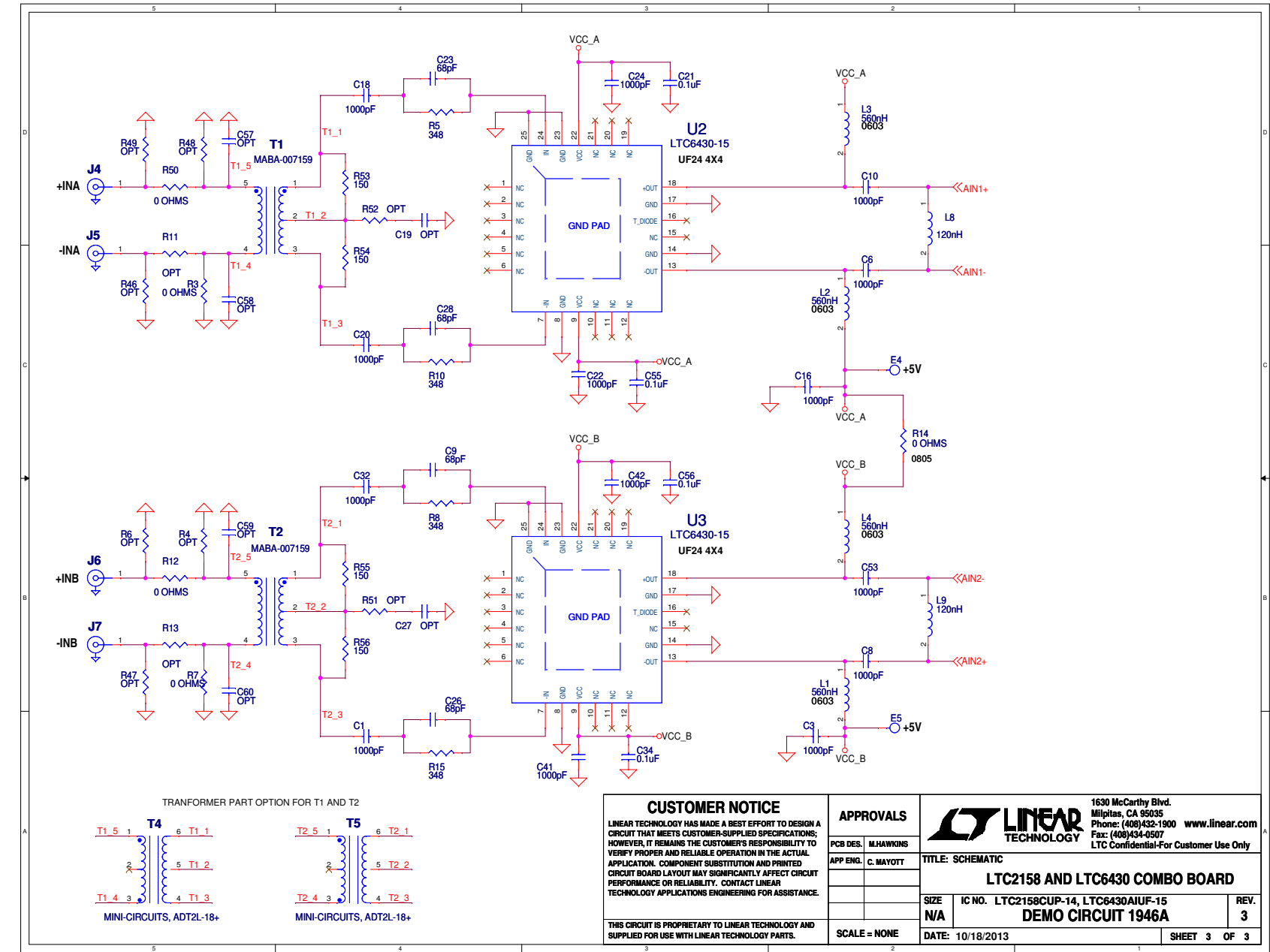LTC Confidential-For Customer Use Only

TITLE: SCHEMATIC
LTC2158 AND LTC6430 COMBO BOARD

SIZE N/A
IC NO. LTC2158CUP-14, LTC6430AIUF-15
DEMO CIRCUIT 1946A
REV. 3
DATE: 10/18/2013
SHEET 1 OF 3

J1H — SEAM-10X40PIN

DA10_11+ ← DA10_11+
DA10_11- ←
DA6_7+ ← DA6_7+
DA6_7- ←
DA2_3+ ← DA2_3+
DA2_3- ←
DB10_11+ ← DB10_11+
DB10_11- ←
DB6_7+ ← DB6_7+
DB6_7- ←
DB2_3+ ← DB2_3+
DB2_3- ←

J1G — SEAM-10X40PIN

DA12_13+ ← DA12_13+
DA12_13- ←
DA8_9+ ← DA8_9+
DA8_9- ←
DA4_5+ ← DA4_5+
DA4_5- ←
DA0_1+ ← DA0_1+
DA0_1- ←
DB12_13+ ← DB12_13+
DB12_13- ←
DB8_9+ ← DB8_9+
DB8_9- ←
DB4_5+ ← DB4_5+
DB4_5- ←
DB0_1+ ← DB0_1+
DB0_1- ←
OF+ ← OF+
OF- ←

J1D — SEAM-10X40PIN

CLKOUT+ ← CLKOUT+
CLKOUT- ← CLKOUT-

J1C — SEAM-10X40PIN

CS — R40 1K — C35 47pF
SDO — R41 1K — C36 47pF
SDI — R42 1K — C37 47pF
SCK — R43 1K — C38 47pF

J1A — SEAM-10X40PIN
J1B — SEAM-10X40PIN
J1F — SEAM-10X40PIN
J1E — SEAM-10X40PIN
J1J — SEAM-10X40PIN
J1K — SEAM-10X40PIN

VDD

U5 24LC32A
C54 0.1uF
R25 4.99K R24 4.99K R18 4.99K
SCL SDA WP A2 A1 A0
VCC VSS

JP2 EEPROM
1 WP
2
3 PROG

APPROVALS
PCB DES. M.HAWKINS
APP ENG. C.MAYOTT

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TITLE: SCHEMATIC

LTC2158 AND LTC6430 COMBO BOARD

SIZE N/A | IC NO. LTC2158CUP-14, LTC6430AIUF-15 | REV. 3

DEMO CIRCUIT 1946A

SCALE = NONE | DATE: 10/18/2013 | SHEET 2 OF 3

TRANSFORMER PART OPTION FOR T1 AND T2

T4
T1_5 — 6 T1_1
2 — 5 T1_2
T1_4 — 4 T1_3
MINI-CIRCUITS, ADT2L-18+

T5
T2_5 — 6 T2_1
2 — 5 T2_2
T2_4 — 4 T2_3
MINI-CIRCUITS, ADT2L-18+

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APPROVALS	
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TITLE: SCHEMATIC
LTC2158 AND LTC6430 COMBO BOARD

SIZE	IC NO. LTC2158CUP-14, LTC6430AIUF-15	REV.
N/A	**DEMO CIRCUIT 1946A**	3

DATE: 10/18/2013 | SHEET 3 OF 3

DEMO MANUAL DC1946A

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