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LTC2270
16-Bit, 20Msps Dual ADC

DESCRIPTION

Demonstration circuit 1975A supports the LTC®2270 high speed, high dynamic range ADC. It was specially designed for applications that require differential DC inputs. DC1975 supports the LTC2270 in CMOS output mode.

The circuitry on the analog inputs is optimized for analog input frequencies from DC to 70MHz. Refer to the data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at http://www.linear.com/demo/DC1975A

DC1975 VARIANTS

DC1975 VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
1975A-A	LTC2270	16-Bit	20Msps	DC to 70MHz

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage: DC1975A	Depending on Sampling Rate and the A/D Converter Provided, This Supply Must Provide Up to 300mA	4.5		6	V
Analog Input Range	Depending on SENSE Pin Voltage	1		2.1	V_{P-P}
Logic Input Voltages	Minimum Logic High Maximum Logic Low		1.3 0.6		V V
Sampling Frequency (Convert Clock Frequency)		1		20	Msps
Convert Clock Level	Single-Ended Encode Mode (ENC– Tied to GND)	0		3.6	V
Convert Clock Level	Differential Encode Mode (ENC– Not Tied to GND)	0.2		3.6	V
Resolution			16		
Input Frequency Range		DC		70	MHz

QUICK START PROCEDURE

DC1975A is easy to set up to evaluate the performance of the LTC2270 A/D converter. Refer to Figure 1 for proper measurement equipment setup and follow the procedure in the Setup section.

SETUP

The DC890 USB demonstration circuit was supplied with the DC1975 demonstration circuit. Follow the DC890 Quick Start Guide to install the required software and for connecting the DC890 to the DC1975 and to a PC.

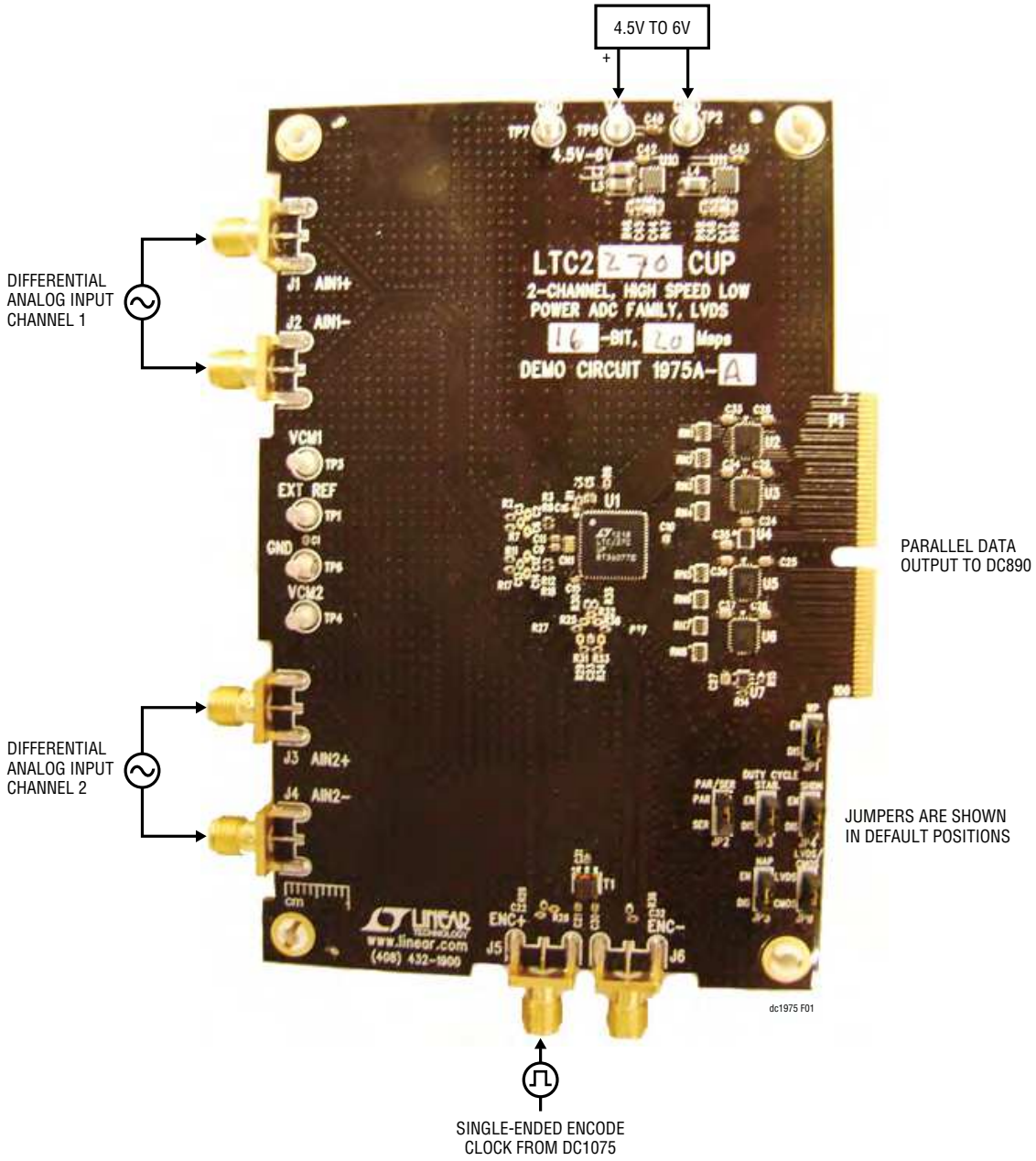

Figure 1. DC1975A Setup

HARDWARE SETUP

SMAs:

J1 AIN1+ and J2 AIN1–: Differential Inputs for Channel 1. Apply a differential signal to these SMA connectors from a differential driver. There are 50Ω resistors at the end of each transmission line that serve as termination for the differential driver. These SMAs are positioned 0.8" apart to accommodate LTC differential driver boards.

J3 AIN2+ and J4 AIN2–: Differential Inputs for Channel 2. Apply a differential signal to these SMA connectors from a differential driver. There are 50Ω resistors at the end of each transmission lines that serve as termination for the differential driver. These SMAs are positioned 0.8" apart to accommodate LTC differential driver boards.

J5 ENC+: Positive Encode Clock Input. As a default the demo board is populated to accept a single-ended clock input from a DC1075A demo board, or an equivalent CMOS signal. For other population options see the Encode Clock section of this manual.

J6 ENC–: Negative Encode Clock Input. As a default this input port is grounded to accommodate the single ended clock drive. For other population options see the Encode clock section of this manual.

TURRETS:

V+ (TP5): Positive Input Voltage for the ADC and Digital Buffers. This voltage feeds a regulator that supplies the proper voltages for the ADC and buffers. The voltage range for this turret is 4.5V up to 6V.

EXT REF (TP1): Optional Reference Programming Voltage. This pin is connected directly to the SENSE pin of the ADC. If no external voltage is supplied this pin will be pulled to VDD through a weak pull-up resistor. This will select the ±1V input range. Connect to GND to select the ±0.5V input range, an external reference between 0.625V and 1.3V will select an input range of ±0.8 • V_{SENSE}.

GND (TP2, TP6, TP7): Ground Connection. This demo board only has a single ground plane. One of these turrets should be tied to the GND terminal of the power supply being used. Extra GND pins are available for convenience when probing.

VCM1 (TP3): Common-Mode Voltage for Channel 1. This turret provides the common-mode voltage from the ADC for channel 1. It is meant to be used to bias the common-mode bias pin of the differential driver.

VCM2 (TP4): Common-Mode Voltage for Channel 2. This turret provides the common-mode voltage from the ADC for channel 2. It is meant to be used to bias the common-mode bias pin of the differential driver.

JUMPERS:

The DC1975A demonstration circuit board should have the following jumper settings as default positions (as per Figure 1) which configures the ADC in serial programming mode. In the default configuration JP3-JP6 should be left in the default locations. This will pull those pins high through weak pull-up resistors so that the SPI commands can be sent from the PC. When JP2 is set to PAR, then jumpers JP3-JP6 can be configured manually.

JP1 WP: EEPROM Write Protect. For factory use only. Should be left in the enable (EN) position.

JP2 PAR/SER: Selects Parallel or Serial Programming Mode. (Default: serial)

JP3 Duty Cycle Stab: In parallel programming mode enables or disables duty cycle stabilizer. In serial programming mode, pull up to VDD. (Default: Enable or pull up)

JP4 SHDN: In parallel programming mode enables or disables LTC2270. In serial programming mode, pull up to VDD. (Default: Enable or pull up)

JP5 NAP: In parallel programming mode enables or disables NAP mode. In serial programming mode, pull up to V_{DD}. (Default: Enable or pull up)

JP6 LVDS/CMOS: In parallel programming mode selects between LVDS or CMOS output signaling. In serial programming mode, pull up to VDD. (Default: LVDS or pull up). Note: In parallel mode CMOS mode must be selected. LVDS mode not supported on the DC1975 demo board.

APPLYING POWER & SIGNALS TO THE DC1975 DEMONSTRATION CIRCUIT

If a DC890 is used to acquire data from the DC1975, the DC890 must FIRST be connected to a powered USB port or provided an external 6V to 9V BEFORE applying 4.5V to 6V across the pins marked V+ and GND on the DC1975. DC1975 requires 4.5V for proper operation. Regulators on the board produce the voltages required for the ADC. The DC1975 demonstration circuit requires up to 300mA depending on the sampling rate and the A/D converter supplied.

The DC890 data collection board is powered by the USB cable and does require an external power supply when collecting data from an LVDS demo board. It must be supplied an external 6V to 9V on turrets G7(+) and G1(–) or the adjacent 2.1mm power jack.

ANALOG INPUT NETWORK

In the default setup both of the inputs are brought out to SMA connectors so the demo board can be driven with a differential source. The DC1975 is populated with no filtering between the input SMAs and the ADC. There are provisions for a custom filter to be designed and installed between the off board driver and ADC.

A common-mode voltage is provided on turrets TP3 and TP4 that can be used to bias the driver. If the driver is supplying the common-mode voltage R10 and R20 should be removed, and the common-mode voltage from the driver can be connected on turrets TP3 and TP4.

In almost all cases, off-board filters will be required on the analog inputs of the differential driver boards to achieve data sheet SNR.

The off-board filters should be located close to the inputs of the differential driver board to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

Apply the analog input signal of interest to the SMA connectors on the DC1975 demonstration circuit board marked J1-J4.

ENCODE CLOCK

Apply an encode clock to the SMA connector on the DC1975A demonstration circuit board marked J5. As a default, the DC1975A is populated to have a single-ended input.

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter, square wave source. The amplitude should be large, up to $3V_{P-P}$ or 13dBm. When using a sinusoidal signal generator, a squaring circuit can be used. Linear Technology also provides DC1075A, a demo board that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTC2270.

Using a bandpass filter on the clock will improve the noise performance by reducing the wideband noise power of the signal. In the case of the DC1975, a bandpass filter used for the clock should be used prior to the DC1075A. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, nonharmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used with TTE bandpass filters for both the clock input and the analog inputs.

An internally generated conversion clock output is available on P1, which could be collected via a logic analyzer, or other data collection system if populated with a SAMTEC MEC8-150 type connector or collected by the DC890 QuikEval™ II data acquisition board using PScope™ software.

CLOCK NETWORK

The clock network on the DC1975 can support a variety of clock inputs. As a default it is populated to accept a single ended square wave clock from a DC1075 or appropriate signal generator. This will drive the ENC+ pin single ended and the ENC– pin on the ADC is tied to GND.

When using a single-ended sine wave generator to drive the encode input of the ADC, it is best to use a single-ended-to-differential translation circuit. To modify the DC1975 to accommodate this first move the 0Ω resistor populated in position R26 to position R28, and move R27 and R37 to the R29 and R34 locations. This will direct the signal through the transformer T1 which will do the single ended to differential translation.

When using a PECL or LVDS clock you can drive the DC1975 differentially through J5 and J6. From the default population, remove the 0ohm resistor in the C32 position and add the appropriate termination for your clock signal. R24, R25, R32, R38 and R39 are available to provide the proper termination for LVDS, PECL, or CML signaling. Blocking capacitors can be installed in the R30 and R35 positions if the common-mode voltage of the clock is not compatible with the LTC2270.

SOFTWARE

The DC890 is controlled by the PScope system software provided or downloaded from the Linear Technology website at http://www.linear.com/software/. If a DC890 was provided, follow the DC890 Quick Start Guide and the instructions below.

To start the data collection software if PScope.exe is installed (by default) in \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1975 demonstration circuit is properly connected to the DC890, PScope should automatically detect the DC1975A, and configure itself accordingly. If necessary, the following procedure explains how to manually configure PScope.

Under the Configure menu, go to ADC Configuration. Check the Config Manually box and use the following configuration options (see Figure 2).

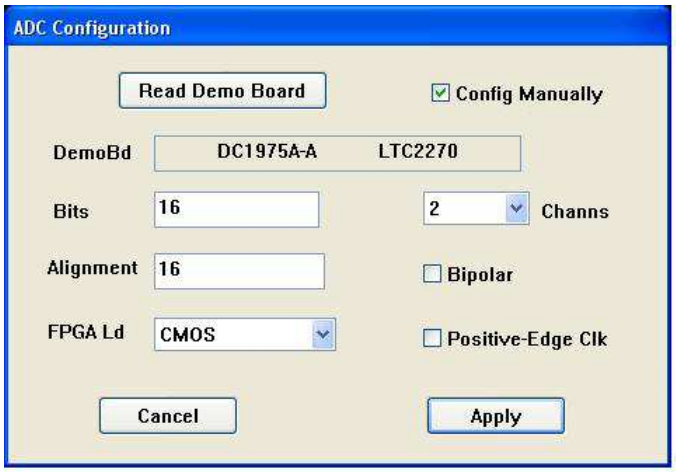

Figure 2. ADC Configuration

Manual Configuration Settings:

Bits: 16

Alignment: 16

FPGA Ld: CMOS

Channs: 2

Bipolar: Unchecked

Positive-Edge Clk: Unchecked

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the Collect button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC890 Quick Start Guide and in the online help available within the PScope program itself.

SERIAL PROGRAMMING

PScope has the ability to program the DC1975 board serially through the DC890. There are several options available in the LTC2270 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the Set Demo Bd Options icon on the PScope toolbar (Figure 3).

This will bring up the menu shown in Figure 4.

Figure 3. PScope Toolbar

SOFTWARE

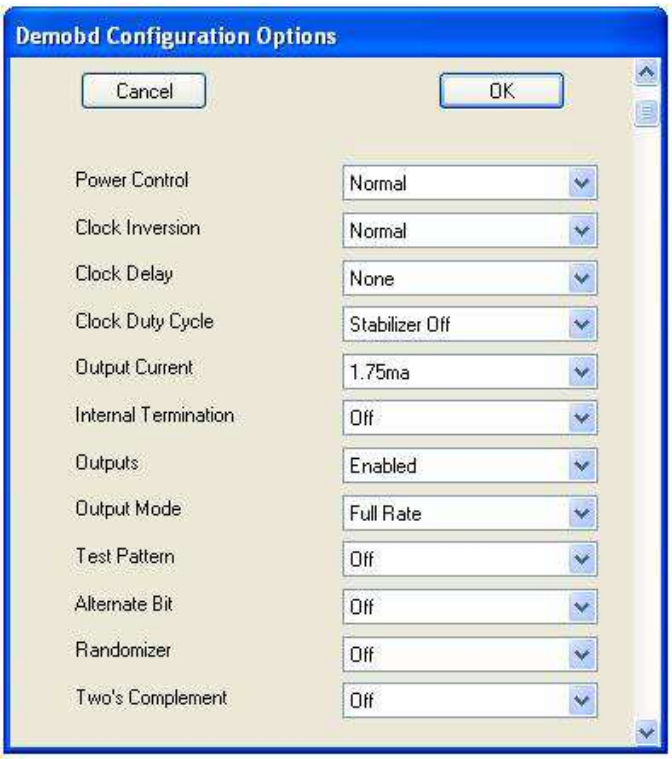

Figure 4. Demobd Configuration Options

This menu allows any of the options available for the LTC2270 family to be programmed serially. The LTC2270 family has the following options:

Power Control: Selects between normal operation, nap and sleep modes

- Normal (default): Entire ADC is powered and active
- Ch1 Normal Ch2 Nap: Channel 1 remains active while channel 2 is put into nap mode
- Nap: ADC core powers down while references stay active
- Shutdown: The entire ADC is powered down

Clock Inversion: Selects the polarity of the CLKOUT signal

- Normal (default): Normal CLKOUT polarity
- Inverted: CLKOUT polarity is inverted

Clock Delay: Selects the phase delay of the CLKOUT signal

- None (default): No CLKOUT delay
- 45 Deg: CLKOUT delayed by 45 degrees
- 90 Deg: CLKOUT delayed by 90 degrees
- 135 Deg: CLKOUT delayed by 135 degrees

Clock Duty Cycle: Enable or disables duty cycle stabilizer

- Stabilizer off (default): Duty cycle stabilizer disabled
- Stabilizer on: Duty cycle stabilizer enabled

Output Current: Selects the LVDS output drive current. (Not supported by DC1975A)

- 1.75mA (default): LVDS output driver current
- 2.1mA: LVDS output driver current
- 2.5mA: LVDS output driver current
- 3mA: LVDS output driver current
- 3.5mA: LVDS output driver current
- 4mA: LVDS output driver current
- 4.5mA: LVDS output driver current

Internal Termination: Enables LVDS internal termination. (Not supported by DC1975A)

- Off (default): Disables internal termination
- On: Enables internal termination

Outputs: Enables Digital Outputs

- Enabled (default): Enables digital outputs
- Disabled: Disables digital outputs

Output Mode: Selects digital output mode

- Full Rate (default): Full rate CMOS output mode.
- Double LVDS: Double data rate LVDS output mode. (This mode is not supported by the DC1975A)
- Double CMOS: Double data rate CMOS output mode. (This mode is not supported by the DC1975A)

SOFTWARE

Test Pattern: Selects digital output test patterns

- Off (default): ADC data presented at output
- All Out =1: All digital outputs are 1
- All Out = 0: All digital outputs are 0
- Checkerboard: OF and D13-D0 alternate between 101 0101 1010 0101 and 010 1010 0101 1010 on alternating samples
- Alternating: Digital outputs alternate between all 1's and all 0's on alternating samples

Alternate Bit: Alternate bit polarity (ABP) mode

- Off (default): Disables alternate bit polarity
- On: Enables alternate bit polarity. Before enabling ABP, be sure the part is in offset binary mode

Randomizer: Enables data output randomizer

- Off (default): Disables data output randomizer
- On: Enables data output randomizer

Two's complement: Enables two's complement mode

- Off (default): Selects offset binary mode
- On: Selects two's complement mode

Once the desired settings are selected, hit OK and PScope will automatically update the register of the device on the DC1975A demo board.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CN1	CAP, X5R, ARRAY, 2.2µF, 20%, 4V, 0508	AVX, W2L14D225MAT1A
2	2	C1, C5	CAP, 0402 2.2µF, 20%, 6.3V, X5R	TAIYO YUDEN, JMK105BJ225MV-F
3	0	C2, C3, C6, C12, C13, C14, C22,	CAP, 0402	OPT
4	5	C4, C8, C9, C11, C18	CAP, 0402, 1µF, 10%, 16V, X6S	TDK, C1005X6S1C105K
5	6	C7, C10, C15, C16, C17, C19	CAP, 0402, 0.01µF, 10%, 16V, X7R	AVX, 0402YC103KAT2A
6	5	C20, C21, C23, C30, C31	CAP, 0402, 0.1µF, 10%, 10V, X5R	TDK, C1005X5R1A104K
7	12	C24-C29, C33-C38	CAP, 0603, 0.1µF, 10%, 50V, X7R	TDK, C1608X7R1H104K
8	3	C39, C40, C41	CAP, 0603, 22pF, 5%, 16V, NPO	AVX, 0603YA220JAT2A
9	1	C42	CAP, 0603, 4.7µF, 20%, 6.3V, X5R	TDK, C1608X5R0J475MT
10	4	C43, C45, C46, C48	CAP, 0603, 1µF, 10%, 16V, X7R	TDK, C1608X7R1C105K
11	2	C44, C47	CAP, 0805, 10µF, 10%, 16V, X5R	MURATA, GRM21BR61C106KE15L

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
12	6	JP1, JP2, JP3, JP4, JP5, JP6	HEADER, 3-PIN, 2mm	SULLIN, NRPN031PAEN-RC
13	6	J1-J6	CONN, SMA 50Ω EDGE-LAUNCH	E.F.JOHNSON, 142-0701-851
14	0	L1	IND, 0603, BEAD	TBD
15	3	L2, L3, L4	FERRITE BEAD, 1206	MURATA, BLM31PG330SN1L
16	9	RN1-RN9	RES, THICK FILM ARRAY, 33Ω	VISHAY, CRA04S08333R0JTD
17	1	R1	RES, 0402, 1kΩ, 5%, 1/16W	VISHAY, CRCW04021K00JNED
18	15	R2, R3, R7, R8, R11, R12, R17, R18, R26, R27, R30, R35, R36, R37, C32	RES, 0402, 0Ω, JUMPER	NIC, NRC04ZOTRF
19	10	R4, R5, R9, R10, R13, R16, R19, R20, R31, R33	RES, 0402, 49.9Ω, 1%, 1/16W	NIC, NRC04F49R9TRF
20	3	R6, R24, R39	RES, 0402, 100Ω, 1%, 1/16W	NIC, NRC04F1000TRF
21	4	R14, R21, R22, R23	RES, 0402, 4.99kΩ, 1%, 1/16W	NIC, NRC04F4991TRF
22	1	R15	RES, 0402, 100kΩ, 5%, 1/16W	NIC, NRC04J104TRF
23	0	R25, R28, R29, R32, R34, R38	RES, 0402	OPT
24	1	R40	RES, 0603, 10kΩ, 5%, 1/10W	NIC, NRC06J103TRF
25	5	R41, R42, R43, R44, R45	RES, 0603, 1kΩ, 5%, 1/10W	VISHAY, CRCW06031K00JNED
26	2	R46, R48	RES, 0603, 3kΩ, 1%, 1/10W	VISHAY, CRCW06033K00FKEA
27	1	R47	RES, 0603, 180kΩ, 1%, 1/10W	VISHAY, CRCW0603180KFKED
28	1	R49	RES, 0603, 330kΩ, 1%, 1/10W	VISHAY, CRCW0603330KFKEA
29	7	TP1-TP7	TP, TURRETS, 0.094"	MILL-MAX, 2501-2-00-80-00-00-07-0
30	1	T1	XFMR, 1:1, TRANS-MABA-007159	MACOM, MABA-007159-000000
31	1	U1	IC, LTC2270CUP, QFN64UP-9×9	LINEAR TECHNOLOGY, LTC2270CUP
32	4	U2, U3, U5, U6	IC, 8-BIT DUAL VOLTAGE SUPPLY TRANSLATOR, MICROPAK-10	FAIRCHILD SEMI., FXLH42245MPX
33	1	U4	IC, 2-BIT DUAL VOLTAGE SUPPLY TRANSLATOR, MICROPAK-10	FAIRCHILD SEMI., FXL2T245L10X
34	1	U7	IC, ULP INVERTER, SC70-5	FAIRCHILD SEMI., NC7SP14P5X
35	1	U8	IC, EEPROM, TSSOP8	MICROCHIP TECH., 24LC025-I/ST
36	1	U9	IC, 8-BIT I/0 EXPANDER, SSOP20G	NXP, PCF8574TS/3
37	2	U10, U11	IC, SINGLE RESISTOR LOW DROPOUT REGULATOR, DFN8DD	LINEAR TECHNOLOGY, LT3080EDD
38	6	SHUNTS FOR JP1-JP6	SHUNT, 2mm	SAMTEC, 2SN-BK-G
39	4	STANDOFF, SNAP-ON		KEYSTONE, 8831
40	2	STENCILS FOR BOTH SIDES		DC1975A-1

SCHEMATIC DIAGRAM

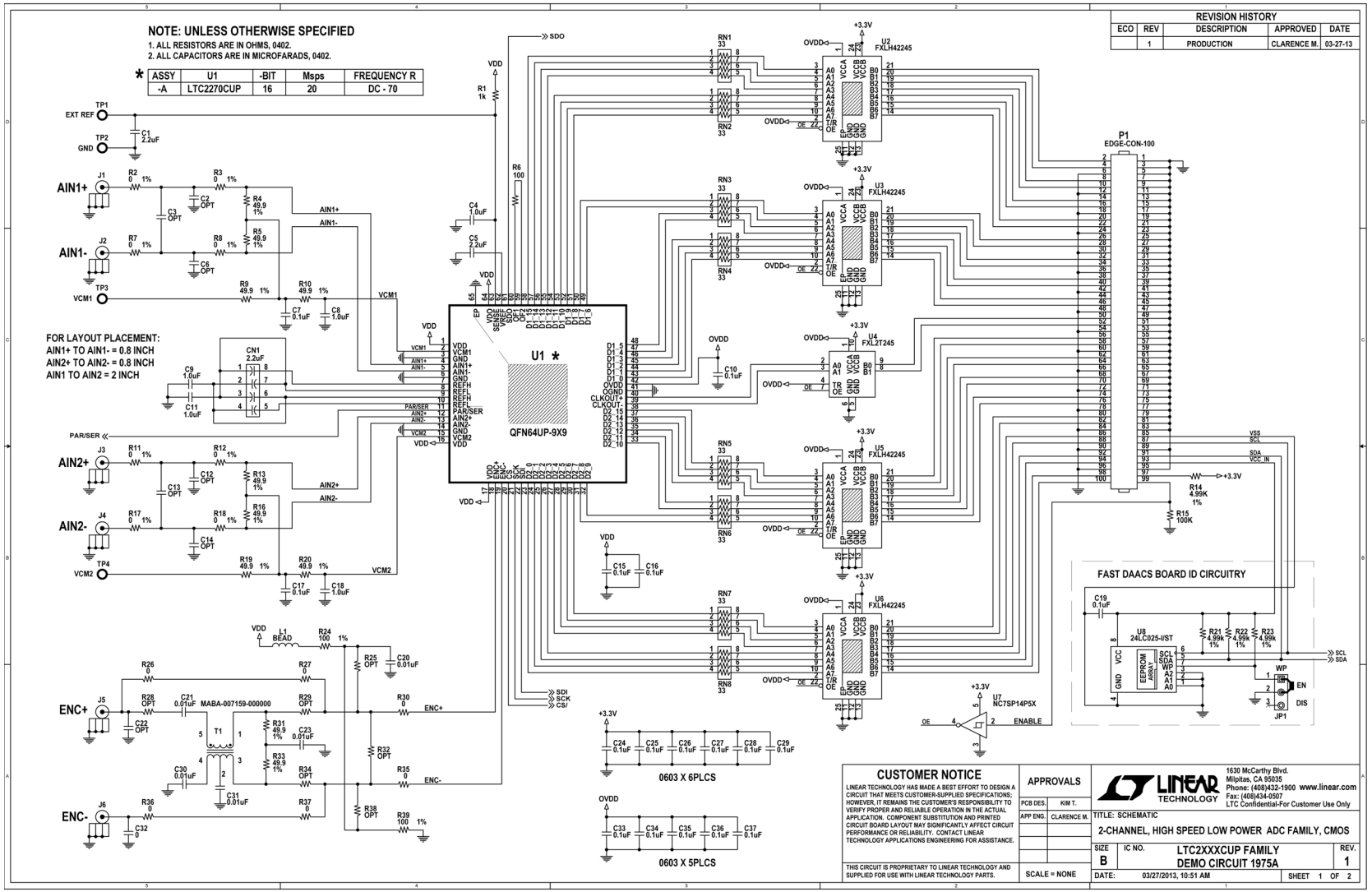

Figure 5. 2-Channel, High Speed, Low Power ADC Family, LVDS

SCHEMATIC DIAGRAM

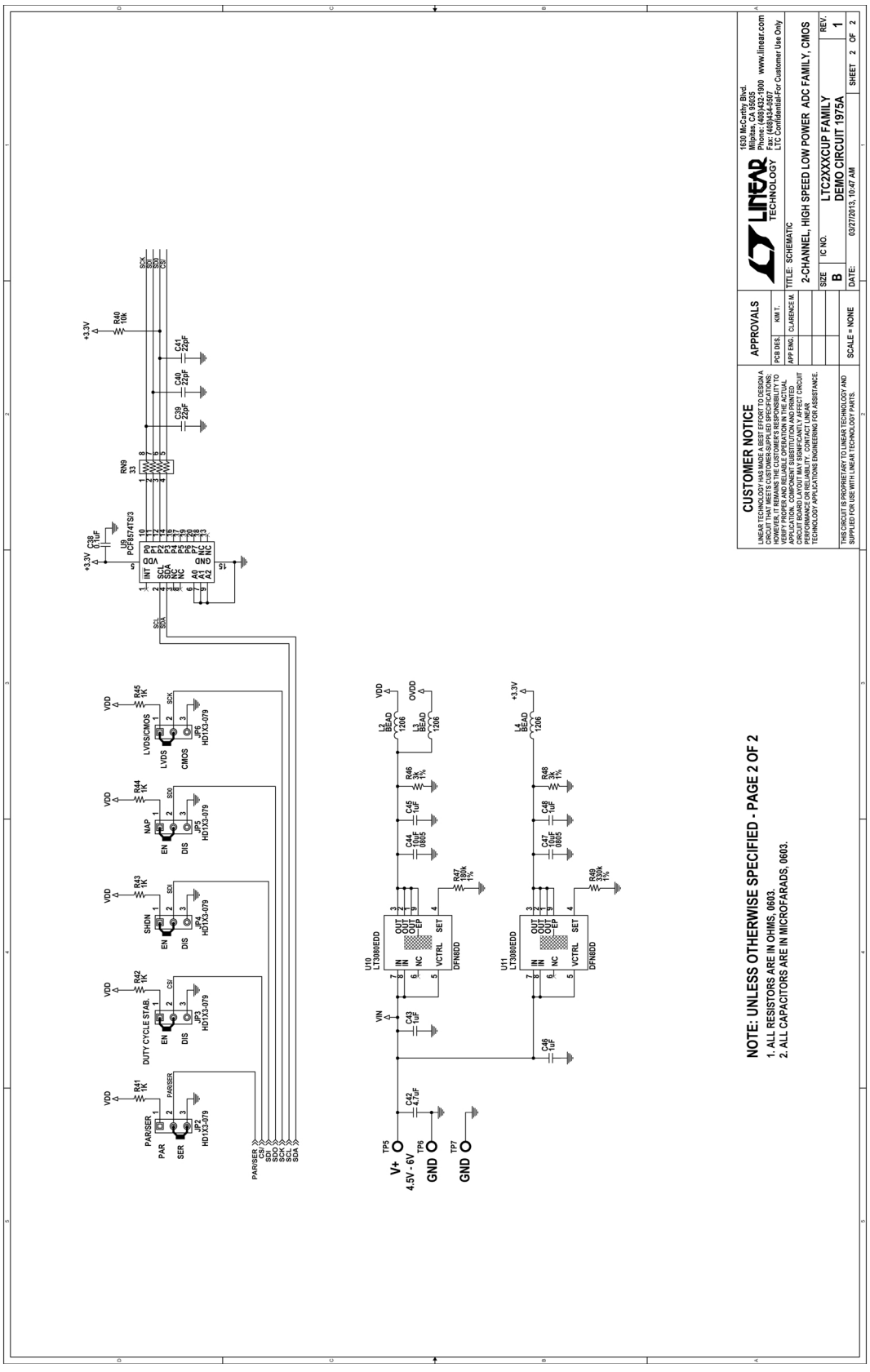

Figure 6. 2-Channel, High Speed, Low Power ADC Family, LVDS

DEMONSTRATION BOARD IMPORTANT NOTICE

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If this evaluation kit does not meet the specifications recited in the DEMO BOARD manual the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY THE SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THIS INDEMNITY, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

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Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged**.

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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