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16-Channel 16-Bit/12-Bit ±10V V_{OUT} SoftSpan DACs with 10ppm/°C Max Reference

DESCRIPTION

Demonstration circuit 2025A features the LTC2668, 16-channel 16-Bit/12-Bit ±10V V_{OUT} SoftSpan™ DACs with 10ppm/°C max reference in a 6mm × 6mm QFN package. This device features per-channel SoftSpan configuration with five output ranges: 0V to 5V, 0V to 10V, ±2.5V, ±5V, and ±10V. A toggle feature allows any or all DACs to switch between two programmed codes via a single SPI command or by the TGP input pin. The versatile SPI interface can operate on any logic level between 1.71V and 5.5V, for easy interface to lower voltage microcontrollers or FPGAs.

DC2025A-A is populated with the 16-bit version of the LTC2668. DC2025A-B is populated with the 12-bit version for lower resolution applications.

Design files for this circuit board are available at http://www.linear.com/demo/DC2025A

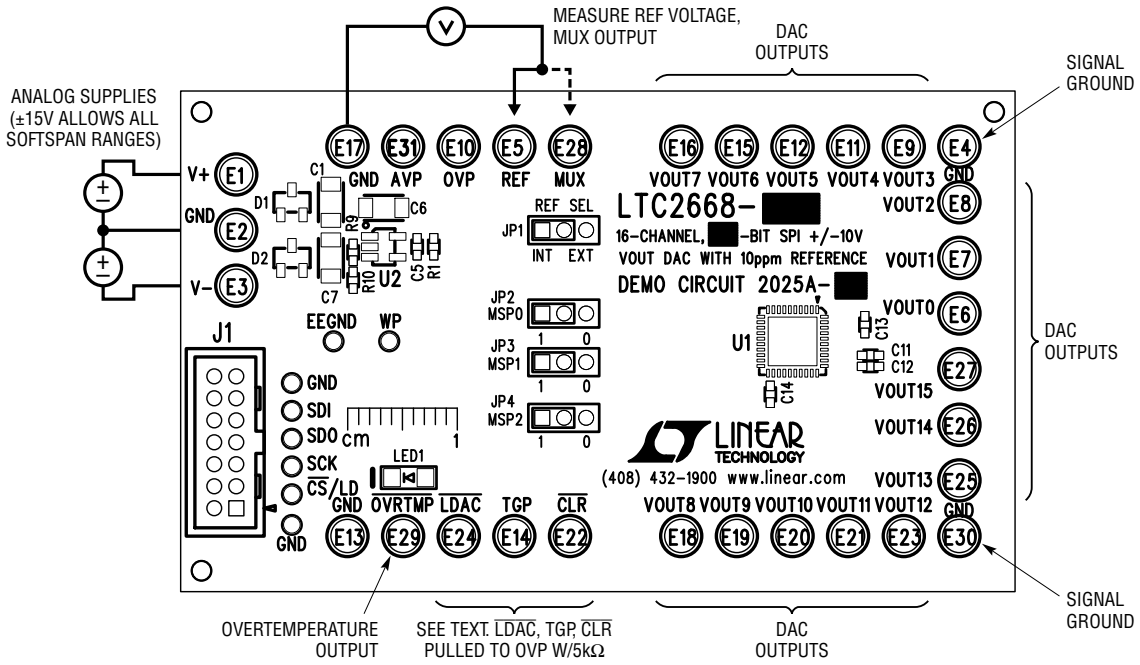


Figure 1. Connection Diagram

QUICK START PROCEDURE

Download and install QuikEval™ from:

http://www.linear.com/designtools/software/#Data

Connect a DC590 controller or DC2026 Linduino with DC590 emulator firmware to the DC2025A with the supplied ribbon cable. Connect low-noise analog power supplies as shown in Figure 1. A ±15V supply will allow all of the SoftSpan ranges to be used, refer to the LTC2668 data sheet for other supply options if not all SoftSpan ranges are used.

Connect the controller to the host PC's USB port and run QuikEval. The DC2025A software will be downloaded and installed, after which a jumper setting window will appear as shown in Figure 2. The default settings are internal reference, SoftSpan operation with 0V to 5V range, 0V output on power-up. If the jumpers on the board have been changed to a different configuration, select the appropriate options in the pull-down menus to match the board.

Click OK and the main dialog will appear. The control panel gives access to all of the LTC2668's functionality including per-channel SoftSpan ranges, toggling, Power-Down, etc. Detailed instructions are provided in the Help menu.

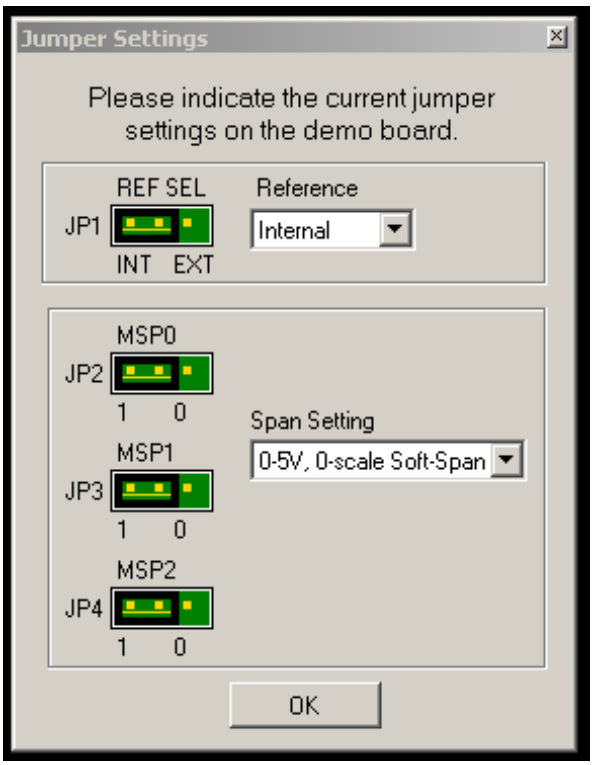


Figure 2. Jumper Settings Dialog

QUICK START PROCEDURE

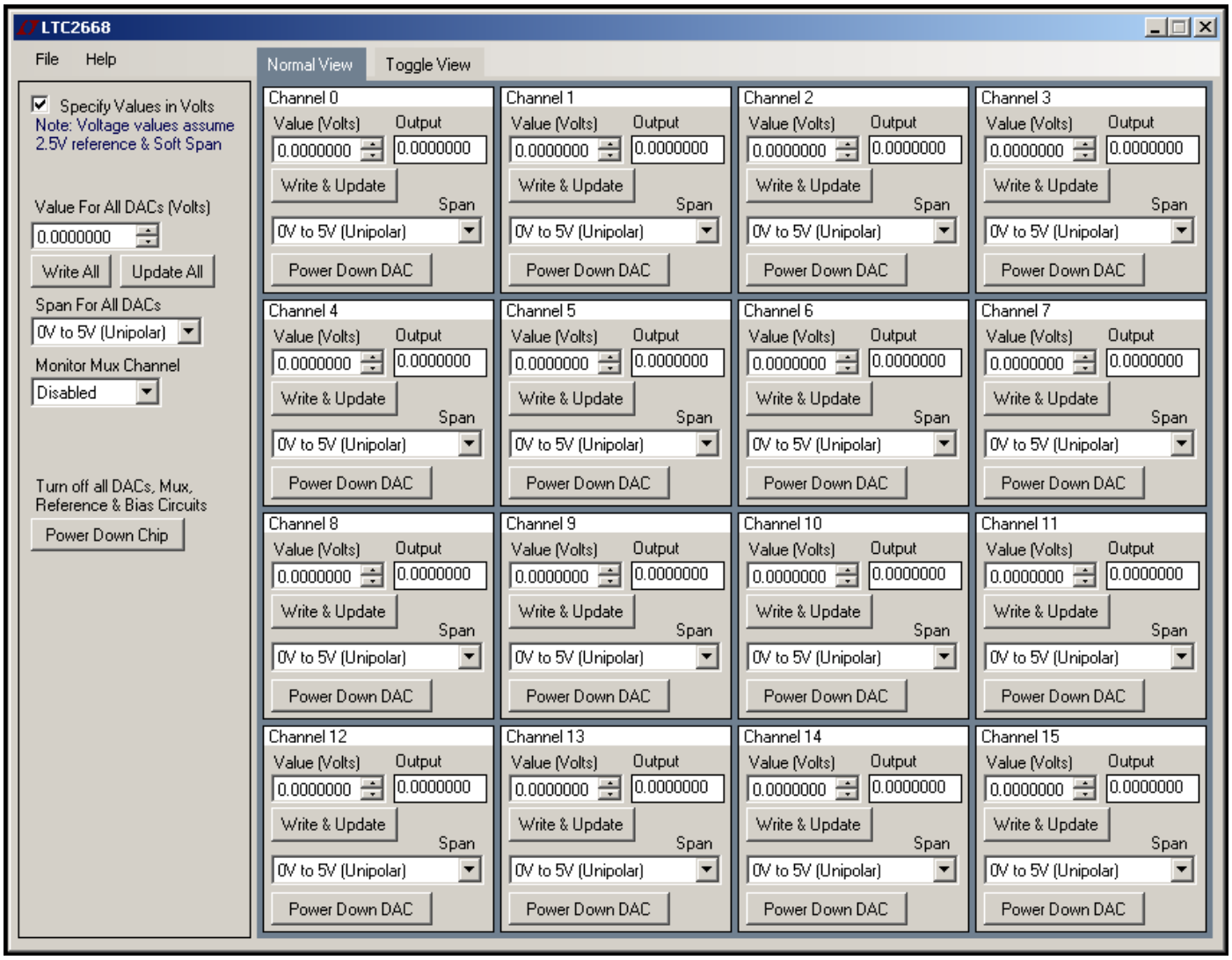


Figure 3. Main Control Panel

QUICK START PROCEDURE

External Connections

J1: Interface connector to DC590 controller or Linduino. Provides OVP power, SPI interface, and board identification.

V^-, GND, V^+: Analog supplies, connected to the LTC2668 V^+ and V^- pins. Nominally ±15V for operation in all SoftSpan ranges. Refer to the data sheet for other supply configurations.

GND: Four additional ground posts and exposed ground plane around board edge allow solid connection to prototype circuitry and measurement equipment.

AVP: Analog supply voltage. Normally supplied by an onboard LT1761-5 fixed 5V regulator that is powered from the V^+ supply. For single 5V supply applications, AVP may be tied directly to V^+ and supplied with 4.5V to 5.5V.

OVP: Digital interface power. No connection to this pin is required when used with a DC590 or Linduino controller. If another controller is used, connect to digital supply that powers the SPI bus controller (1.71 to 5.5V).

REF: Connection to the REF pin. In internal reference mode, the reference voltage may be monitored at this point. Placing REF_SEL jumper in the EXT position allows an external reference to be connected to this point.

MUX: Monitor Mux output. Allows surveying the DAC outputs under software control. Must be measured with a high impedance meter (output impedance is nominally 2.1kΩ).

VOUT0 to VOUT15: DAC outputs.

$\overline{\text{CLR}}$: Asynchronous clear input (pulled high to OVP with a 4.99k resistor). Pull to ground to reset the DAC to the power-on reset value (determined by MSPx pins.)

TGP: Toggle input (pulled high to OVP with a 4.99k resistor). A high level on this pin enables software toggling. See data sheet for a complete description of toggle operation.

$\overline{\text{LDAC}}$: Asynchronous DAC update. If $\overline{\text{CS}}$/LD is high at the falling edge of $\overline{\text{LDAC}}$, DAC outputs will be updated with the contents of the input registers. If $\overline{\text{CS}}$/LD is low when $\overline{\text{LDAC}}$ goes low, the DAC registers are updated after $\overline{\text{CS}}$/LD returns high.

$\overline{\text{OVRTMP}}$: Overtemperature pin (pulled high to OVP with a 4.99k resistor). The LTC2668 pulls this pin low if the die temperature exceeds approximately 160°C. It is released on the next rising edge of $\overline{\text{CS}}$/LD.

QUICK START PROCEDURE

Jumpers

REF_SEL (JP1): Selects internal or external reference mode. (See data sheet description of REFCOMP pin.)

MSP0, MSP1, MSP2 (JP2, JP3, JP4): Manual Span control. Setting all jumpers to the 1 position (Default) selects SoftSpan operation, with a power-up default span of 0V to 5V, and reset to Zero-Scale. Other options are listed in Table 1.

LEDs

OVRTMP: Lights when $\overline{\text{OVRTMP}}$ pin asserts, indicating an overtemperature state. (Note that LED will light if positive analog supply is present and OVP is not. OVP is normally supplied by the controller.)

Test Points

The SPI bus is available on a row of through-hole test points next to J1 that may be used to monitor the bus or to drive the bus with an external controller.

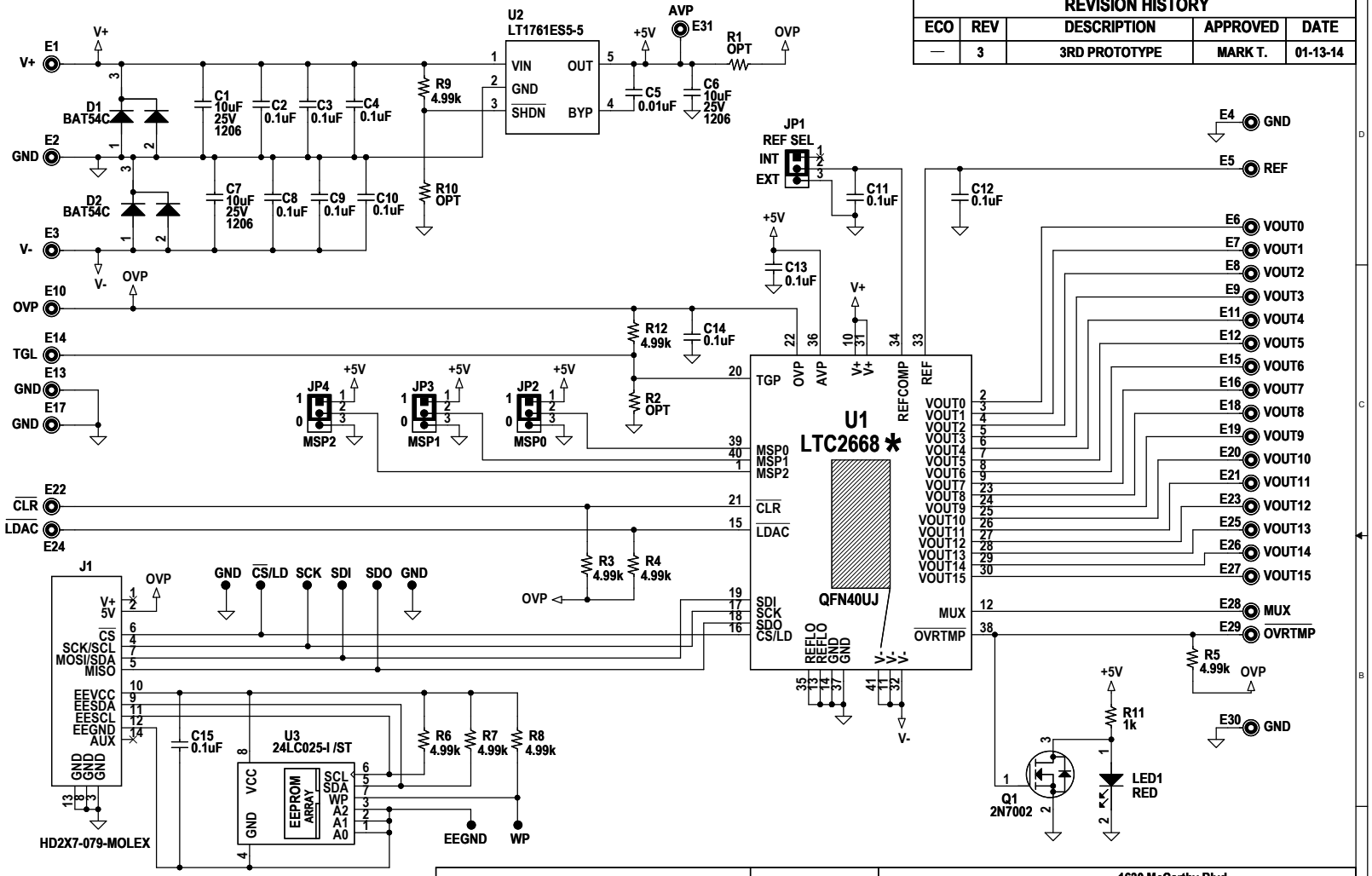
EEGND, WP: For factory use only.

Table 1

MSP2	MSP1	MSP0	OUTPUT RANGE	RESET CODE	MANUAL SPAN	SoftSpan
0	0	0	±10V	Mid-Scale	X	
0	0	1	±5V	Mid-Scale	X	
0	1	0	±2.5V	Mid-Scale	X	
0	1	1	0V to 10V	Zero-Scale	X	
1	0	0	0V to 10V	Mid-Scale	X	
1	0	1	0V to 5V	Zero-Scale	X	
1	1	0	0V to 5V	Mid-Scale	X	
1	1	1	0V to 5V	Zero-Scale		X

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	3	C1, C6, C7	CAP., X5R, 10µF 25V, 10%, 1206	MURATA, GRM31CR61E106KA12L
2	11	C2, C3, C4, C8-C15	CAP., X7R, 0.1µF 25V, 10%, 0603	MURATA, GRM188R71E104KA01D
3	1	C5	CAP., X7R, 0.01µF 25V, 10%, 0603	MURATA, GRM188R71E103KA01D
4	2	D1, D2	DIODE, SCHOTTKY DUAL 30V, SOT23-3	DIODES INC., BAT54C-7-F
5	31	E1-E31	TURRET, TESTPOINT 0.064"	MILL-MAX, 2308-2-00-80-00-00-07-0
6	4	JP1, JP2, JP3, JP4	HEADER, 2mm SINGLE STR 3POS	SULLINS, NRPN031PAEN-RC
7	1	J1	CONN., HEADER 14POS 2mm VERT GOLD	MOLEX, 87831-1420
8	1	LED1	LED, RED, LED-ROHM-SML-010VT	ROHM, SML-010VTT86L
9	1	Q1	MOSFET, N-CH 60V 300mA SOT-23	VISHAY SILICONIX, 2N7002K-T1-E3
10	0	R1, R2, R10	RES., 0603	OPT
11	8	R3, R4, R5, R6, R7, R8, R9, R12	RES., CHIP, 4.99k, 1/10W, 1% 0603	VISHAY, CRCW06034K99FKEA
12	1	R11	RES., CHIP, 1k, 1/10W, 1% 0603	VISHAY, CRCW06031K00FKEA
13	1	U2	I.C., LT1761ES5-5, SOT23-5	LINEAR TECH., LT1761ES5-5#PBF
14	1	U3	I.C., 24LC025-I/ST, TSSOP8	MICROCHIP, 24LC025-I/ST
DC2025A-A Required Circuit Components				
15	1	U1	I.C., 16-BIT, QFN40UJ-6X6	LINEAR TECH., LTC2668CUJ-16#PBF
DC2025A-B Required Circuit Components				
15	1	U1	I.C., 12-BIT, QFN40UJ-6X6	LINEAR TECH., LTC2668CUJ-12#PBF



NOTE: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITORS ARE IN MICROFARADS, 0603.

*	ASSY	U1	SUFFIX	-Bit
	A	LTC2668-16	16	16
	B	LTC2668-12	12	12

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APPROVALS

PCB DES.	KIM T.
APP ENG.	MARK T.

SCALE = NONE

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TITLE: SCHEMATIC **16-CHANNEL, 16/12-BIT SPI +/-10V VOUT DAC WITH 10ppm REFERENCE**

SIZE	IC NO.	REV.
N/A	LTC2668CUJ - 16 / 12 DEMO CIRCUIT 2025A	3

DATE: 01/13/2014, 12:06 PM SHEET 1 OF 1

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