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LTC2107
16-BIT, 210 Msps ADCs

DESCRIPTION

Demonstration circuit 2183A supports the LTC®2107, a high speed and high dynamic range ADC. It was specially designed for applications that require a single-ended AC-coupled input. DC2183 supports the LTC2107 using the DDR LVDS output mode.

The LTC2107 characteristics are listed in Table 1. Depending on the version, the circuitry on the analog inputs is optimized for analog input frequencies from 5MHz to 70MHz or 70MHz to 180MHz.

Refer to the LTC2107 data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at http://www.linear.com/demo/DC2183A

Table 1: DC2183 Variants

DC2183 VARIANTS	ADC PART NUMBER	RESOLUTION	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
2183A-A	LTC2107	16-BIT	210 Msps	5MHz to 70MHz
2183A-B	LTC2107	16-BIT	210 Msps	70MHz to 180MHz

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage – DC2183	This supply must provide up to 800mA.	3.3		5.0	V
Analog Input Range	Depending on PGA setting	1.6		2.4	V_{P-P}
Logic Input Voltages	Minimum Logic High	1.2			V
	Maximum Logic Low			0.6	V
Logic Output Voltages (Differential)	Nominal Logic Levels (100Ω load, 3.5mA Mode, 1.25V common mode)	0.350			V
	Minimum Logic Levels (100Ω load, 3.5mA Mode, 1.25V common mode)	0.247			V
Sampling Frequency (Encode Clock Frequency)		10		210	MHz
Convert Clock Level (Single Ended)	Logic Levels (ENC^- tied to GND)	0		2.5	V
Convert Clock Level (Differential)	Minimum Logic Levels (ENC^- not tied to GND, 1.2V common mode)	0.2			V

QUICK START PROCEDURE

DC2183 is easy to set up to evaluate the performance of the LTC2107 A/D converter. Refer to Figure 1 for proper measurement equipment set-up and follow the procedure below:

Setup

The DC1371 Data Acquisition and Collection System was supplied with the DC2183 board. Follow the DC1371 Quick Start Guide to install the required software and for connecting the DC1371 to the DC2183 and to a PC.

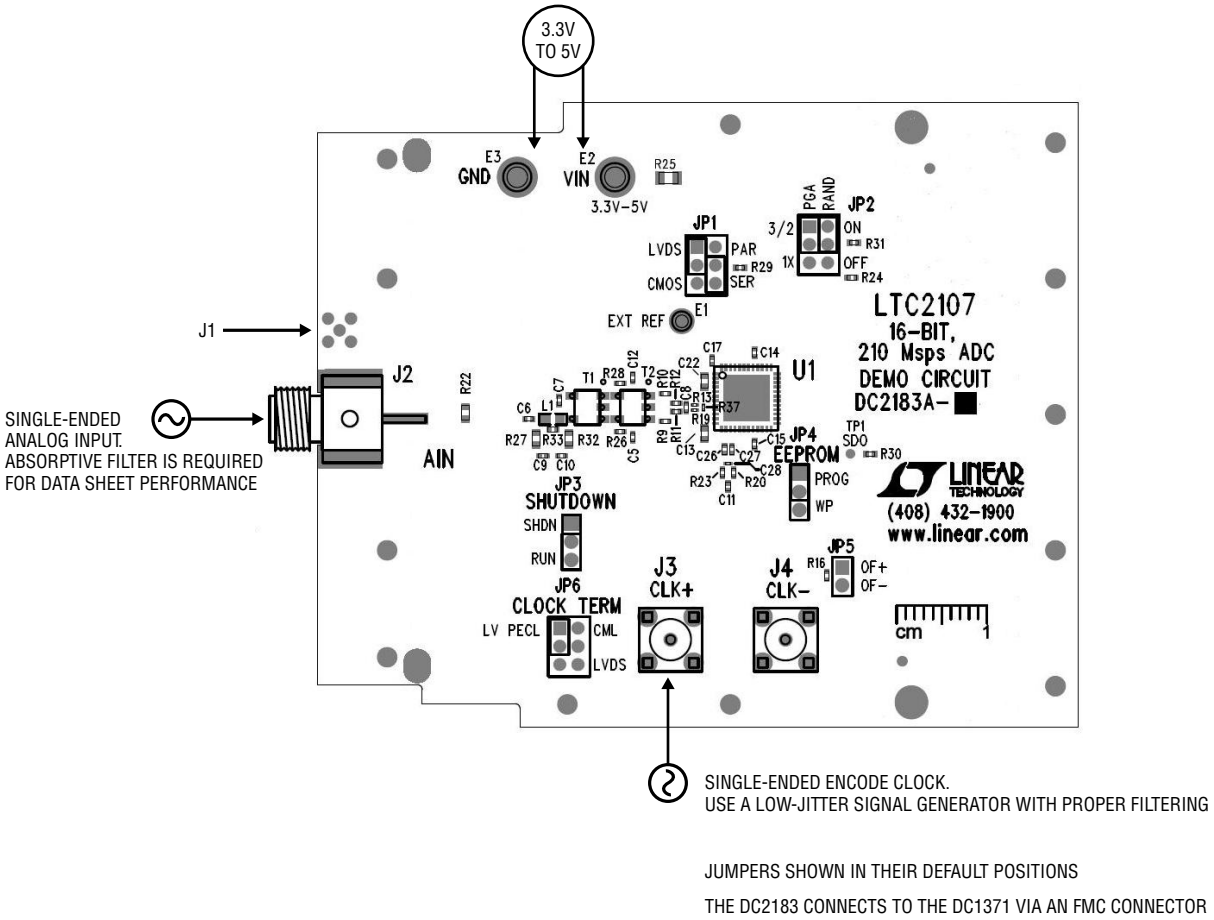

Figure 1. DC2183 Proper Measurement Equipment Setup
(zoom in for detail)

QUICK START PROCEDURE

HARDWARE SETUP

SMAs:

J2: Analog Input. Apply a signal to J2 from a 50Ω driver. Absorptive filters are required for data sheet performance.

J3: Encode Clock Input. Apply a clock signal to this SMA connector from a 50Ω driver. A filter is required for data sheet performance.

J4: Encode Clock Input For Differential Signals. By default the DC2183 is defined to accept a single-ended clock signal. It can be modified to accept a differential clock signal through J3 and J4. Some component changes are required, see the Encode Clock section for more information.

MMCX Connectors:

J1: Optional Analog Input. As a default, this connector is not populated. Standard MMCX connectors should be used. To connect this connector to the input of the ADC, populate R22 and remove J2 completely. By using this connector, the DC2183 becomes fully compliant with the FMC specification.

Turrets:

VIN: Positive Input Voltage for the ADC and Digital Buffers. This voltage feeds a regulator that supplies the proper voltages for the ADC and buffers. The voltage range for this turret is 3.3V to 5V.

EXT REF: Optional Reference Voltage. This pin is connected directly to the SENSE pin of the ADC. Connect EXT REF to a 1.25V external reference and the external reference mode is automatically selected. The external reference must be 1.25V ±25mV for proper operation. If no external voltage is supplied, this pin will be pulled up to 2.5V through a weak pull-up resistor.

GND: Ground Connection. This demo board only has a single ground plane. This turret should be tied to the GND terminal of the power supply being used.

Jumpers:

The DC2183 demonstration circuit should have the following jumper settings as default positions (per Figure 1) which configure the ADC in serial programming mode. In the default configuration JP1-JP2 should be left in the default locations. This will pull PAR/SER low, and the required pins high through weak pull-up resistors so the SPI commands can be sent from the PC. If JP1 is set to PAR then jumpers JP1-JP2 can be configured manually.

JP1: PAR/SER: Selects Parallel or serial programming mode (Default: Serial)

CMOS/LVDS: In Serial Programming Mode (SER), this pin should be in the LVDS position to allow for serial data transfer. (Default: LVDS or up) In the Parallel Programming Mode (PAR), this pin controls the Digital Output Mode. When this pin is in the CMOS position, the Full-Rate CMOS Output Mode is enabled. When this pin is in the LVDS position, the Double Data Rate LVDS Output Mode (with 3.5mA output current) is enabled. Note: When using the DC1371, parallel mode DDR LVDS must be selected.

JP2: PGA: In Serial Programming Mode (SER), this pin is pulled high through a weak pull-up resistor to allow serial data transfer. In the Parallel Programming Mode (PAR), this pin controls the Programmable Gain Amplifier front-end, PGA. In the 1x jumper position a front-end gain of 1x is selected, input range of $2.4V_{P-P}$. In the 3/2 jumper position a front-end gain of 1.5x is selected, input range of $1.6V_{P-P}$. (Default: 3/2 or up)

RAND: In Serial Programming Mode (SER), this pin is pulled high through a weak pull-up resistor to allow serial data transfer. In the Parallel Programming Mode (PAR), this pin becomes the Digital Output Randomization Control Bit. When this pin is in the OFF position, digital output randomization is disabled. When this pin is in the ON position, digital output randomization is enabled. To decode the randomized data, exclusive-OR each bit with the least significant bit. This is done for you in PScope when the randomizer option is toggled. (Default: ON or up).

QUICK START PROCEDURE

JP3: SHUTDOWN: In the RUN position this pin results in normal operation of the ADC. In the SHDN position the ADC is powered down and the digital outputs are set in high impedance state. (Default: RUN or down)

JP4: EEPROM: EEPROM Write Protect. For factory use only. Should be left in the enable (PROG) position.

JP5: Overflow Test Point: This is a test point for the differential overflow signal. This jumper can be installed to provide a convenient way to probe the overflow signal. (Default: removed)

JP6: Clock Term: This jumper provides termination voltages for various signaling standards. LVPECL, CML, and LVDS termination voltages can be selected. The selected voltage is then used to terminate the clock input through 50Ω resistors. By removing the jumper completely an external voltage can be applied directly to pin 5 of JP6 so an arbitrary signaling scheme can be used. (Default: LVPECL)

APPLYING POWER AND SIGNALS TO THE DC2183 DEMONSTRATION CIRCUIT

If a DC1371 is used to acquire data from the DC2183, the DC1371 must FIRST be connected to a powered USB port and provided an external 5 Volts BEFORE applying +3.3V to +5.0V across the pins marked VIN and GND on the DC2183. DC2183 requires at least 3.3V for proper operation. Regulators on the board produce the voltages required for the ADC. The DC2183 demonstration circuit requires up to 800mA. The DC2183 should not be removed or connected to the DC1371 while power is applied.

ANALOG INPUT NETWORK

Apply the analog input signal of interest to the SMA connector on the DC2183 demonstration circuit board marked J2. In the default setup, the DC2183 has an SMA input that is meant to be driven with a 50Ω source. The DC2183 is populated with an input diplexer filter to provide a 50Ω characteristic impedance over all frequencies. This can be modified to produce different frequency responses as needed.

In almost all cases, off-board absorptive filters will be required on the analog input of the DC2183 to produce data sheet SNR.

The off-board filter should be located close to the input of the demo board to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to make the filter look more absorptive to obtain low distortion.

ENCODE CLOCK

Apply an encode clock to the SMA connector on the DC2183 demonstration circuit board marked J3. As a default the DC2183 is populated to have a single ended clock input.

For the best noise performance, the encode input must be driven with a very low jitter signal generator source. The amplitude should be as large as possible up to $2V_{P-P}$ or 10dBm.

The DC2183 demo board is designed to accept single ended signals as a default. To modify the DC2183 to accept a differential signal, remove C31 and populate R18 with a 0Ω resistor. Changing the position of JP6 to CML, LVDS, or LVPECL selects the proper termination for your input signal. These SMAs are positioned 0.5” apart to accommodate LTC differential clock boards.

QUICK START PROCEDURE

SOFTWARE

The DC1371 is controlled by the PScope System Software which can be downloaded from the Linear Technology® website at http://www.linear.com/software/. If a DC1371 was provided, follow the DC1371 Quick Start Guide and the instructions below.

To start the data collection software, if *PScope.exe* is installed (by default) in \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC2183 demonstration circuit is properly connected to the DC1371, PScope should automatically detect the DC2183, and configure itself accordingly. If necessary, the procedure below explains how to manually configure PScope.

Under the Configure menu, go to ADC Configuration... Check the Config Manually box and use the following configuration options, see Figure 2:

Manual Configuration settings:

Bits: 16
Alignment: 16
FPGA Ld: S2157
Channs: 1
Bipolar: Unchecked
Positive-Edge Clk: Unchecked

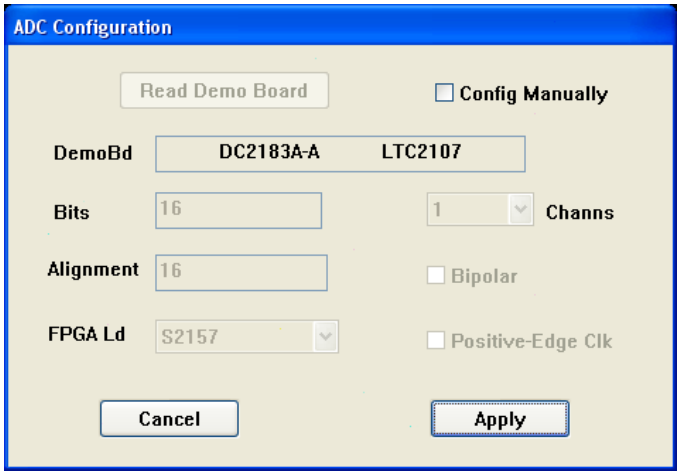

Figure 2. ADC Configuration

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the Collect button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC1371 quick start guide and in the online help available within the PScope program itself.

QUICK START PROCEDURE

SERIAL PROGRAMMING

PScope has the ability to program the DC2183 board serially through the DC1371. There are several options available for the LTC2107 that are only available through serial programming. PScope allows all of these features to be tested.

These options are available by first clicking on the Set Demo Bd Options icon on the PScope toolbar (Figure 3).

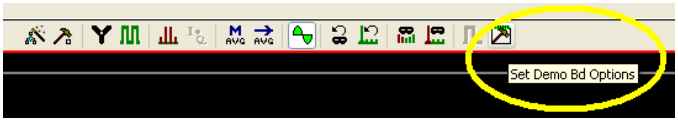

Figure 3. PScope Toolbar

This will bring up the menu shown in Figure 4.

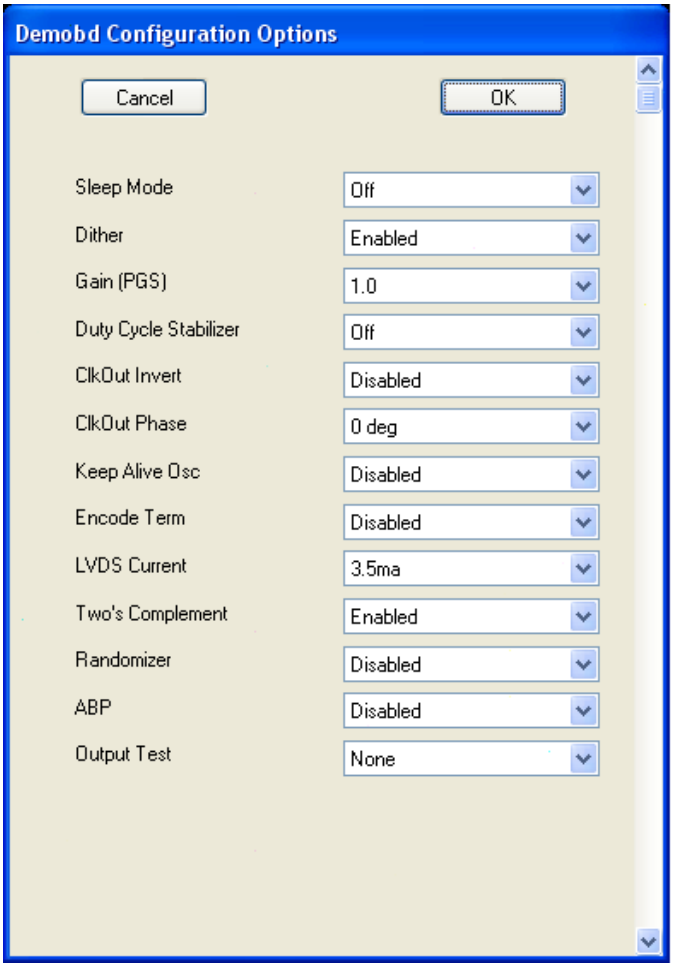

Figure 4. Demobd Configuration Options.

This menu allows any of the options available for the LTC2107 to be programmed serially. The LTC2107 has the following options:

Sleep Mode – Selects between normal operation and sleep mode:

- Off (Default) – Entire ADC is powered, and active
- On – The entire ADC is powered down

Dither – Selects between internal dither being enabled or disabled:

- Enabled (Default) – Internal dither enabled
- Disabled – Internal dither disabled

Gain (PGS) – Selects input range of the ADC:

- 1.0 (Default) – Selects the 2.4V input range
- 1.5 – Selects the 1.6V input range

Duty Cycle Stabilizer – Enables or disables duty cycle stabilizer:

- Stabilizer off (Default) – Duty cycle stabilizer disabled
- Stabilizer on – Duty cycle stabilizer enabled

ClkOut Invert – Selects the polarity of the CLKOUT signal:

- Disabled (Default) – Normal CLKOUT polarity
- Enabled – CLKOUT polarity is inverted

ClkOut Phase – Selects the phase delay of the CLKOUT signal:

- 0 deg (Default) – No CLKOUT delay
- 45 deg – CLKOUT delayed by 45 degrees
- 90 deg – CLKOUT delayed by 90 degrees
- 135 deg – CLKOUT delayed by 135 degrees

Keep Alive Osc – Enables or disables the internal keep alive oscillator:

- Disabled (Default) – Keep alive oscillator is disabled
- Enabled – Keep alive oscillator is enabled

Encode Termination – Enables or disables LVDS internal termination:

- Disabled (Default) – Disables internal termination
- Enabled – Enables internal termination

LVDS Current – Selects the LVDS output drive current:

- 1.75mA - LVDS output driver current
- 2.1mA - LVDS output driver current
- 2.5mA - LVDS output driver current
- 3.0mA - LVDS output driver current
- 3.5mA (Default) - LVDS output driver current
- 4.0mA - LVDS output driver current
- 4.5mA - LVDS output driver current

Two's Complement – Enables two's complement mode:

- Enabled (Default) – Selects two's complement mode
- Disabled – Selects offset binary mode

Randomizer – Enables data output randomizer:

- Disabled (Default) – Disables data output randomizer
- Enabled – Enables data output randomizer

ABP – Alternate Bit Polarity (ABP) mode:

- Disabled (Default) – Disables alternate bit polarity
- Enabled – Enables alternate bit polarity (Before enabling ABP, be sure the part is in offset binary mode)

Output Test – Selects digital output test patterns:

- None (Default) – ADC data presented at output
- All out = 1 – All digital outputs are 1
- All out = 0 – All digital outputs are 0
- Checkerboard – OF and D15-D0 alternate between 1 0101 0101 1010 0101 and 0 1010 1010 0101 1010 on alternating samples
- Alternating – Digital outputs alternate between all 1s and all 0s on alternating samples

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC2183 demo board.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	C1, C12	CAP., X7R, 0.1µF, 16V 10% 0402	AVX, 0402YC104KAT2A
2	2	C2, C4	CAP., X5R, 100µF, 16V 20% 1210	TAIYO YUDEN, EMK325ABJ107MM-T
3	2	C3, C22	CAP., X5R, 1µF, 25V 10% 0603	TDK, C1608X5R1E105K080AC
4	3	C5, C6, C7, C31	CAP., X7R, 0.01µF, 16V 10% 0402	TDK, C1005X7R1C103K
5	5	C11, C14, C15, C23, C29	CAP., X5R, 0.1µF, 16V 10% 0402	AVX, 0402YD104KAT2A
6	1	C13	CAP., X5R, 2.2µF, 16V 20% 0603	AVX, 0603YD225MAT2A
7	4	C16, C19, C20, C24	CAP., X5R, 10µF, 16V 20% 1206	TDK, C3216X5R1C106M
8	1	C17	CAP., X5R, 2.2µF, 16V 20% 0402	TDK, C1005X5R1C225M050BC
9	0	C18, C30	CAP., OPT, 0402	OPTION
10	1	C21	CAP., X5R, 47µF, 16V 20% 1206	TDK, C3216X5R1C476M160AB
11	1	C25	CAP., X7R, 10µF, 16V 10% 0805	SAMSUNG, CL21B106KOQNNNE
12	2	C26, C27	CAP., COG, 2200pF, 25V 5% 0402	KEMET, C0402C222J3GACTU
13	0	C28	CAP., OPT, 0201	OPTION
14	1	E1	TEST POINT, TURRET, .061, PBF	MILL-MAX, 2308-2-00-80-00-00-07-0
15	2	E2, E3	TEST POINT, TURRET, .094, PBF	MILL-MAX, 2501-2-00-80-00-00-07-0
16	3	JP1, JP2, JP6	HEADER, 2X3 PIN, 0.079CC	SULLINS, NRPN032PAEN-RC
17	2	JP3, JP4	HEADER, 3 PIN 0.079 SINGLE ROW	SULLINS, NRPN031PAEN-RC
18	0	JP5	JUMPER, 2PINS, .079 CTR, OPTION	OPTION
19	0	J1	CON.,MMCX, RIGHT ANGLE, THRU-HOLE, OPTION	AMPHENOL CONNEX, 262105
20	1	J2	CON., SMA 50Ω EDGE-LAUNCH	AMPHENOL CONNEX, 132372
21	2	J3, J4	CON.,SMA JACK, STRAIGHT, THRU-HOLE	AMPHENOL CONNEX, 132134
22	0	L2	INDUCTOR, OPTION, 0603	OPTION
23	1	L3	FERRITE BEAD, 47ΩS@100mhz, 0603	MURATA, BLM18BB470SN1D
24	1	P1	BGA CONNECTOR, 40X10	SAMTEC, SEAM-40-02.0-S-10-2-A-K-TR
25	6	R1, R6, R7, R8, R14, R17	RES., CHIP, 1k, 1/16W, 5% 0402	VISHAY, CRCW04021K00JNED
26	1	R2, R9, R10	RES., CHIP, 0ΩS JUMPER, 1/16W, 0402	VISHAY, CRCW04020000Z0ED
27	3	R3, R4, R5	RES., CHIP, 4.99k, 1/16W, 1% 0402	VISHAY, CRCW04024K99FKED
28	2	R11, R12	RES., CHIP, 33.2ΩS, 1/16W, 1% 0402	VISHAY, CRCW040233R2FKED
29	2	R15, R16	RES., CHIP, 100ΩS, 1/16W, 5% 0402	VISHAY, CRCW0402100RJNED
30	0	R18, R20, R23	RES., CHIP, OPT, 0402	OPTION
31	1	R21	RES., CHIP, 49.9ΩS, 1/8W, 1% 0402	VISHAY, CRCW040249R9FKEDHP
32	0	R22	RES., CHIP, OPT, 0603	OPTION
33	4	R24, R29, R30, R31	RES., CHIP, 33ΩS, 1/16W, 5% 0402	VISHAY, CRCW040233R0JNED
34	0	R25	RES., CHIP, OPT, 0805	OPTION
35	2	R34, R36	RES., CHIP, 24.9ΩS, 1/16W, 1% 0402	VISHAY, CRCW040224R9FKED
36	1	R37	RES., CHIP, 200Ω, 1/20W, 1% 0201	VISHAY, CRCW0201200RFKED
37	2	T1, T3	TRANSFORMER, RF,SMT, 1:1BALUN	MACOM, MABA-007159-000000
38	1	T2	TRANSFORMER, RF 1:1 FLUX COUPLED, SMT	MACOM, MABAES0060
39	1	U2	IC, LDO LINEAR REGULATOR, 2.5V, DFN	LINEAR TECH., LT1965EDD-2.5#PBF
40	1	U3	IC, LDO LINEAR REGULATOR, 1.8V, DFN	LINEAR TECH., LT1965EDD-1.8#PBF
41	1	U4	IC, SERIAL EEPROM, TSSOP	MICROCHIP TECH., 24LC32A-I/ST
42	7	XJP1, XJP2, XJP3, XJP4, XJP5, XJP6, XJP7	SHUNT, 2MM	SAMTEC, 2SN-BK-G

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC2183A-A Required Circuit Components				
1	1	DC2183A	DC2183A General BOM	
2	1	C8	CAP., NP0, 4.7pF, 50V ± 0.25pF, 0402	TDK, C1005C0G1H4R7C
3	2	C9,C10	CAP., NP0, 8.2pF, 50V ± 0.25pF 0402	TDK, C1005C0G1H8R2C
4	1	L1	INDUCTOR, CERAMIC CHIP, 56nH, 2%, 0603	MURATA, LQP18MN56NG02D
5	2	R13,R19	RES., CHIP, 15Ω, 1/20W, 5% 0201	VISHAY, CRCW020115R0JNED
6	0	R26,R28	RES., CHIP, OPT, 0402	OPTION
7	2	R27,R32	RES., CHIP, 86.6, 1/10W, 1% 0603	VISHAY, CRCW060386R6FKEA
8	1	R33	RES., CHIP, 86.6, 1/16W, 1% 0402	VISHAY, CRCW040286R6FKED
9	1	U1	ADC, 16 BIT, 210 Msps, QFN	LINEAR TECH., LTC2107IUK#PBF
DC2183A-B Required Circuit Components				
1	1	DC2183A	DC2183A General BOM	
2	1	C8	CAP., NP0, 12pF, 50V 5% 0402	MURATA, GRM1555C1H120JA01D
3	2	C9,C10	CAP., NP0, 3.9pF, 50V ± 0.25pF 0402	TDK, C1005C0G1H3R9C
4	1	L1	INDUCTOR, CERAMIC CHIP, 18nH, 2%, 0603	MURATA, LQP18MN18NG02D
5	2	R13,R19	RES., CHIP, 10Ω, 1/20W, 5% 0201	VISHAY, CRCW020110R0JNED
6	2	R26,R28	RES., CHIP, 68.1Ω, 1/16W, 1% 0402	VISHAY, CRCW040268R1FKED
7	2	R27,R32	RES., CHIP, 43.2, 1/10W, 1% 0603	VISHAY, CRCW060343R2FKEA
8	1	R33	RES., CHIP, 105Ω, 1/16W, 1% 0402	VISHAY, CRCW0402105RFKED
9	1	U1	ADC, 16 BIT, 210 Msps, QFN	LINEAR TECH., LTC2107IUK#PBF

SCHEMATIC DIAGRAM

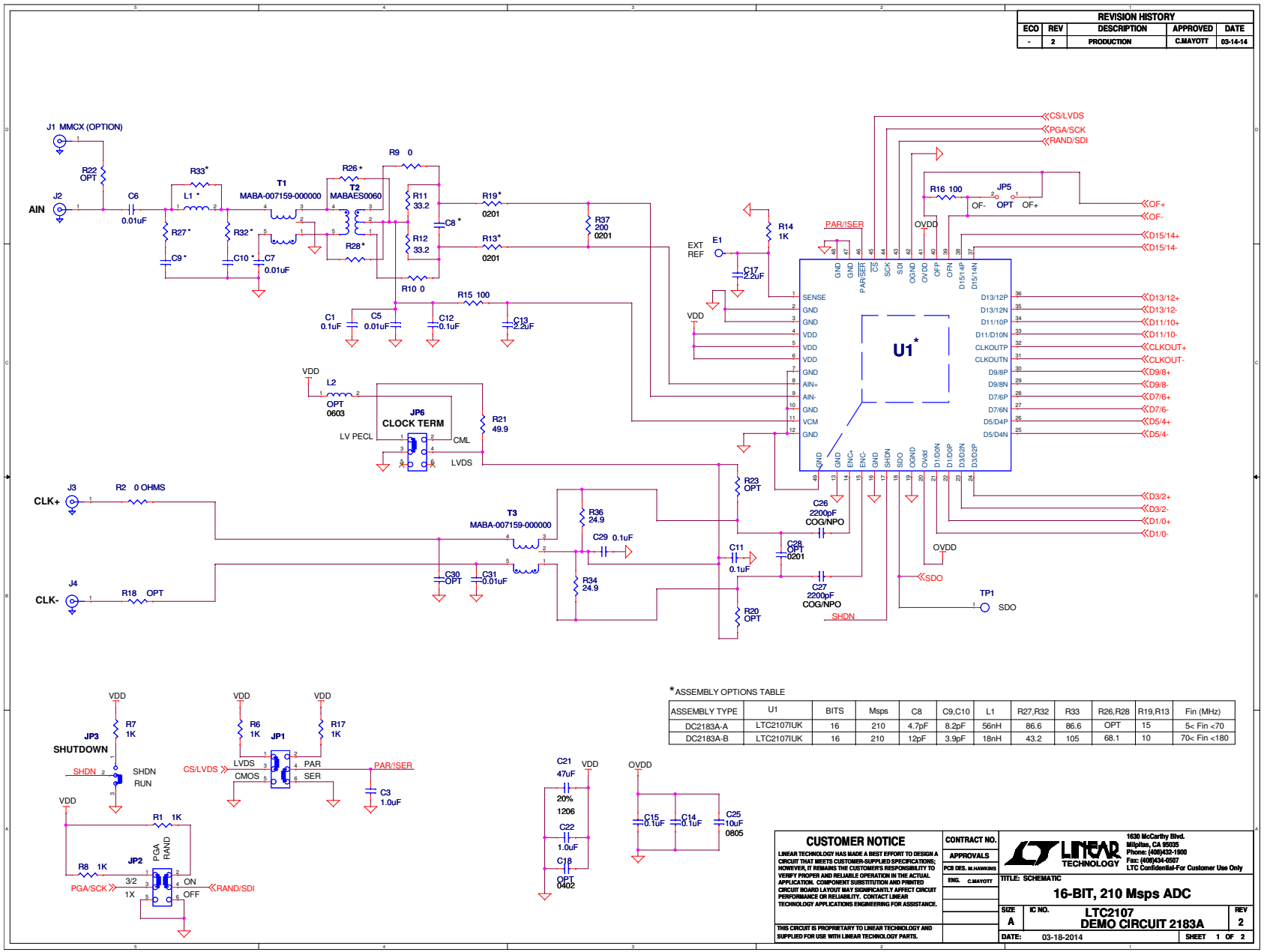

Figure 5. DC2183A Demo Circuit Schematic, Page 1

SCHEMATIC DIAGRAM

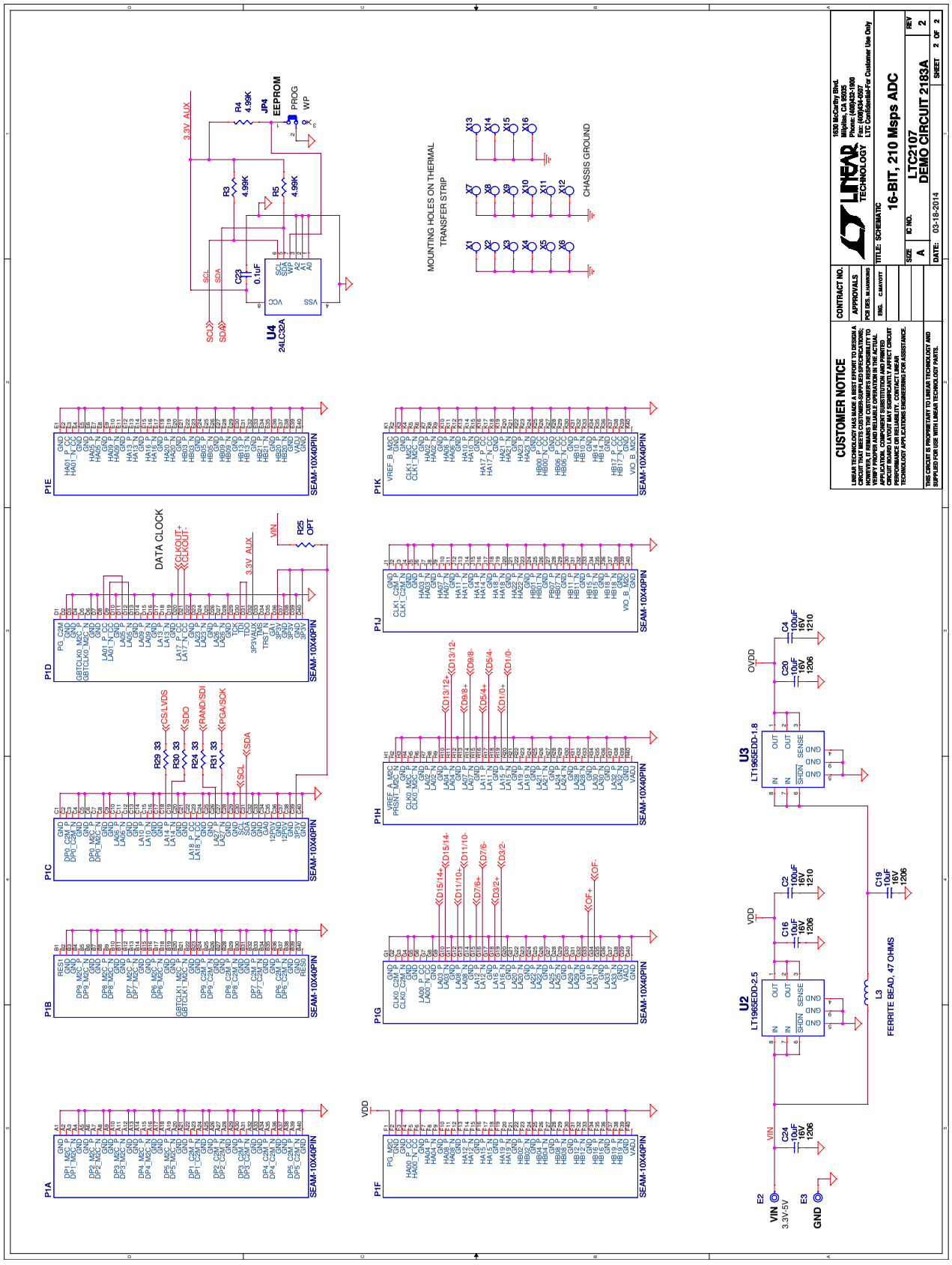

Figure 6. DC2183A Demo Circuit Schematic, Page 2

DEMONSTRATION BOARD IMPORTANT NOTICE

Linear Technology Corporation (LTC) provides the enclosed product(s) under the following **AS IS** conditions:

This demonstration board (DEMO BOARD) kit being sold or provided by Linear Technology is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not provided by LTC for commercial use. As such, the DEMO BOARD herein may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including but not limited to product safety measures typically found in finished commercial goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may or may not meet the technical requirements of the directive, or other regulations.

If this evaluation kit does not meet the specifications recited in the DEMO BOARD manual the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY THE SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THIS INDEMNITY, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user releases LTC from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. Also be aware that the products herein may not be regulatory compliant or agency certified (FCC, UL, CE, etc.).

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LTC currently services a variety of customers for products around the world, and therefore this transaction **is not exclusive**.

Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged**.

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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