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LT3042EDD

20V, 200mA, Ultralow Noise Ultrahigh PSRR RF LDO Regulator

DESCRIPTION

DC2246A is a linear regulator featuring the **LT[®]3042EDD**, which is a 200mA, ultralow noise, and ultrahigh power supply rejection ratio (PSRR) RF low dropout (LDO) linear regulator with programmable current limit.

DC2246A operates over an input range of 3.8V to 20V. The LT3042 has a maximum output current of 200mA. It features ultralow noise (0.8 μ Vrms from 10Hz to 100kHz) and very high PSRR (79dB at 1MHz). The power good feedback (PGFB) pin voltage is programmable for power good threshold. A current limit function is provided. Current monitoring is also achievable by sensing the voltage of ILIM.

Built-in protection includes reverse battery protection, reverse current protection, internal current limit with foldback and thermal limit with hysteresis.

The LT3042 data sheet gives a complete description of the device, operation and applications information. The data sheet must be read in conjunction with this Demo Manual for demonstration circuit DC2246A. The LT3042EDD is assembled in a 10-lead (3mm x 3mm) plastic DFN package with an exposed pad on the bottom-side of the IC. **Proper board layout is essential for maximum thermal performance and ultrahigh PSRR.**

Design files for this circuit board are available at <http://www.linear.com/demo/DC2246A>

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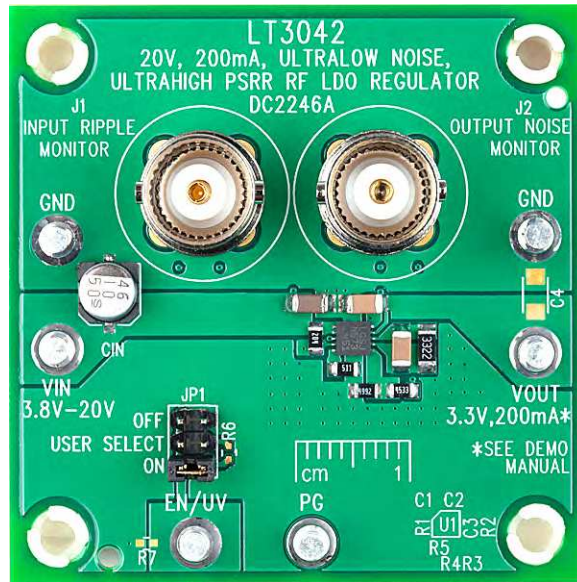
PERFORMANCE SUMMARY

Specifications are at $T_A = 25^\circ\text{C}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range (V_{IN})	$V_{OUT} = 3.3V$	3.8		20	V
Shutdown Input Current (I_{IN})	JP1 = OFF, $V_{IN} = 6V$		0.1		μ A
Output Voltage (V_{OUT})	$V_{IN} = 5V$, $I_{OUT} = 200mA$	3.2	3.3	3.4	V
Output Current Range (I_{OUT})	$V_{IN} = 3.8V\sim 19.7V$, $V_{OUT} = 3.3V$	0		200	mA
Output Current Range (I_{OUT})	$V_{IN} = 3.8V\sim 20V$, $V_{OUT} = 3.3V$	0		195*	mA

* Please refer to the Current Limit vs. Input-to-Output Differential in the LT3042 data sheet.

BOARD PHOTO



QUICK START PROCEDURE

The DC2246A is easy to set up to evaluate the performance of the LT3042EDD. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Connect Load between the VOUT and GND terminals.
2. With power off, connect the input power supply to the VIN and GND terminals.
3. Make sure the shunt of JP1 is in the ON position.
4. Turn the input power supply on and make sure the voltage is between 3.8V and 20V.
5. R6 and R7 can define an accurate undervoltage lockout (UVLO) threshold when the shunt of JP1 is in the USER SELECT position.
6. Please refer to Application Note 70 for more precise techniques for measuring the output noise.

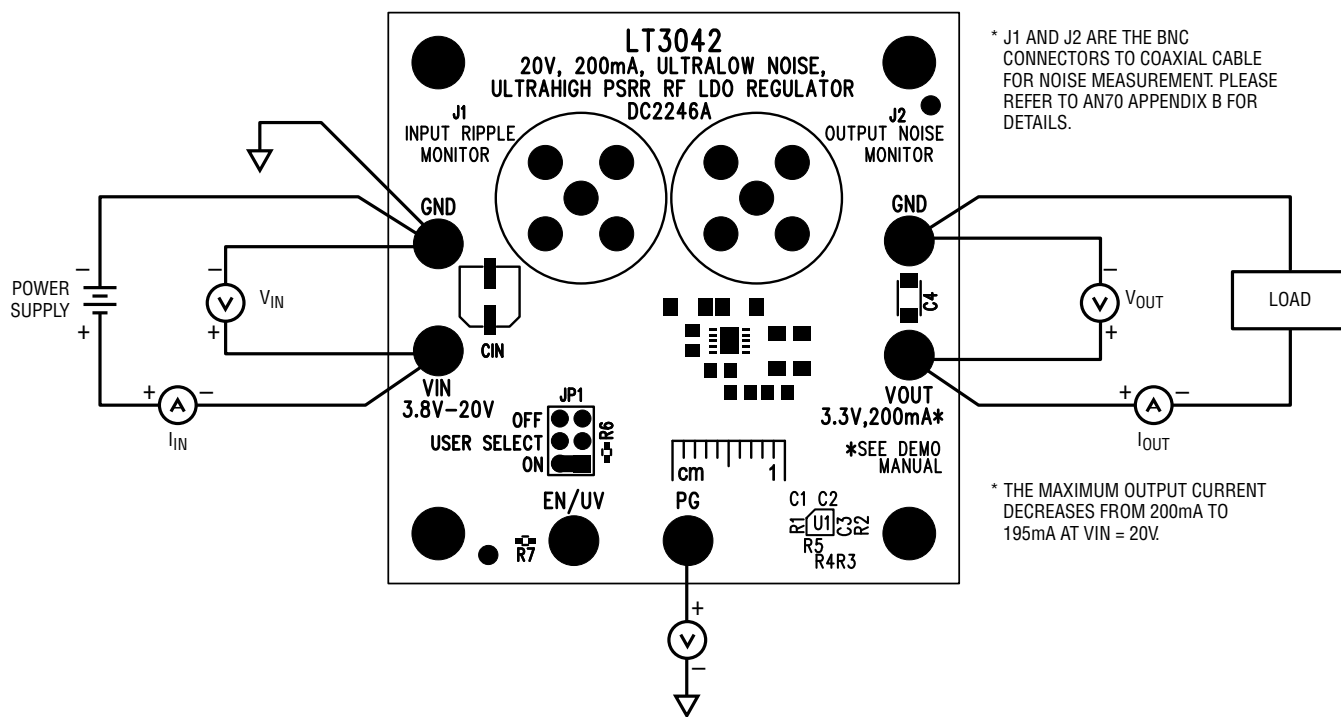


Figure 1. Test Procedure Setup Drawing for DC2246A

DEMO MANUAL DC2246A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CIN	CAP., ALUM, 10 μ F, 50V, 5X5.4MM	SUN SELECT., 50CE10BSS
2	1	C1	CAP., X7R, 4.7 μ F, 50V, 10% 1206	MURATA, GRM31CR71H475KA12L
3	2	C2, C3	CAP., X7R, 4.7 μ F, 25V, 10% 1206	MURATA, GRM31CR71E475KA88L
4	1	R1	RES., CHIP, 200k, 1/16W, 5% 0805	VISHAY, CRCW0805200KJNEA
5	1	R2	RES., CHIP, 33.2k, 1/8W, 1% 1206	NIC, NRC12F3322TRF
6	1	R3	RES., CHIP, 453k, 1/8W, 1% 0805	VISHAY, CRCW0805453KFKEA
7	1	R4	RES., CHIP, 49.9k, 1/8W, 1% 0805	VISHAY, CRCW080549K9FKEA
8	1	R5	RES., CHIP, 510 Ω , 1/16W, 5% 0805	VISHAY, CRCW0805510RJNEA
9	1	U1	IC, LT3042EDD, DFN 3X3mm	LINEAR TECH., LT3042EDD#PBF
Optional Electronic Components				
1	0	C4 (OPT)	CAP., 1206	
2	0	C5, C6 (OPT)	CAP., 0603	
3	0	R6, R7 (OPT)	RES., 0402	
Hardware: For Demo Board Only				
1	6	E1-E6	TESTPOINT, TURRET, 0.094" PBF	MILL-MAX, 2501-2-00-80-00-00-07-0
2	1	JP1	HEADER 3 PIN 0.079 DOUBLE ROW	WÜRTH ELEKTRONIK, 620 006 211 21
3	1	XJP1	SHUNT, 0.079" CENTER	WÜRTH ELEKTRONIK, 608 002 134 21
4	2	J1, J2	CONN., BNC, 5 PINS	CONNEX, 112404
5	4	MH1-MH4	STAND-OFF, NYLON, 0.25"	KEYSTONE, 8831(SNAP ON)

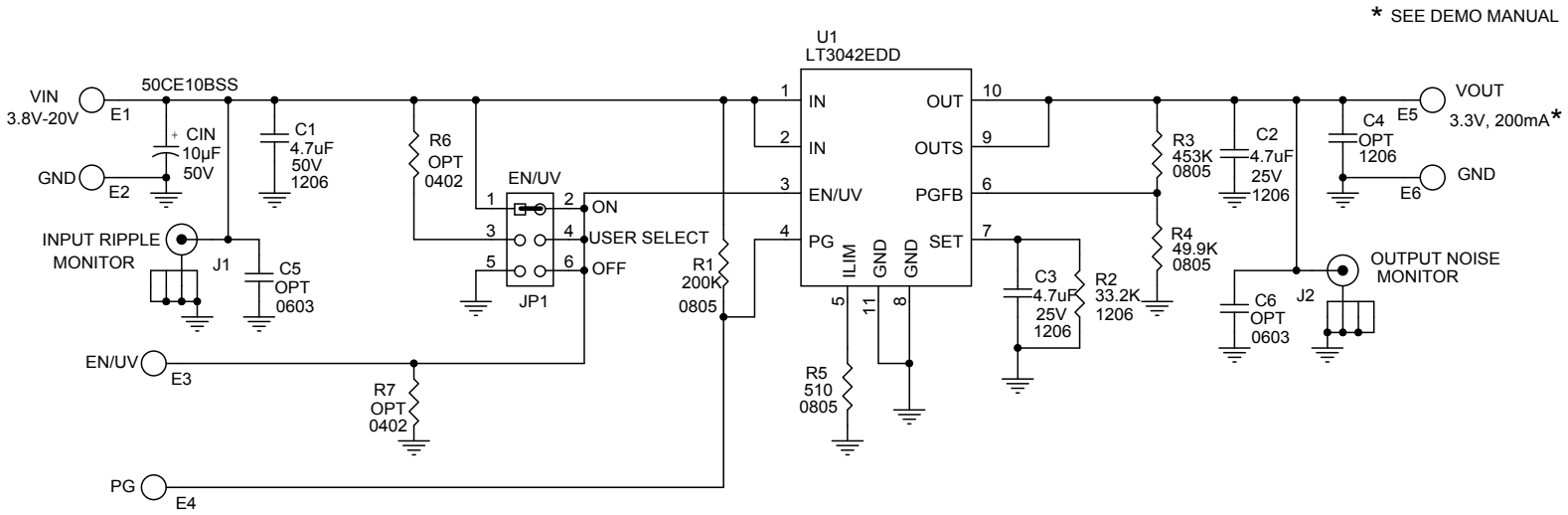


Figure 2. DC2246A Demo Circuit Schematic

DEMO MANUAL DC2246A

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