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DEMO CIRCUIT 852
QUICK START GUIDE

LTC4354
200W Negative Voltage Diode-OR Controller

DESCRIPTION

Demonstration Circuit 852 showcases the LTC®4354 negative voltage diode-OR controller and monitor in a 200W, 36 to 72V application. Included on board are two S-8 ORing MOSFETs and an LED to indicate fault conditions. The –48V inputs are separated from RTN and from each other with at least 60 mils spacing, except for where drain sensing resistors bridge the gap. 93-mil turrets make input and output connections; if removed, these accommodate insertion of up to 12 gauge wires for in-situ testing.

The small size of this demonstration circuit facilitates grafting into a working system for evaluation purposes. On the backside of the board there are pads for D2-pak MOSFETs. The S-8 MOSFETs included on the board are avalanche rated and carry up to 5A for ATCA® applications.

Design files for this circuit board are available. Call the LTC factory.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Input Supply Range	(–48VA)–(–48VB)	–100		100	V
	Maximum Output Current		5			A
	Commutation Time			700		ns

BOARD LAYOUT

The top of the board contains the components necessary for the application. The 93-mil turrets are not swaged and may be removed before assembly in a working system with up to 12-gauge wire. The FDS3672 MOSFETs can handle 5A continuous load current in this board.

The bottom of the board contains no components but provisions are made for installation of optional D2-pak MOSFETs. Remove the topside S-8 MOSFETs if others are installed on the bottom side. Larger MOSFETs extend the usable range of this board to in excess of 10A.

The FDS3672 S-8 MOSFETs are capable of handling up to 7.5A for short periods, limited by the thermal characteristics of the board. A continuous load current of 5A is permissible with the board laying face-up on a lab bench with only convection cooling. Thus situated and carrying 5A load current, either MOSFET experiences a junction temperature rise of approximately 75°C.

Copper loss is equivalent to about 2 squares of 1-ounce copper, or ≅1.2mΩ, measured from turret to S-8 MOSFET lead.

Dissipation for the combined MOSFET and board loss is 700mW at 5A. In contrast, the power loss from an equivalent passive Schottky diode circuit would measure about 3.1W. This represents a power and thermal area savings of more than 4X.

A clear line of demarcation separates RTN, –48VA and –48VB, with a spacing of at least 60 mils to any adjacent trace. Spacing necks down in the vicinity of R1 and R2.

To increase the voltage capability of this area, use either larger resistors (1206, for example) or apply conformal coating. Since operational spacing is ultimately limited by the LTC4354's DFN package, the latter is preferred. An S-8 package (LTC4354CS8 or LTC4354IS8) with wider pad spacing is also available.

The LTC4354 detects excessive Vds (>260mV) across the MOSFETs and reports this to the FAULT pin, asserting it high and illuminating LED1. As a result the LED not only indicates faults, but also doubles as a clamp for the FAULT pin, limiting the high-state voltage to less than 2V.

At room temperature the typical resistance of the FDS3672 MOSFET is 19mΩ, requiring a current of 13.7A to trip the FAULT pin. Although this exceeds the MOSFET's maximum continuous current rating, the device can handle such a current for up to 400ms. As the MOSFET heats up, its resistance increases to a point where as little as 7.5A drain current is necessary to trip the FAULT detector. Under normal operating conditions LED1 will not illuminate.

Note that the aforementioned Vds detection is performed in a negative direction, asserting FAULT when Vd is 260mV or more negative with respect to Vs. This corresponds to either an open MOSFET, or current flow far in excess of the intended operating range.

QUICK START PROCEDURE

Connect –48V power sources to –48VA and –48VB, with the combined returns connected to RTN. The 48V output is taken at –48VOUT. The larger magnitude supply will source current as controlled by the diode action of the LTC4354.

The turrets are installed without swaging in 93-mil plated through holes. They may be removed for insertion of up to 12 AWG wire for in-situ testing.

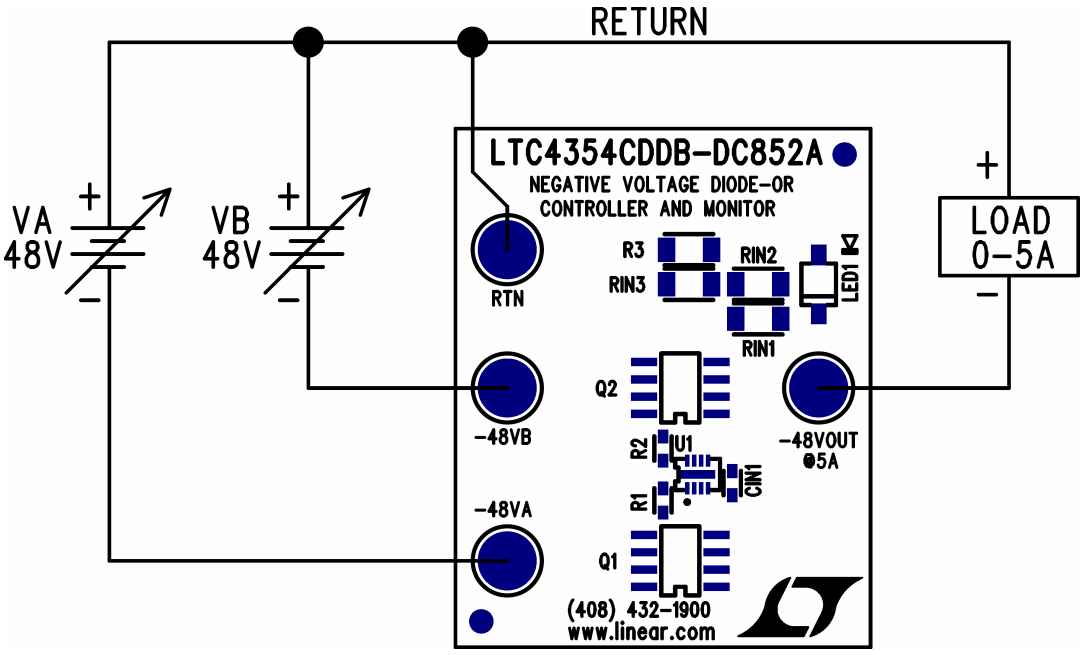
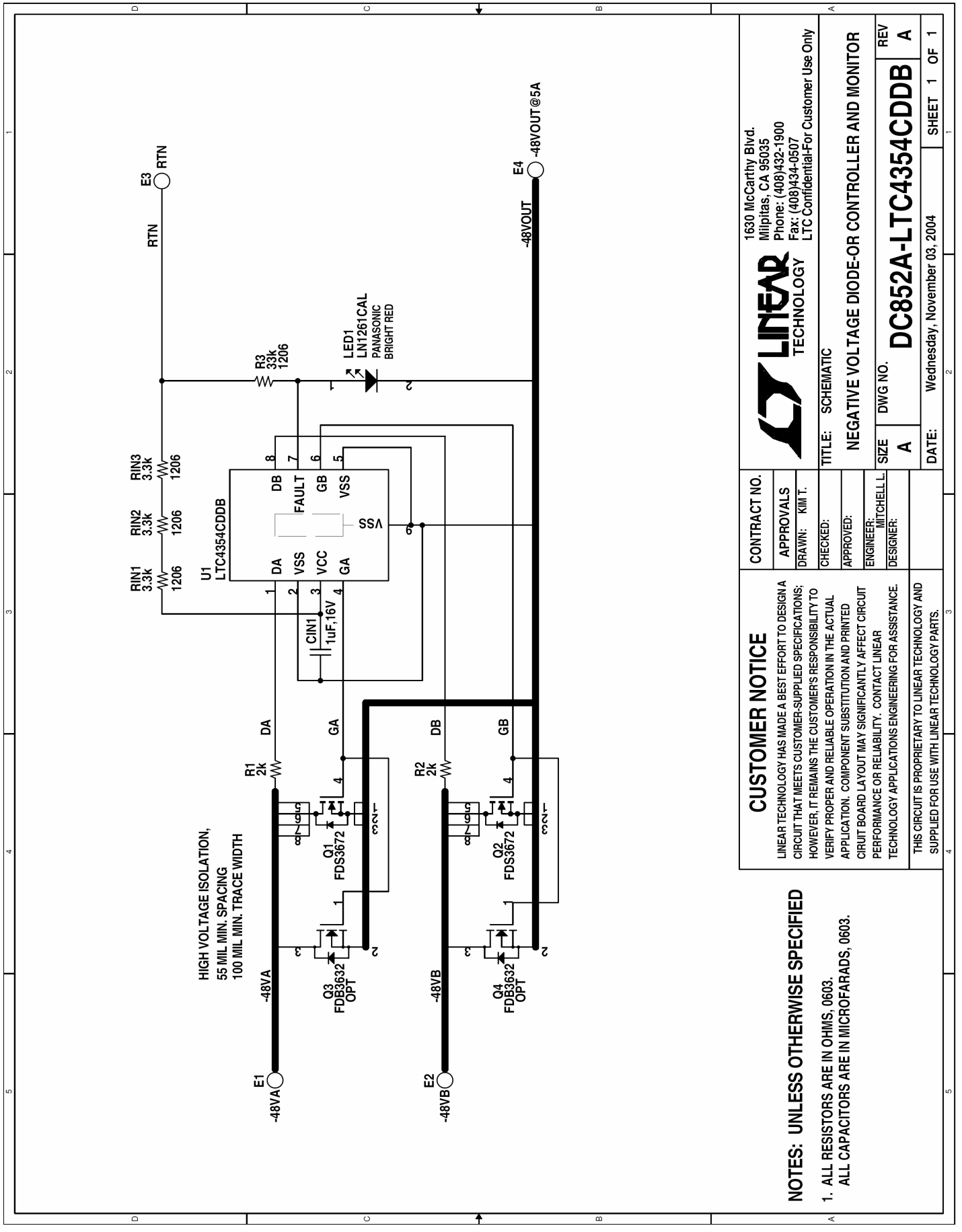


Figure 1. Proper Measurement Equipment Setup


E3
RTN
RTN
R3
33k
1206
LED1
LN1261CAL
PANASONIC
BRIGHT RED
E4
-48VOUT@5A
-48VOUT
RIN1
3.3k
1206
RIN2
3.3k
1206
RIN3
3.3k
1206
U1
LTC4354CDDB
DA
VSS
VCC
GA
DB
FAULT
GB
VSS
SSA
CIN1
1uF;16V
R1
2k
R2
2k
Q1
FDS3672
Q2
FDS3672
Q3
FDB3632
OPT
Q4
FDB3632
OPT
HIGH VOLTAGE ISOLATION,
55 MIL MIN. SPACING
100 MIL MIN. TRACE WIDTH
E1
-48VA
E2
-48VB
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 0603.
ALL CAPACITORS ARE IN MICROFARADS, 0603.
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CHECKED:
APPROVED:
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SIZE A
DWG NO. DC852A-LTC4354CDDB
REV A
DATE: Wednesday, November 03, 2004
SHEET 1 OF 1