



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## FEATURES

- **Sample Rate: 80MSPS/65MSPS**
- **81.5dBFS Noise Floor**
- **100dB SFDR**
- **SFDR >95dB at 70MHz**
- **85fs<sub>RMS</sub> Jitter**
- **2.75V<sub>P-P</sub> Input Range**
- **400MHz Full Power Bandwidth S/H**
- **Optional Internal Dither**
- **Optional Data Output Randomizer**
- **LVDS or CMOS Outputs**
- **Single 3.3V Supply**
- **Power Dissipation: 970mW/700mW**
- **Clock Duty Cycle Stabilizer**
- **Pin-Compatible with LTC2208, LTC2217**
- **64-Pin (9mm × 9mm) QFN Package**

## APPLICATIONS

- Telecommunications
- Receivers
- Cellular Base Stations
- Spectrum Analysis
- Imaging Systems
- ATE

## DESCRIPTION

The LTC<sup>®</sup>2216/LTC2215 are 80MSPS/65MSPS sampling 16-bit A/D converters designed for digitizing high frequency, wide dynamic range signals with input frequencies up to 400MHz. The input range of the ADC is fixed at 2.75V<sub>P-P</sub>.

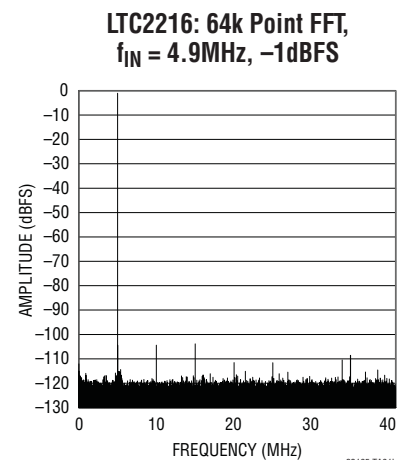
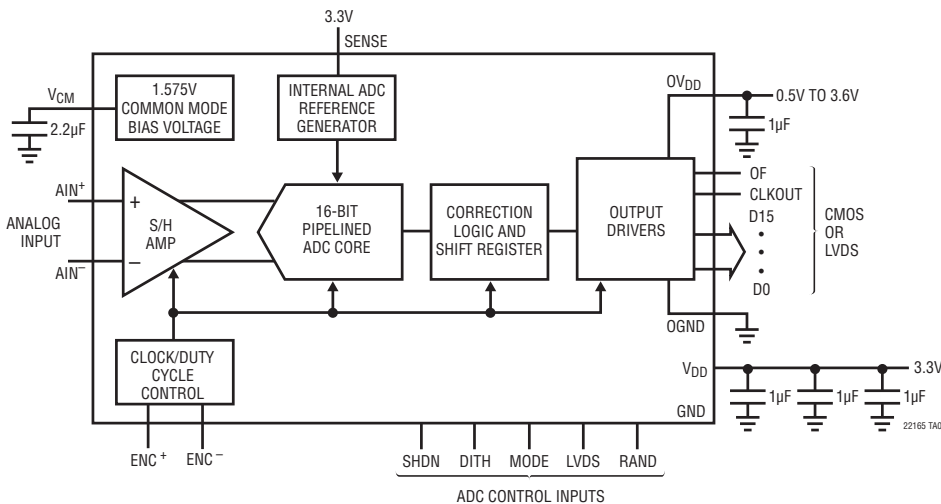
The LTC2216/LTC2215 are perfect for demanding communications applications, with AC performance that includes 81.5dBFS noise floor and 100dB spurious free dynamic range (SFDR). Ultra low jitter of 85fs<sub>RMS</sub> allows undersampling of high input frequencies while maintaining excellent noise performance. Maximum DC specs include ±3.5LSB INL, ±1LSB DNL (no missing codes).

The digital output can be either differential LVDS or single-ended CMOS. There are two format options for the CMOS outputs: a single bus running at the full data rate or demultiplexed buses running at half data rate. A separate output power supply allows the CMOS output swing to range from 0.5V to 3.6V.

The ENC<sup>+</sup> and ENC<sup>-</sup> inputs may be driven differentially or single-ended with a sine wave, PECL, LVDS, TTL or CMOS inputs. An optional clock duty cycle stabilizer allows high performance at full speed with a wide range of clock duty cycles.

LT, LT, LTC and LTM are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

## TYPICAL APPLICATION



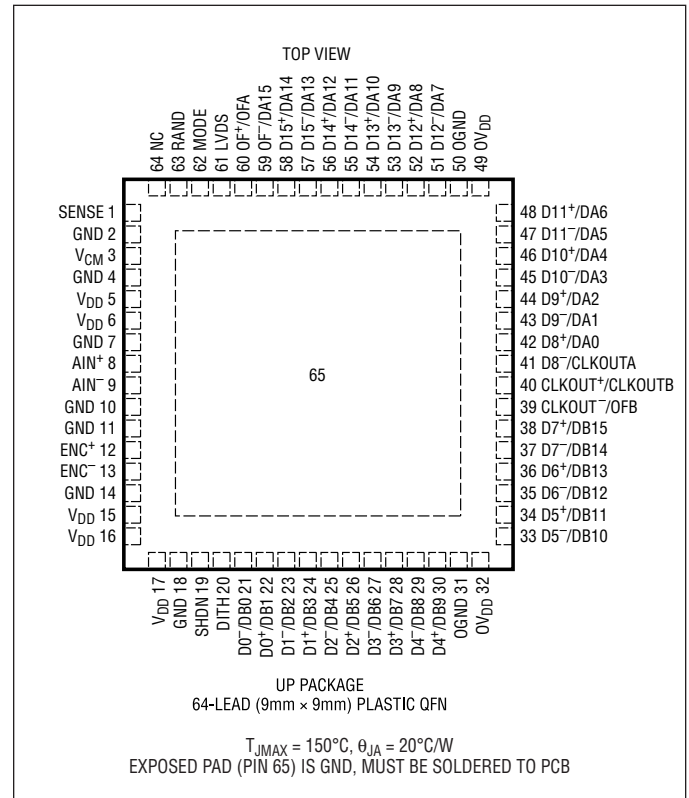
# LTC2216/LTC2215

## ABSOLUTE MAXIMUM RATINGS

$OV_{DD} = V_{DD}$  (Notes 1 and 2)

Supply Voltage ( $V_{DD}$ )	-0.3V to 4V
Digital Output Supply Voltage ( $OV_{DD}$ )	-0.3V to 4V
Digital Output Ground Voltage ( $OGND$ )	-0.3V to 1V
Analog Input Voltage (Note 3)	-0.3V to ( $V_{DD} + 0.3V$ )
Digital Input Voltage	-0.3V to ( $V_{DD} + 0.3V$ )
Digital Output Voltage	-0.3V to ( $OV_{DD} + 0.3V$ )
Power Dissipation	2000mW
Operating Temperature Range	
LTC2215C/LTC2216C	0°C to 70°C
LTC2215I/LTC2216I	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2215CUP#PBF	LTC2215CUP#TRPBF	LTC2215UP	64-Lead (9mm x 9mm) Plastic QFN	0°C to 70°C
LTC2215IUP#PBF	LTC2215IUP#TRPBF	LTC2215UP	64-Lead (9mm x 9mm) Plastic QFN	-40°C to 85°C
LTC2216CUP#PBF	LTC2216CUP#TRPBF	LTC2216UP	64-Lead (9mm x 9mm) Plastic QFN	0°C to 70°C
LTC2216IUP#PBF	LTC2216IUP#TRPBF	LTC2216UP	64-Lead (9mm x 9mm) Plastic QFN	-40°C to 85°C
LEAD BASED FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2215CUP	LTC2215CUP#TR	LTC2215UP	64-Lead (9mm x 9mm) Plastic QFN	0°C to 70°C
LTC2215IUP	LTC2215IUP#TR	LTC2215UP	64-Lead (9mm x 9mm) Plastic QFN	-40°C to 85°C
LTC2216CUP	LTC2216CUP#TR	LTC2216UP	64-Lead (9mm x 9mm) Plastic QFN	0°C to 70°C
LTC2216IUP	LTC2216IUP#TR	LTC2216UP	64-Lead (9mm x 9mm) Plastic QFN	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

## CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Integral Linearity Error	Differential Analog Input (Note 5)	●		±1.2	±3.5	LSB
Differential Linearity Error	Differential Analog Input	●		0.16/-0.2	±1	LSB
Offset Error	(Note 6)	●		±1.5	±8	mV
Offset Drift				±4		$\mu\text{V}/^\circ\text{C}$
Gain Error	External Reference	●		±0.3	±1	%FS
Full-Scale Drift	Internal Reference			-65		ppm/ $^\circ\text{C}$
	External Reference			±12		ppm/ $^\circ\text{C}$
Transition Noise	External Reference			2		$\text{LSB}_{\text{RMS}}$

## ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{\text{IN}}$	Analog Input Range ( $A_{\text{IN}}^+ - A_{\text{IN}}^-$ )	$3.135\text{V} \leq V_{\text{DD}} \leq 3.465\text{V}$			2.75		$V_{\text{P-P}}$
$V_{\text{IN, CM}}$	Analog Input Common Mode	Differential Input (Note 7)	●	1.2	1.575	1.8	V
$I_{\text{IN}}$	Analog Input Leakage Current	$0\text{V} \leq A_{\text{IN}}^+, A_{\text{IN}}^- \leq V_{\text{DD}}$	●	-1		1	$\mu\text{A}$
$I_{\text{SENSE}}$	SENSE Input Leakage Current	$0\text{V} \leq \text{SENSE} \leq V_{\text{DD}}$	●	-3		3	$\mu\text{A}$
$I_{\text{MODE}}$	MODE Pin Pull-Down Current to GND				10		$\mu\text{A}$
$I_{\text{LVDS}}$	LVDS Pin Pull-Down Current to GND				10		$\mu\text{A}$
$C_{\text{IN}}$	Analog Input Capacitance	Sample Mode $\text{ENC}^+ < \text{ENC}^-$			9.1		pF
		Hold Mode $\text{ENC}^+ > \text{ENC}^-$			1.8		pF
$t_{\text{AP}}$	Sample-and-Hold Acquisition Delay Time				0.35		ns
$t_{\text{JITTER}}$	Sample-and-Hold Aperture Jitter				85		fs RMS
CMRR	Analog Input Common Mode Rejection Ratio	$1.2\text{V} < (A_{\text{IN}}^+ = A_{\text{IN}}^-) < 1.8\text{V}$			80		dB
BW-3dB	Full Power Bandwidth	$R_S < 25\Omega$			400		MHz

# LTC2216/LTC2215

**DYNAMIC ACCURACY** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $A_{IN} = -1\text{dBFS}$  with 2.75V range unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LTC2215			LTC2216			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-Noise Ratio	5MHz Input		81.5		81.3		dBFS	
		15MHz Input, $T_A = 25^\circ\text{C}$		80.8	81.4	80.6	81.2	dBFS	
		15MHz Input	●	80.5	81	80.2	80.8	dBFS	
		30MHz Input, $T_A = 25^\circ\text{C}$			81.2		81.1	dBFS	
		70MHz Input, $T_A = 25^\circ\text{C}$		80	80.6	80	80.5	dBFS	
		70MHz Input	●	79.7	80.2	79.7	80.2	dBFS	
		140MHz Input		79		79	dBFS		
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	5MHz Input		100		100		dBc	
		15MHz Input, $T_A = 25^\circ\text{C}$		88	100	88	100	dBc	
		15MHz Input	●	88	96	88	99	dBc	
		30MHz Input			91		95	dBc	
		70MHz Input, $T_A = 25^\circ\text{C}$		85	96	85	97	dBc	
		70MHz Input	●	84	95	84	97	dBc	
		140MHz Input		89		91	dBc		
SFDR	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input		105		105		dBc	
		15MHz Input	●	95	105	94	105	dBc	
		30MHz Input			105		105	dBc	
		70MHz Input	●	94	104	93	103	dBc	
		140MHz Input			100		100	dBc	
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input		81.5		81.3		dBc	
		15MHz Input, $T_A = 25^\circ\text{C}$		80.3	81.2	80.2	81.1	dBFS	
		15MHz Input	●	80.2	80.8	80	80.7	dBFS	
		30MHz Input			80.9		80.8	dBFS	
		70MHz Input, $T_A = 25^\circ\text{C}$		79.3	80.3	79.6	80.4	dBFS	
		70MHz Input	●	79.2	80	79.4	80.1	dBFS	
		140MHz Input		78.8		78.8	dBFS		
SFDR	Spurious Free Dynamic Range at $-25\text{dBFS}$ Dither "OFF"	5MHz Input		105		105		dBFS	
		15MHz Input		105		105		dBFS	
		30MHz Input		105		105		dBFS	
		70MHz Input		105		105		dBFS	
		140MHz Input		100		100		dBFS	
SFDR	Spurious Free Dynamic Range at $-25\text{dBFS}$ Dither "ON"	5MHz Input		115		115		dBFS	
		15MHz Input	●	100	115	100	115	dBFS	
		30MHz Input			115		115	dBFS	
		70MHz Input			115		115	dBFS	
		140MHz Input			110		110	dBFS	
IMD	Intermodulation Distortion	$f_{IN1} = 14\text{MHz}$ , $f_{IN2} = 21\text{MHz}$ , $-7\text{dBFS}$		100		100		dBc	
		$f_{IN1} = 67\text{MHz}$ , $f_{IN2} = 74\text{MHz}$ , $-7\text{dBFS}$		96		97		dBc	

## COMMON MODE BIAS CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CM}$ Output Voltage	$I_{OUT} = 0$	● 1.475	1.575	1.675	V
$V_{CM}$ Output Tempco	$I_{OUT} = 0$		±60		ppm/°C
$V_{CM}$ Line Regulation	$3.135\text{V} \leq V_{DD} \leq 3.465\text{V}$		2.4		mV/V
$V_{CM}$ Output Resistance	$ I_{OUT}  \leq 0.8\text{mA}$		1.1		$\Omega$

## DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Encode Inputs (ENC<sup>+</sup>, ENC<sup>-</sup>)</b>						
$V_{ID}$	Differential Input Voltage	(Note 7)	● 0.2			V
$V_{ICM}$	Common Mode Input Voltage	Internally Set Externally Set (Note 7)	1.2	1.6	3	V V
$R_{IN}$	Input Resistance	(See Figure 2)		6		k $\Omega$
$C_{IN}$	Input Capacitance	(Note 7)		3		pF

### Logic Inputs

$V_{IH}$	High Level Input Voltage	$V_{DD} = 3.3\text{V}$	● 2			V
$V_{IL}$	Low Level Input Voltage	$V_{DD} = 3.3\text{V}$	●		0.8	V
$I_{IN}$	Digital Input Current	$V_{IN} = 0\text{V}$ to $V_{DD}$	●		±10	$\mu\text{A}$
$C_{IN}$	Digital Input Capacitance	(Note 7)		1.5		pF

### LOGIC OUTPUTS (CMOS MODE)

#### $OV_{DD} = 3.3\text{V}$

$V_{OH}$	High Level Output Voltage	$V_{DD} = 3.3\text{V}$	$I_O = -10\mu\text{A}$ $I_O = -200\mu\text{A}$	● 3.1	3.299 3.29	V V	
$V_{OL}$	Low Level Output Voltage	$V_{DD} = 3.3\text{V}$	$I_O = 160\mu\text{A}$ $I_O = 1.6\text{mA}$	●	0.01 0.10	0.4	V V
$I_{SOURCE}$	Output Source Current	$V_{OUT} = 0\text{V}$			-50	mA	
$I_{SINK}$	Output Sink Current	$V_{OUT} = 3.3\text{V}$			50	mA	

#### $OV_{DD} = 2.5\text{V}$

$V_{OH}$	High Level Output Voltage	$V_{DD} = 3.3\text{V}$	$I_O = -200\mu\text{A}$		2.49	V
$V_{OL}$	Low Level Output Voltage	$V_{DD} = 3.3\text{V}$	$I_O = 1.60\text{mA}$		0.1	V

#### $OV_{DD} = 1.8\text{V}$

$V_{OH}$	High Level Output Voltage	$V_{DD} = 3.3\text{V}$	$I_O = -200\mu\text{A}$		1.79	V
$V_{OL}$	Low Level Output Voltage	$V_{DD} = 3.3\text{V}$	$I_O = 1.60\text{mA}$		0.1	V

### LOGIC OUTPUTS (LVDS MODE)

#### STANDARD LVDS

$V_{OD}$	Differential Output Voltage	100 $\Omega$ Differential Load	●	247	350	454	mV
$V_{OS}$	Output Common Mode Voltage	100 $\Omega$ Differential Load	●	1.125	1.2	1.375	V

#### Low Power LVDS

$V_{OD}$	Differential Output Voltage	100 $\Omega$ Differential Load	●	125	175	250	mV
$V_{OS}$	Output Common Mode Voltage	100 $\Omega$ Differential Load	●	1.125	1.2	1.375	V

22165f

# LTC2216/LTC2215

## POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $A_{IN} = -1\text{dBFS}$  unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LTC2215			LTC2216			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{DD}$	Analog Supply Voltage	(Note 8)	● 3.135	3.3	3.465	3.135	3.3	3.465	V
$P_{SHDN}$	Shutdown Power	$SHDN = V_{DD}$		17		17			mW

### Standard LVDS Output Mode

$OV_{DD}$	Output Supply Voltage	(Note 8)	● 3	3.3	3.6	3	3.3	3.6	V
$I_{VDD}$	Analog Supply Current		●	217	290	300	370		mA
$I_{OVDD}$	Output Supply Current		●	75	90	75	90		mA
$P_{DIS}$	Power Dissipation		●	964	1254	1240	1518		mW

### Low Power LVDS Output Mode

$OV_{DD}$	Output Supply Voltage	(Note 8)	● 3	3.3	3.6	3	3.3	3.6	V
$I_{VDD}$	Analog Supply Current		●	215	290	298	370		mA
$I_{OVDD}$	Output Supply Current		●	42	50	42	50		mA
$P_{DIS}$	Power Dissipation		●	848	1122	1120	1386		mW

### CMOS Output Mode

$OV_{DD}$	Output Supply Voltage	(Note 8)	● 0.5		3.6	0.5		3.6	V
$I_{VDD}$	Analog Supply Current		●	212	290	295	370		mA
$P_{DIS}$	Power Dissipation		●	700	957	970	1220		mW

## TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LTC2215			LTC2216			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$f_S$	Sampling Frequency	(Note 8)	● 1		65	1		80	MHz
$t_L$	ENC Low Time	Duty Cycle Stabilizer Off (Note 7)	● 7.31	7.692	500	5.94	6.25	500	ns
		Duty Cycle Stabilizer On (Note 7)	● 5	7.692	500	4.06	6.25	500	ns
$t_H$	ENC High Time	Duty Cycle Stabilizer Off (Note 7)	● 7.31	7.692	500	5.94	6.25	500	ns
		Duty Cycle Stabilizer On (Note 7)	● 5	7.692	500	4.06	6.25	500	ns

### LVDS Output Mode (Standard and Low Power)

$t_D$	ENC to DATA Delay	(Note 7)	● 1.3	2.5	3.8	1.3	2.5	3.8	ns
$t_C$	ENC to CLKOUT Delay	(Note 7)	● 1.3	2.5	3.8	1.3	2.5	3.8	ns
$t_{SKEW}$	DATA to CLKOUT Skew	$(t_C - t_D)$ (Note 7)	● -0.6	0	0.6	-0.6	0	0.6	ns
$t_{RISE}$	Output Rise Time			0.5		0.5			ns
$t_{FALL}$	Output Fall Time			0.5		0.5			ns
Data Latency	Data Latency			7		7			Cycles

### CMOS Output Mode

$t_D$	ENC to DATA Delay	(Note 7)	● 1.3	2.7	4	1.3	2.7	4	ns
$t_C$	ENC to CLKOUT Delay	(Note 7)	● 1.3	2.7	4	1.3	2.7	4	ns
$t_{SKEW}$	DATA to CLKOUT Skew	$(t_C - t_D)$ (Note 7)	● -0.6	0	0.6	-0.6	0	0.6	ns
Data Latency	Data Latency	Full Rate CMOS Demuxed		7		7			Cycles

## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to GND, with GND and OGND shorted (unless otherwise noted).

**Note 3:** When these pin voltages are taken below GND or above  $V_{DD}$ , they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above  $V_{DD}$  without latching.

**Note 4:**  $V_{DD} = 3.3V$ ,  $f_{SAMPLE} = 65MHz$  (LTC2215) or 80MHz (LTC2216), LVDS outputs, differential  $ENC^+/ENC^- = 2V_{P-P}$  sine wave with 1.6V common mode, input range =  $2.75V_{P-P}$  with differential drive, unless otherwise specified.

**Note 5:** Integral nonlinearity is defined as the deviation of a code from a “best fit straight line” to the transfer curve. The deviation is measured from the center of the quantization band.

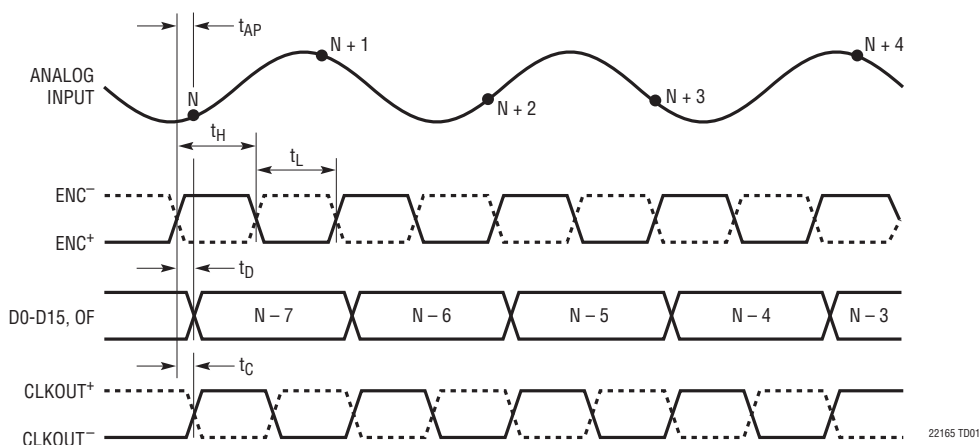
**Note 6:** Offset error is the offset voltage measured from  $-1/2LSB$  when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111 in 2’s complement output mode.

**Note 7:** Guaranteed by design, not subject to test.

**Note 8:** Recommended operating conditions.

## TIMING DIAGRAM

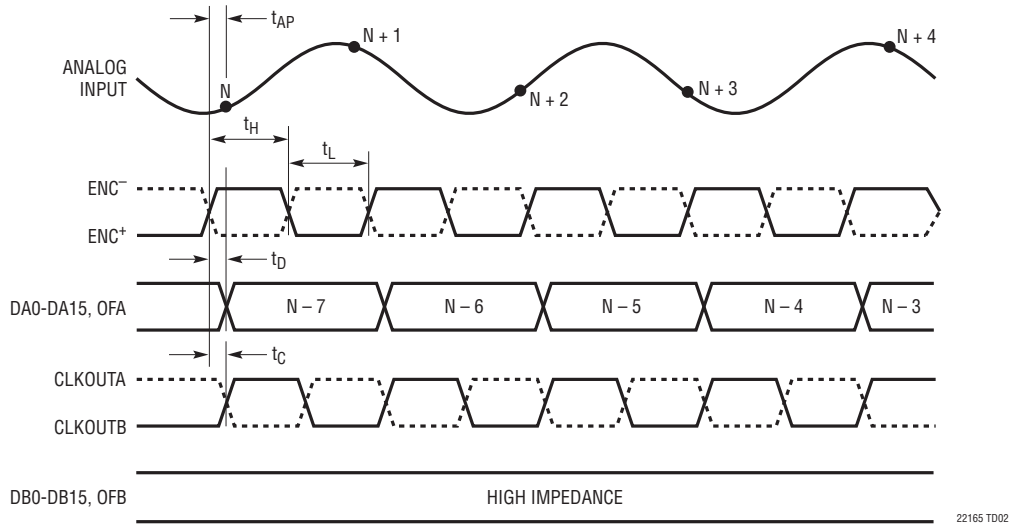
**LVDS Output Mode Timing**  
All Outputs are Differential and Have LVDS Levels



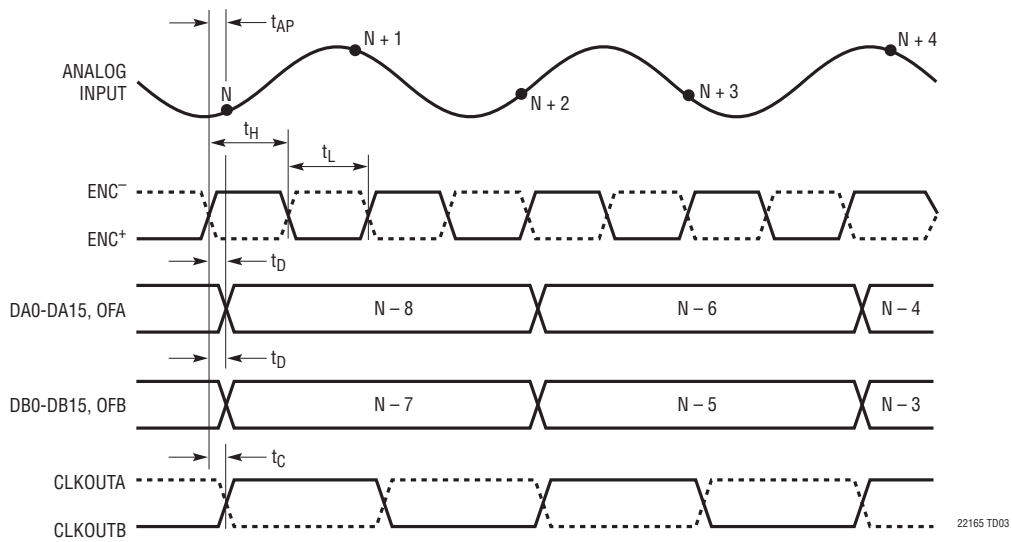


## TIMING DIAGRAMS

**Full-Rate CMOS Output Mode Timing**  
All Outputs are Single-Ended and Have CMOS Levels

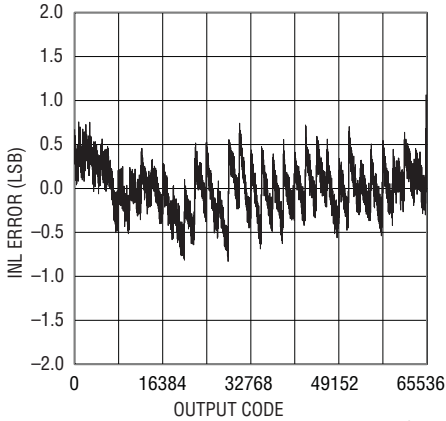


**Demultiplexed CMOS Output Mode Timing**  
All Outputs are Single-Ended and Have CMOS Levels

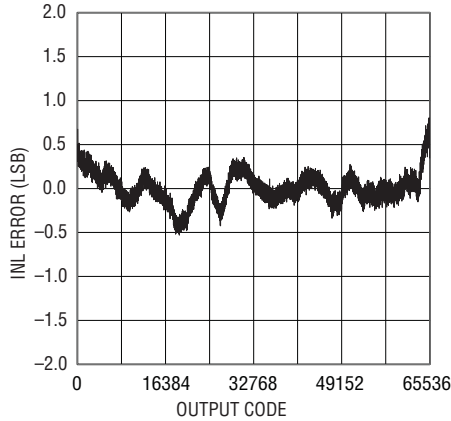


# TYPICAL PERFORMANCE CHARACTERISTICS

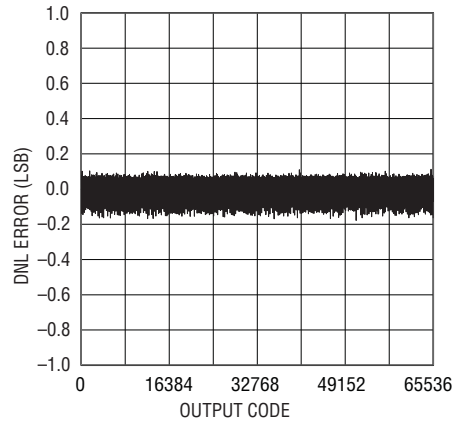
**LTC2216 Integral Nonlinearity (INL) vs Output Code, Dither "Off"**



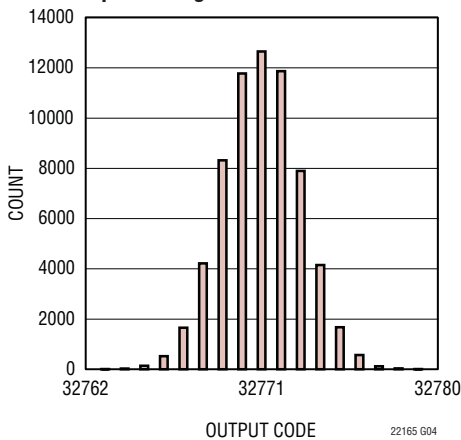
**LTC2216 Integral Nonlinearity (INL) vs Output Code, Dither "On"**



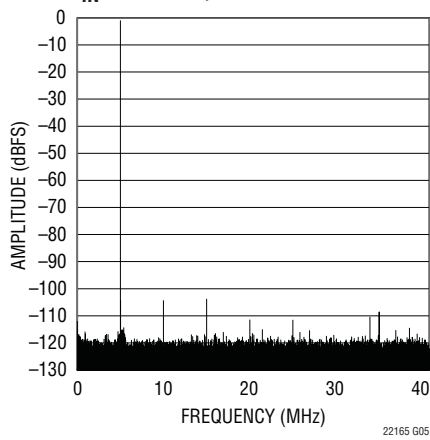
**LTC2216 Differential Nonlinearity (DNL) vs Output Code**



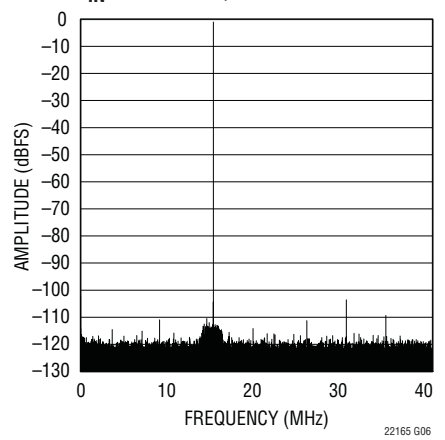
**LTC2216 AC Grounded Input Histogram**



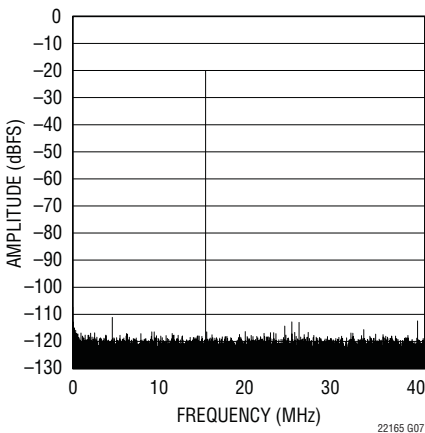
**LTC2216 64k Point FFT,  $f_{IN} = 4.9\text{MHz}$ ,  $-1\text{dBFS}$**



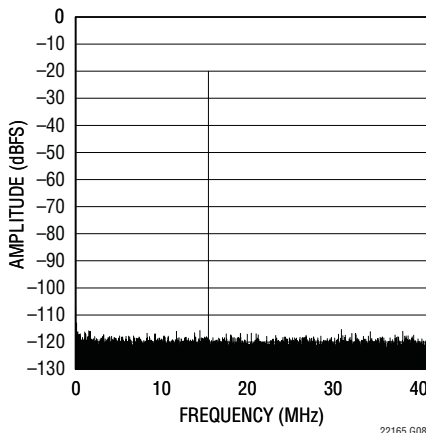
**LTC2216 64k Point FFT,  $f_{IN} = 15.1\text{MHz}$ ,  $-1\text{dBFS}$**



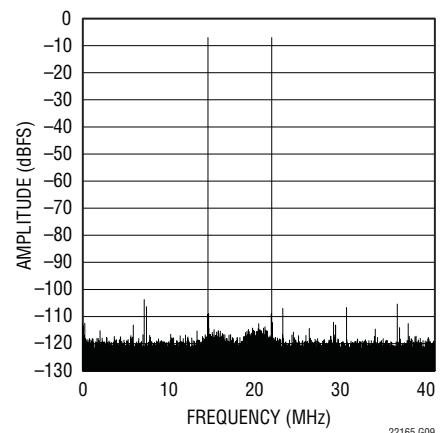
**LTC2216 64k Point FFT,  $f_{IN} = 15.1\text{MHz}$ ,  $-20\text{dBFS}$ , Dither "Off"**



**LTC2216 64k Point FFT,  $f_{IN} = 15.1\text{MHz}$ ,  $-20\text{dBFS}$ , Dither "On"**

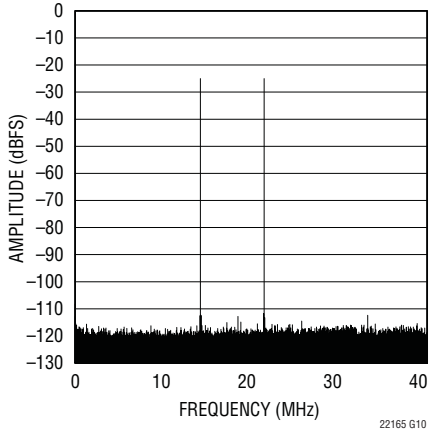


**LTC2216 64k Point 2-Tone FFT,  $f_{IN} = 14.25\text{MHz}$  and  $21.5\text{MHz}$ ,  $-7\text{dBFS}$**

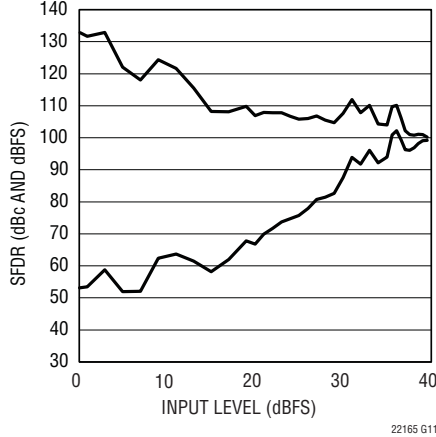


## TYPICAL PERFORMANCE CHARACTERISTICS

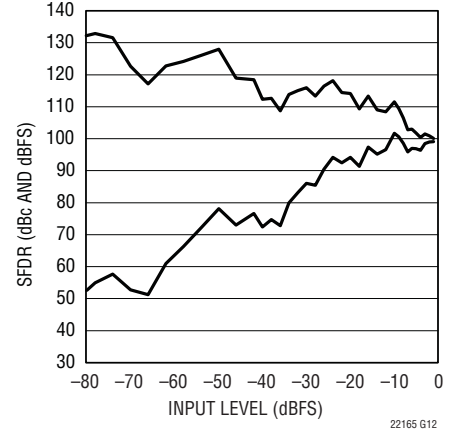
**LTC2216 64k Point 2-Tone FFT,  
f<sub>IN</sub> = 14.25MHz and 21.5MHz,  
-25dBFS, Dither "On"**



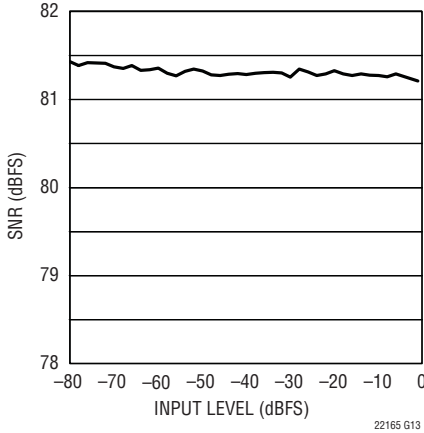
**LTC2216 SFDR vs Input Level,  
f<sub>IN</sub> = 15.2MHz, Dither "Off"**



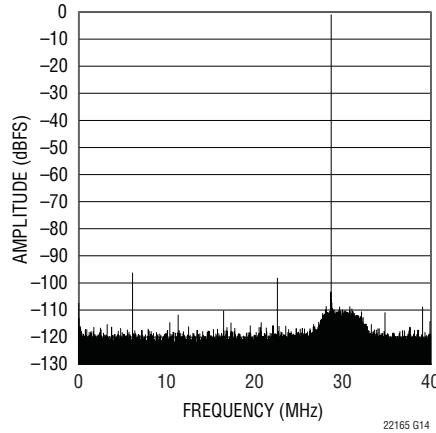
**LTC2216 SFDR vs Input Level,  
f<sub>IN</sub> = 15.2MHz, Dither "On"**



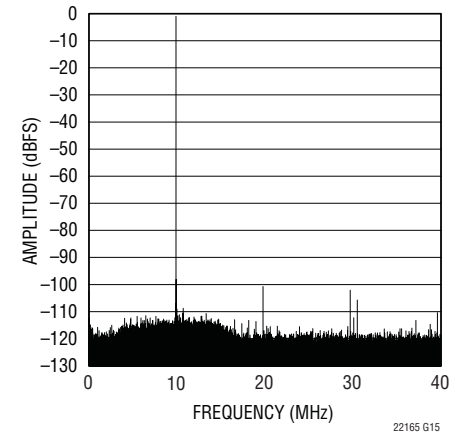
**LTC2216 SNR vs Input Level,  
f<sub>IN</sub> = 15.2MHz**



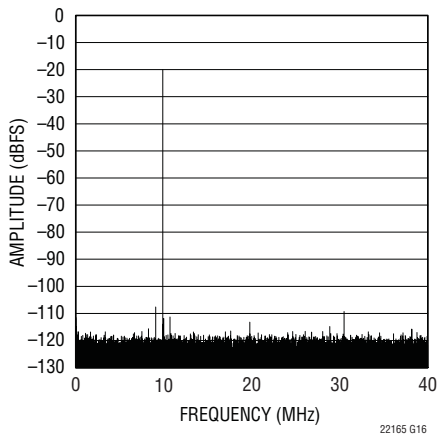
**LTC2216 64k Point FFT,  
f<sub>IN</sub> = 28.7MHz, -1dBFS**



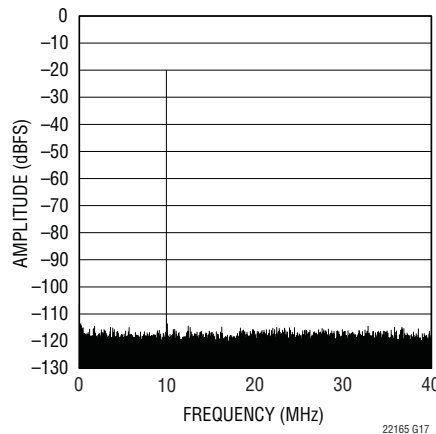
**LTC2216 64k Point FFT,  
f<sub>IN</sub> = 70.2MHz, -1dBFS**



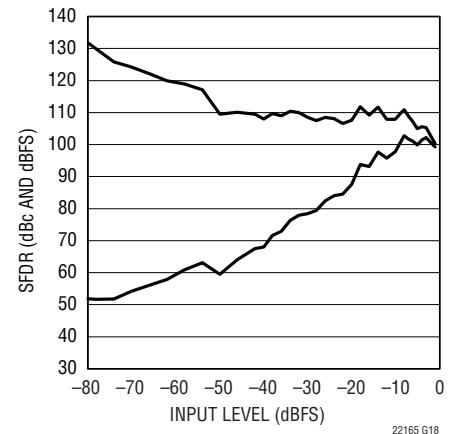
**LTC2216 64k Point FFT,  
f<sub>IN</sub> = 70.1MHz, -20dBFS, Dither "Off"**



**LTC2216 64k Point FFT,  
f<sub>IN</sub> = 70.1MHz, -20dBFS, Dither "On"**

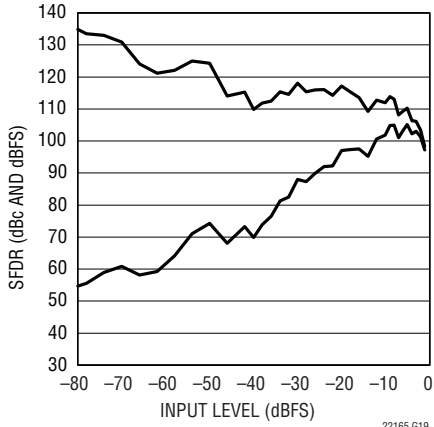


**LTC2216 SFDR vs Input Level,  
f<sub>IN</sub> = 70.5MHz, Dither "Off"**



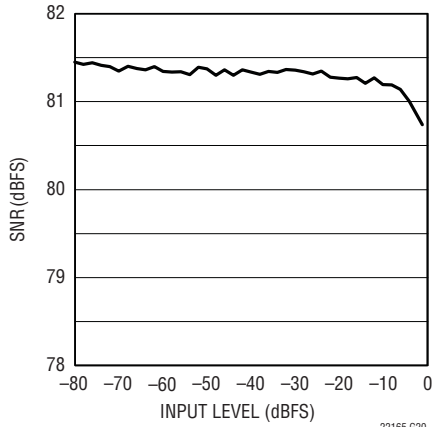
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2216 SFDR vs Input Level,  
 $f_{IN} = 70.5\text{MHz}$ , Dither "On"



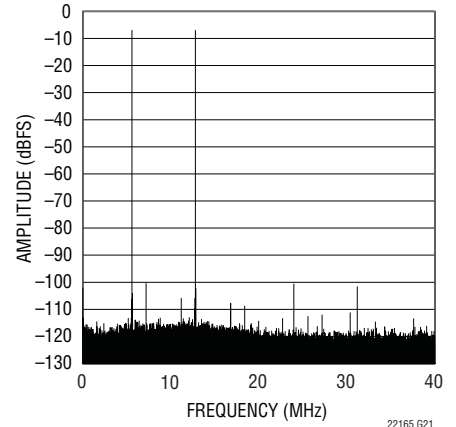
22165 G19

LTC2216 SNR vs Input Level,  
 $f_{IN} = 70.5\text{MHz}$



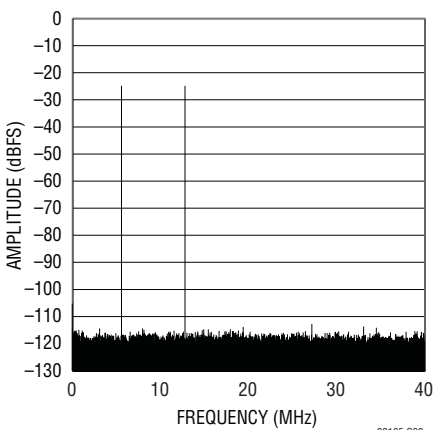
22165 G20

LTC2216 64k Point 2-Tone FFT,  
 $f_{IN} = 67.2\text{MHz}$  and  $74.4\text{MHz}$ ,  
 $-7\text{dBFS}$



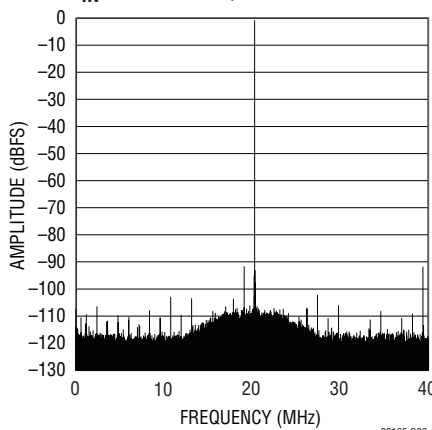
22165 G21

LTC2216 64k Point 2-Tone FFT,  
 $f_{IN} = 67.2\text{MHz}$  and  $74.4\text{MHz}$ ,  
 $-25\text{dBFS}$ , Dither "On"



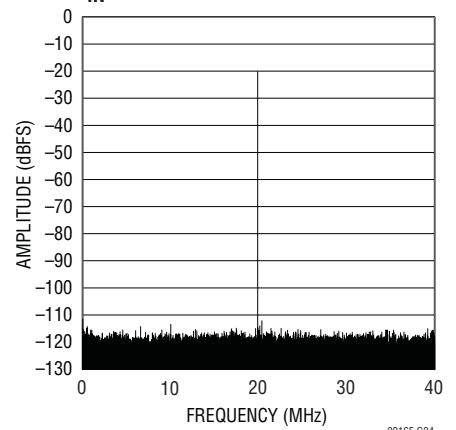
22165 G22

LTC2216 64k Point FFT,  
 $f_{IN} = 140.5\text{MHz}$ ,  $-1\text{dBFS}$



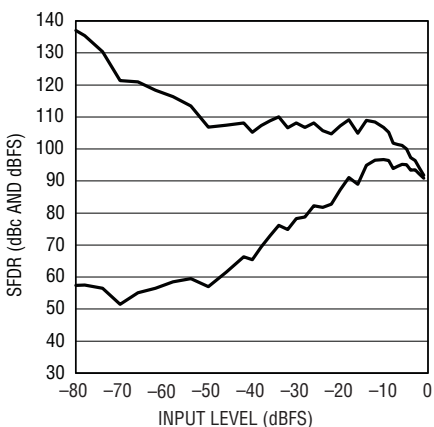
22165 G23

LTC2216 64k Point FFT,  
 $f_{IN} = 140.1\text{MHz}$ ,  $-20\text{dBFS}$ , Dither "On"



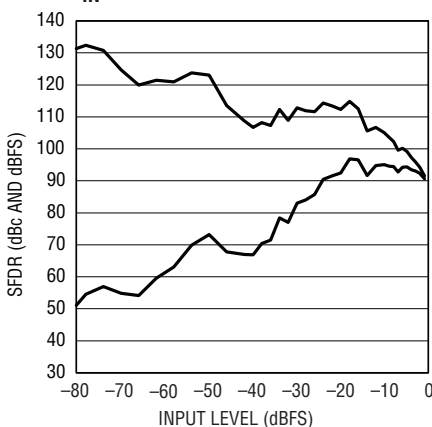
22165 G24

LTC2216 SFDR vs Input Level,  
 $f_{IN} = 140.5\text{MHz}$ , Dither "Off"



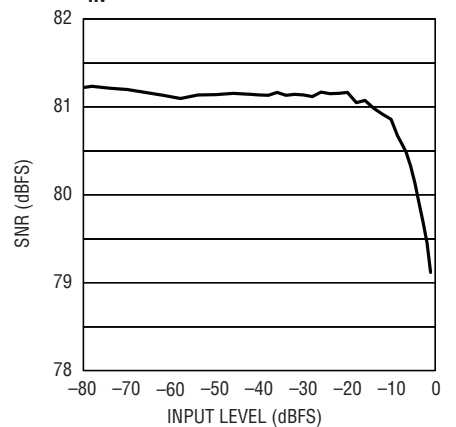
22165 G25

LTC2216 SFDR vs Input Level,  
 $f_{IN} = 140.5\text{MHz}$ , Dither "On"



22165 G26

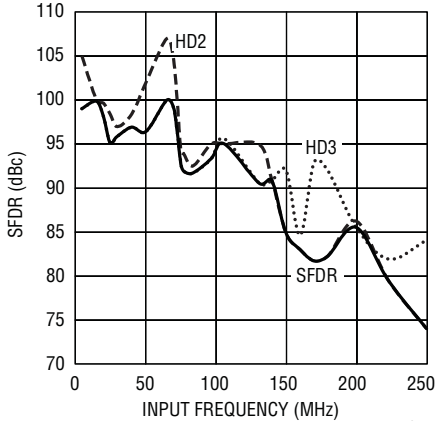
LTC2216 SNR vs Input Level,  
 $f_{IN} = 140.5\text{MHz}$



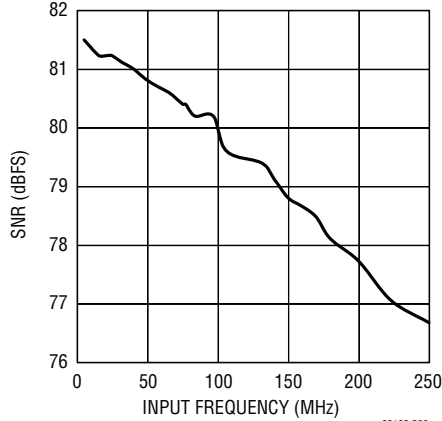
22165 G27

## TYPICAL PERFORMANCE CHARACTERISTICS

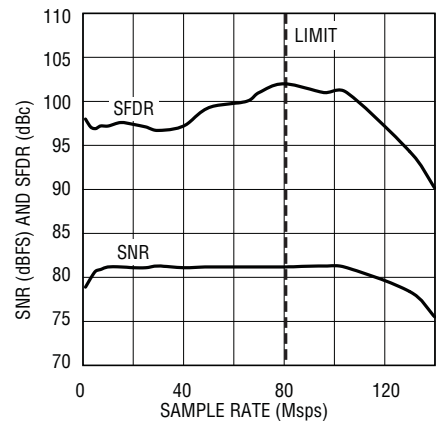
**LTC2216 SFDR (HD2 and HD3) vs Input Frequency**



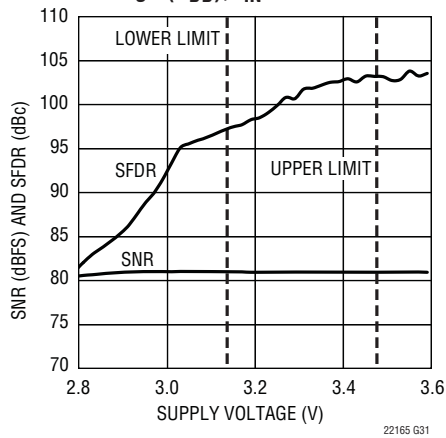
**LTC2216 SNR vs Input Frequency**



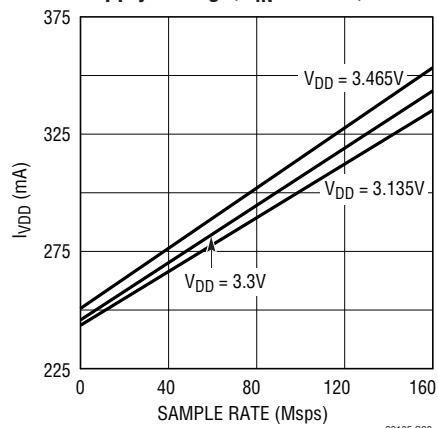
**LTC2216 SNR and SFDR vs Sample Rate,  $f_{IN} = 5.2\text{MHz}$**



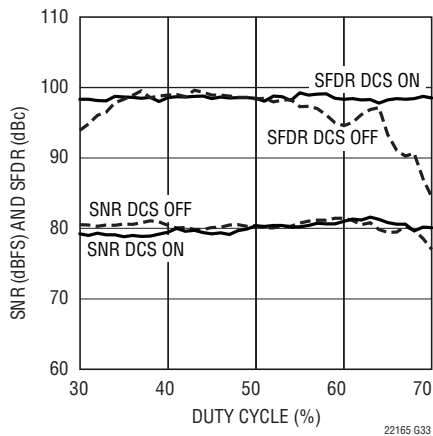
**LTC2216 SNR and SFDR vs Supply Voltage ( $V_{DD}$ ),  $f_{IN} = 5.1\text{MHz}$**



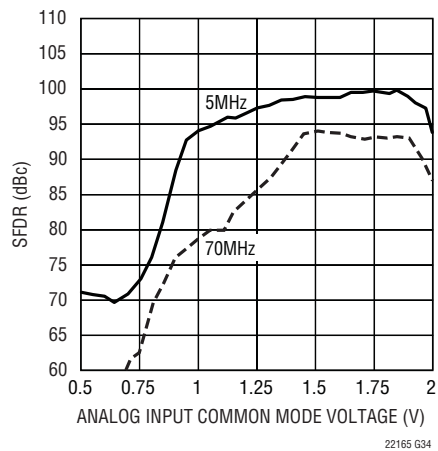
**LTC2216  $I_{VDD}$  vs Sample Rate and Supply Voltage,  $f_{IN} = 5\text{MHz}$ ,  $-1\text{dBFS}$**



**LTC2216 SNR and SFDR vs Clock Duty Cycle,  $f_{IN} = 5.2\text{MHz}$**

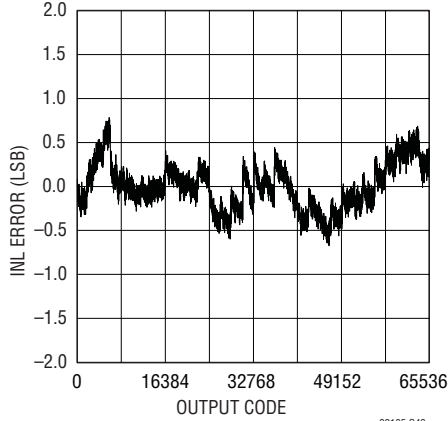


**LTC2216 SFDR vs Analog Input Common Mode Voltage, 5MHz and 70MHz,  $-1\text{dBFS}$**

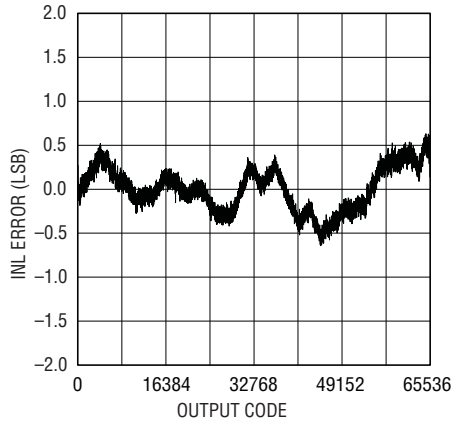


# TYPICAL PERFORMANCE CHARACTERISTICS

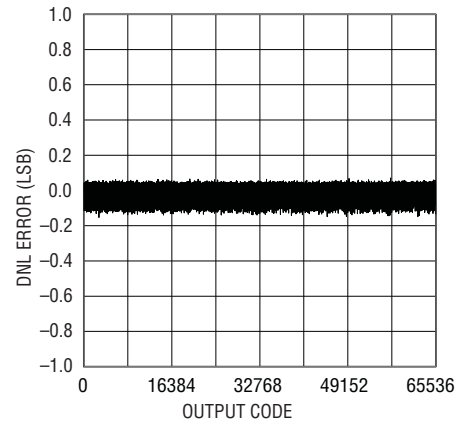
**LTC2215 Integral Nonlinearity (INL) vs Output Code, Dither "Off"**



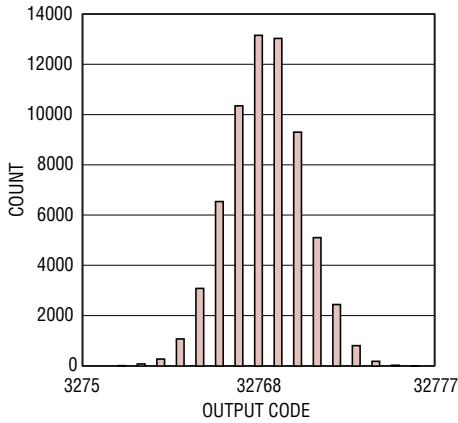
**LTC2215 Integral Nonlinearity (INL) vs Output Code, Dither "On"**



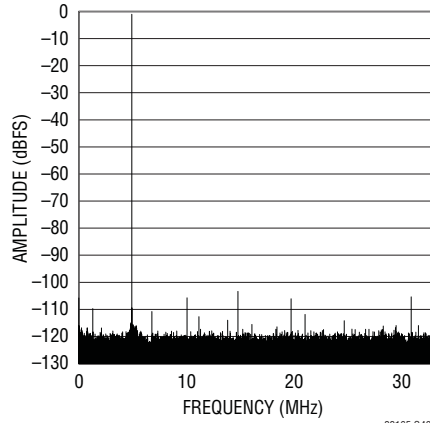
**LTC2215 Differential Nonlinearity (DNL) vs Output Code**



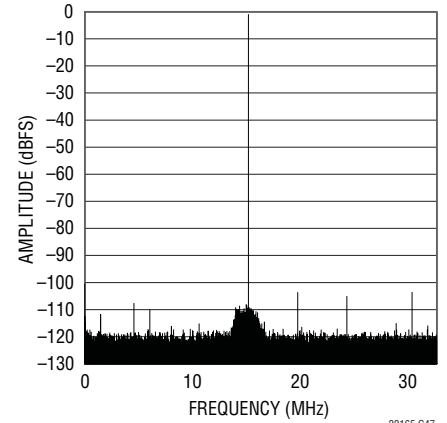
**LTC2215 AC Grounded Input Histogram**



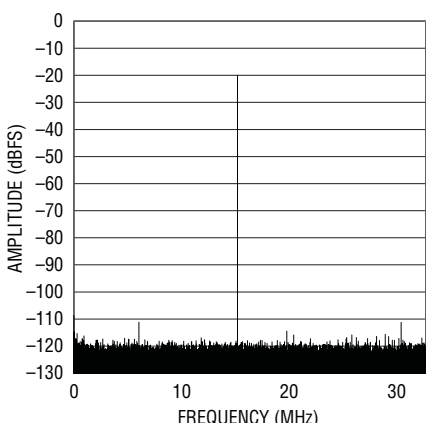
**LTC2215 64k Point FFT,  $f_{IN} = 4.9\text{MHz}$ ,  $-1\text{dBFS}$**



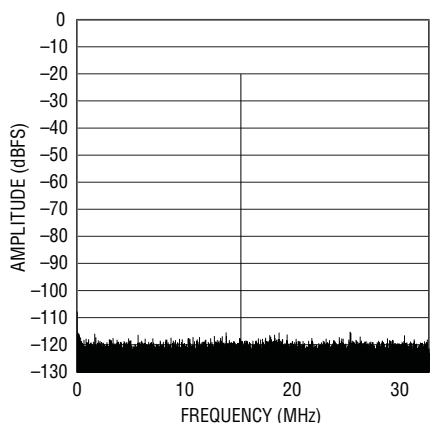
**LTC2215 64k Point FFT,  $f_{IN} = 15.1\text{MHz}$ ,  $-1\text{dBFS}$**



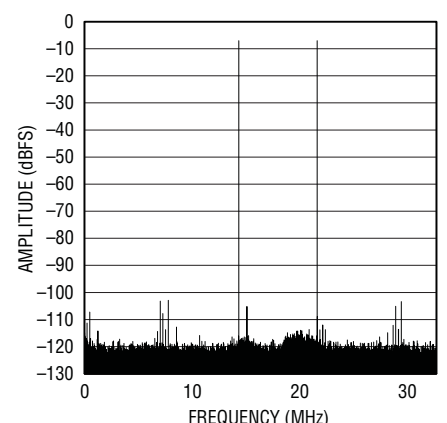
**LTC2215 64k Point FFT,  $f_{IN} = 15.1\text{MHz}$ ,  $-20\text{dBFS}$ , Dither "Off"**



**LTC2215 64k Point FFT,  $f_{IN} = 15.1\text{MHz}$ ,  $-20\text{dBFS}$ , Dither "On"**

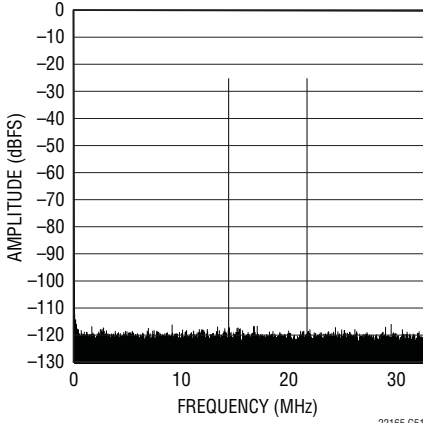


**LTC2215 64k Point 2-Tone FFT,  $f_{IN} = 14.25\text{MHz}$  and  $21.5\text{MHz}$ ,  $-7\text{dBFS}$**

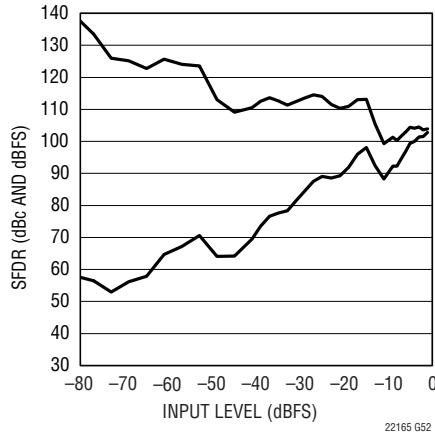


## TYPICAL PERFORMANCE CHARACTERISTICS

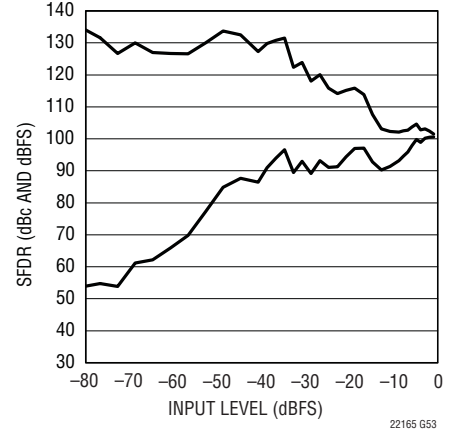
**LTC2215 64k Point 2-Tone FFT,  
 $f_{IN} = 14.25\text{MHz}$  and  $21.5\text{MHz}$ ,  
 $-25\text{dBFS}$ , Dither "On"**



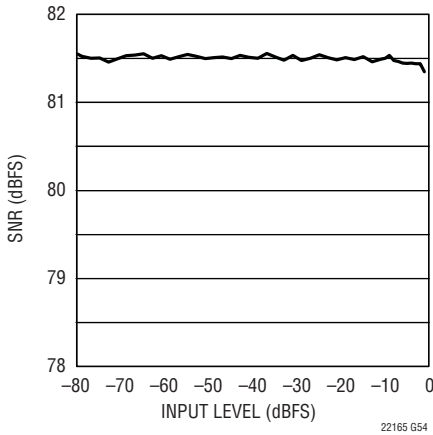
**LTC2215 SFDR vs Input Level,  
 $f_{IN} = 15.2\text{MHz}$ , Dither "Off"**



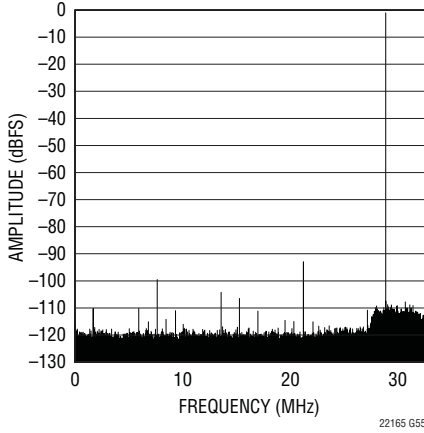
**LTC2215 SFDR vs Input Level,  
 $f_{IN} = 15.2\text{MHz}$ , Dither "On"**



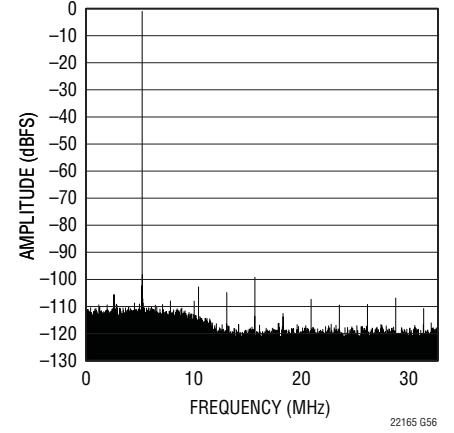
**LTC2215 SNR vs Input Level,  
 $f_{IN} = 15.2\text{MHz}$**



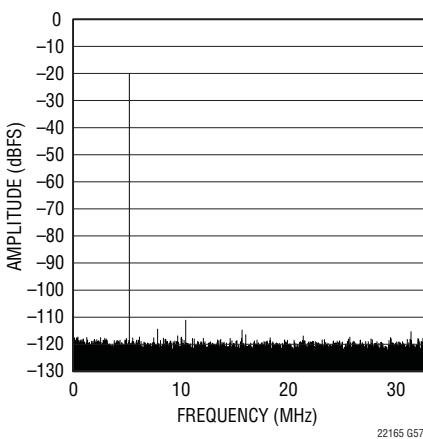
**LTC2215 64k Point FFT,  
 $f_{IN} = 28.7\text{MHz}$ ,  $-1\text{dBFS}$**



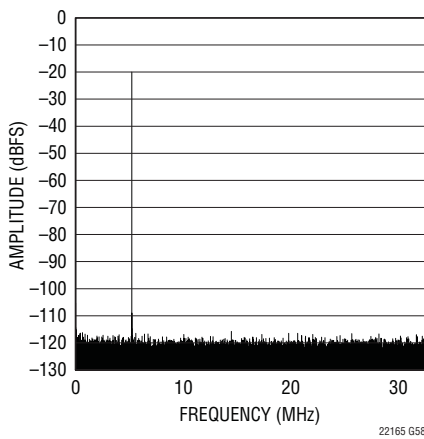
**LTC2215 64k Point FFT,  
 $f_{IN} = 70.2\text{MHz}$ ,  $-1\text{dBFS}$**



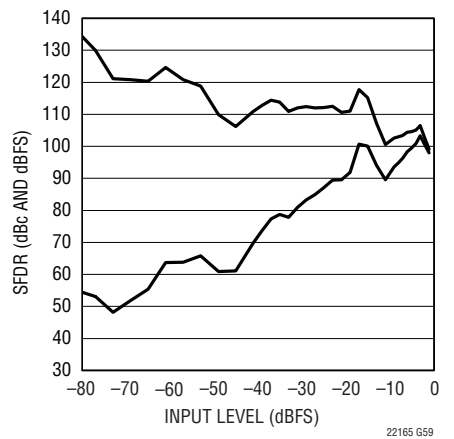
**LTC2215 64k Point FFT,  
 $f_{IN} = 70.1\text{MHz}$ ,  $-20\text{dBFS}$ ,  
 Dither "Off"**



**LTC2215 64k Point FFT,  
 $f_{IN} = 70.1\text{MHz}$ ,  $-20\text{dBFS}$ ,  
 Dither "On"**

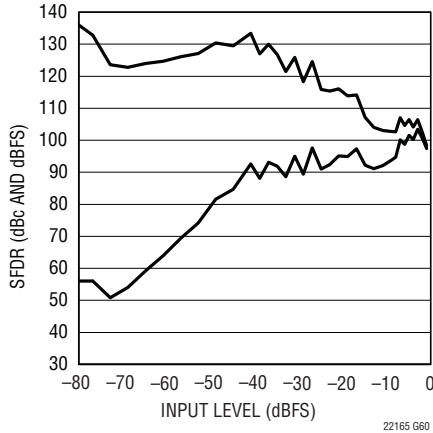


**LTC2215 SFDR vs Input Level,  
 $f_{IN} = 70.5\text{MHz}$ , Dither "Off"**

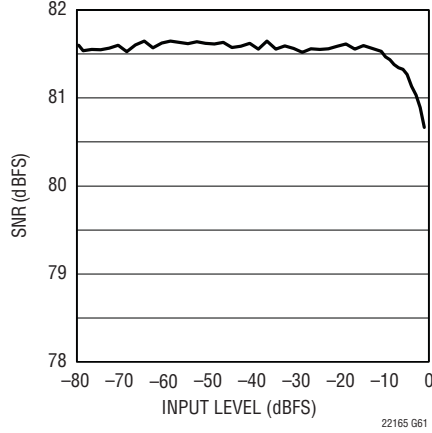


# TYPICAL PERFORMANCE CHARACTERISTICS

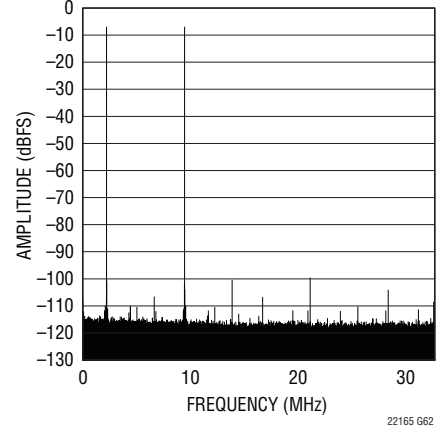
**LTC2215 SFDR vs Input Level,  
 $f_{IN} = 70.5\text{MHz}$ , Dither "On"**



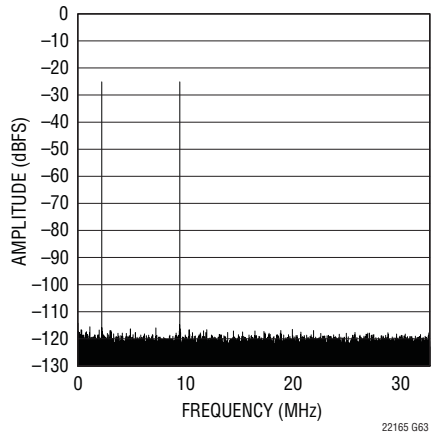
**LTC2215 SNR vs Input Level,  
 $f_{IN} = 70.5\text{MHz}$**



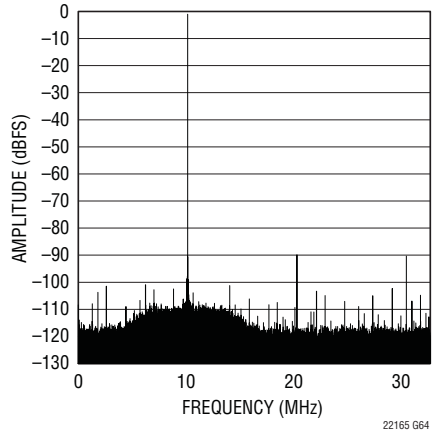
**LTC2215 64k Point 2-Tone FFT,  $f_{IN} = 67.2\text{MHz}$  and  $74.4\text{MHz}$ , -7dBFS**



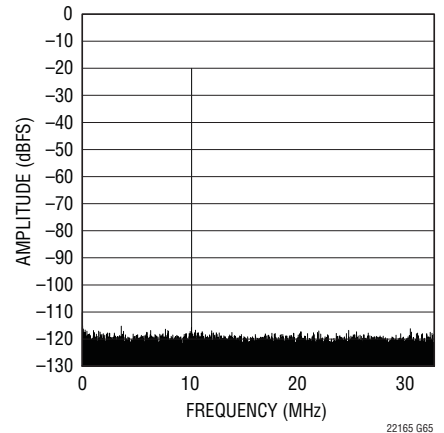
**LTC2215 64k Point 2-Tone FFT,  
 $f_{IN} = 67.2\text{MHz}$  and  $74.4\text{MHz}$ ,  
-25dBFS, Dither "On"**



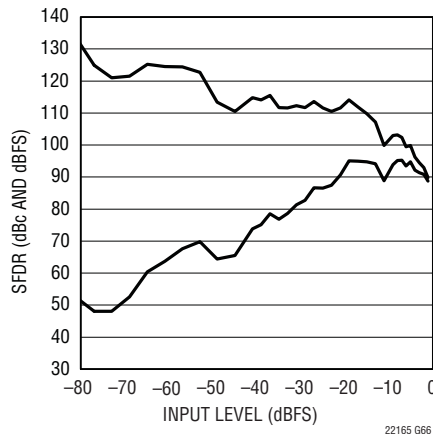
**LTC2215 64k Point FFT,  
 $f_{IN} = 140.5\text{MHz}$ , -1dBFS**



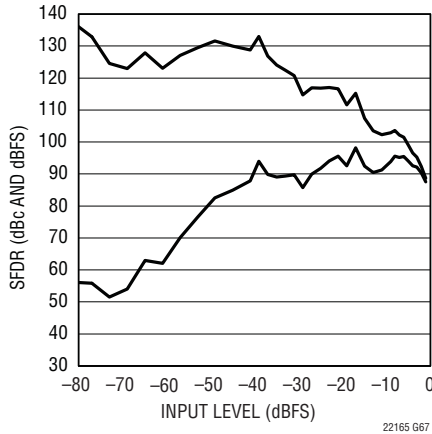
**LTC2215 64k Point FFT,  
 $f_{IN} = 140.1\text{MHz}$ , -20dBFS,  
Dither "On"**



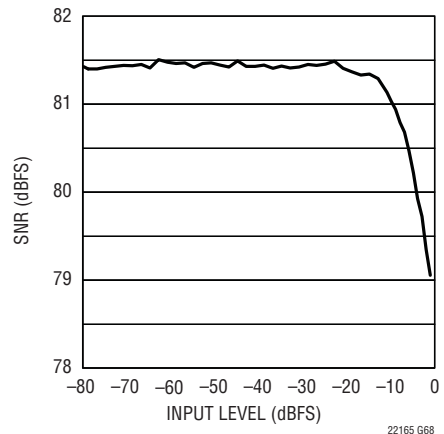
**LTC2215 SFDR vs Input Level,  
 $f_{IN} = 140.5\text{MHz}$ , Dither "Off"**



**LTC2215 SFDR vs Input Level,  
 $f_{IN} = 140.5\text{MHz}$ , Dither "On"**



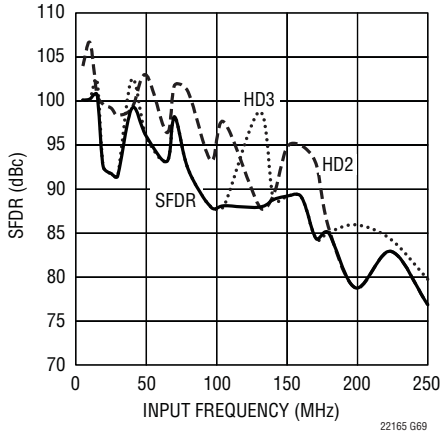
**LTC2215 SNR vs Input Level,  
 $f_{IN} = 140.5\text{MHz}$**





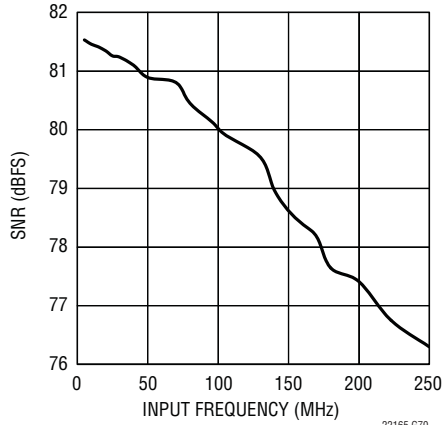
## TYPICAL PERFORMANCE CHARACTERISTICS

**LTC2215 SFDR (HD2 and HD3) vs Input Frequency**



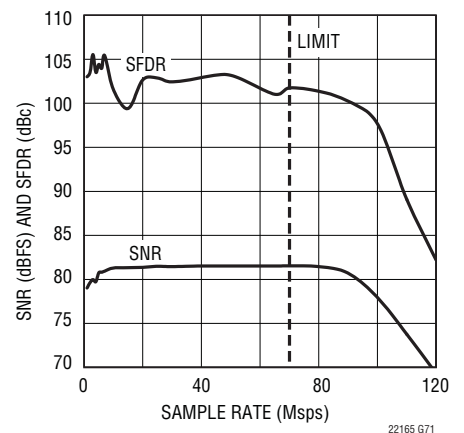
22165 G69

**LTC2215 SNR vs Input Frequency**



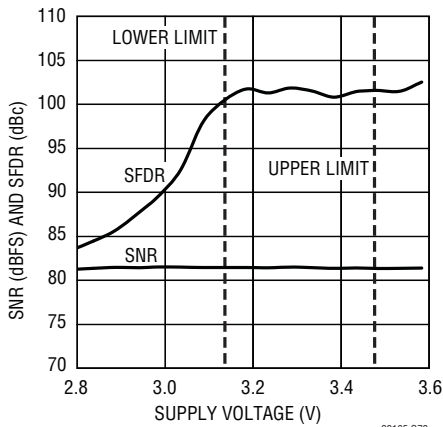
22165 G70

**LTC2215 SNR and SFDR vs Sample Rate,  $f_{IN} = 5.2\text{MHz}$**



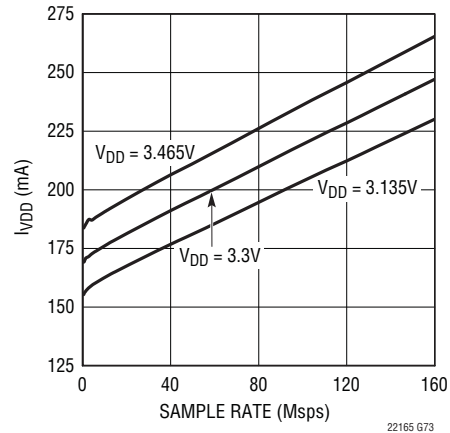
22165 G71

**LTC2215 SNR and SFDR vs Supply Voltage ( $V_{DD}$ ),  $f_{IN} = 5.1\text{MHz}$**



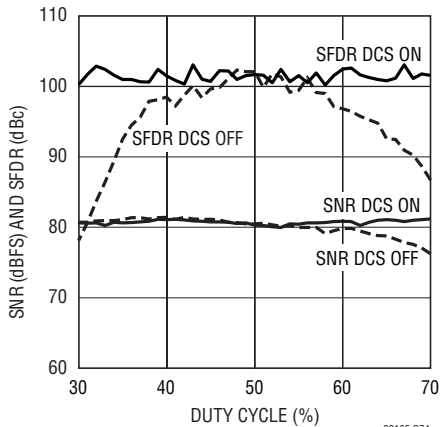
22165 G72

**LTC2215  $I_{VDD}$  vs Sample Rate and Supply Voltage,  $f_{IN} = 5\text{MHz}$ ,  $-1\text{dBFS}$**



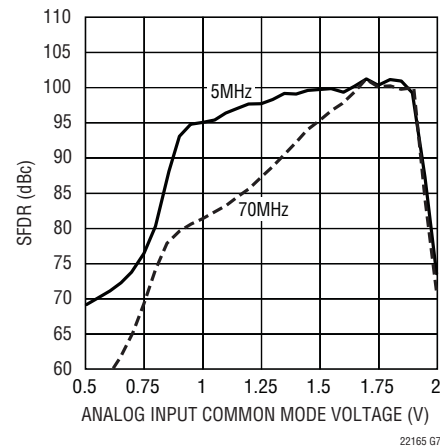
22165 G73

**LTC2215 SNR and SFDR vs Clock Duty Cycle,  $f_{IN} = 5.2\text{MHz}$**



22165 G74

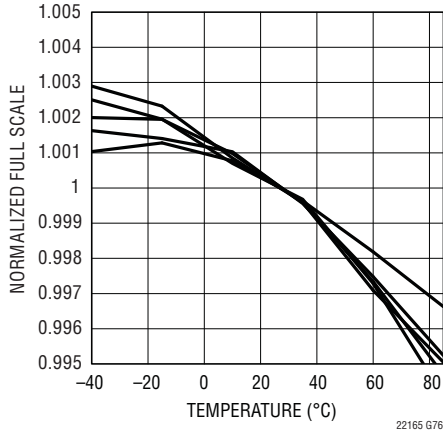
**LTC2215 SFDR vs Analog Input Common Mode Voltage, 5MHz and 70MHz,  $-1\text{dBFS}$**



22165 G75

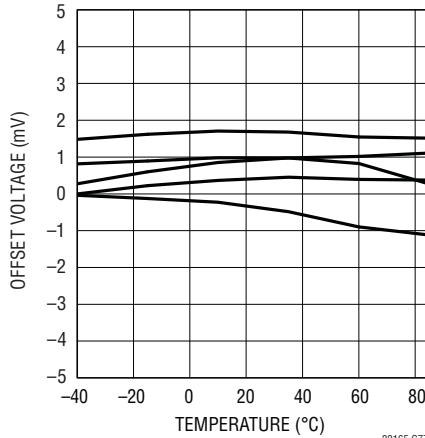
# TYPICAL PERFORMANCE CHARACTERISTICS

**LTC2216/LTC2215 Normalized Full-Scale vs Temperature, Internal Reference, 5 Units**



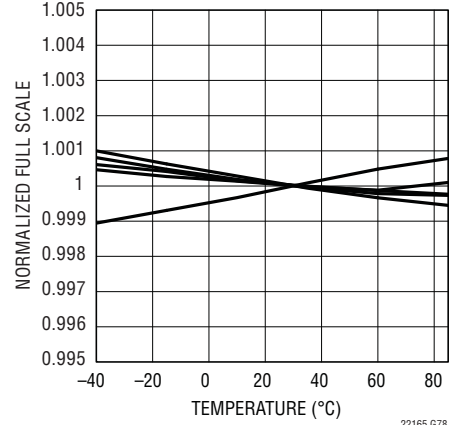
22165 G76

**LTC2216/LTC2215 Input Offset Voltage vs Temperature, Internal Reference, 5 Units**



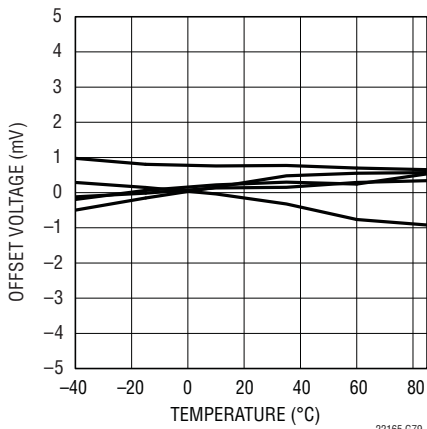
22165 G77

**LTC2216/LTC2215 Normalized Full-Scale vs Temperature, External Reference, 5 Units**



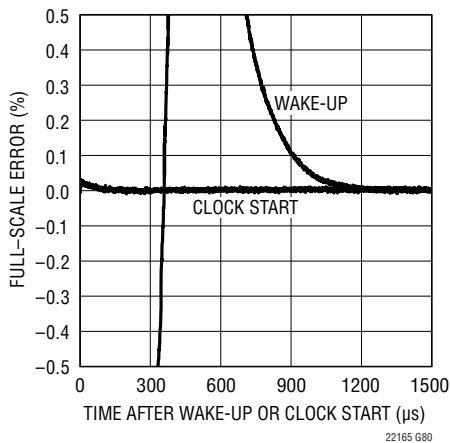
22165 G78

**LTC2216/LTC2215 Input Offset Voltage vs Temperature, External Reference, 5 Units**



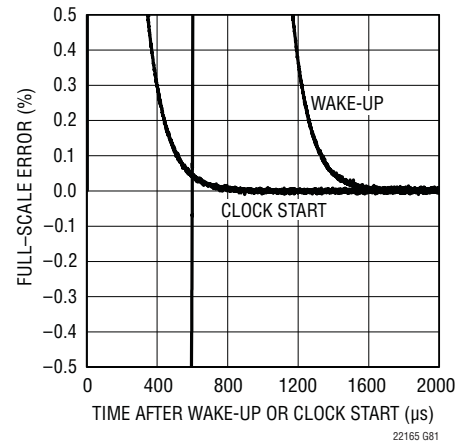
22165 G79

**LTC2216/LTC2215 Mid-Scale Settling After Wake-Up from Shutdown or Starting Encode Clock**



22165 G80

**LTC2216/LTC2215 Full-Scale Settling After Wake-Up from Shutdown or Starting Encode Clock**



22165 G81

## PIN FUNCTIONS

### For CMOS Mode, Full Rate or Demultiplexed

**SENSE (Pin 1):** Reference Mode Select and External Reference Input. Tie SENSE to  $V_{DD}$  to select the internal 2.5V bandgap reference. An external reference of 2.5V or 1.25V may be used; both reference values will set a full-scale ADC range of 2.75V.

**GND (Pins 2, 4, 7, 10, 11, 14, 18):** ADC Power Ground.

**$V_{CM}$  (Pin 3):** 1.575V Output. Optimum voltage for input common mode. Must be bypassed to ground with a minimum of 2.2 $\mu$ F. Ceramic chip capacitors are recommended.

**$V_{DD}$  (Pins 5, 6, 15, 16, 17):** 3.3V Analog Supply Pin. Bypass to GND with 1 $\mu$ F ceramic chip capacitors.

**$A_{IN}^+$  (Pin 8):** Positive Differential Analog Input.

**$A_{IN}^-$  (Pin 9):** Negative Differential Analog Input.

**ENC<sup>+</sup> (Pin 12):** Positive Differential Encode Input. The sampled analog input is held on the rising edge of ENC<sup>+</sup>. Internally biased to 1.6V through a 6.2k $\Omega$  resistor. Output data can be latched on the rising edge of ENC<sup>+</sup>.

**ENC<sup>-</sup> (Pin 13):** Negative Differential Encode Input. The sampled analog input is held on the falling edge of ENC<sup>-</sup>. Internally biased to 1.6V through a 6.2k $\Omega$  resistor. Bypass to ground with a 0.1 $\mu$ F capacitor for a single-ended Encode signal.

**SHDN (Pin 19):** Power Shutdown Pin. SHDN = low results in normal operation. SHDN = high results in powered down analog circuitry and the digital outputs are placed in a high impedance state.

**DITH (Pin 20):** Internal Dither Enable Pin. DITH = low disables internal dither. DITH = high enables internal dither. Refer to Internal Dither section of this data sheet for details on dither operation.

**DB0-DB15 (Pins 21-30 and 33-38):** Digital Outputs, B Bus. DB15 is the MSB. Active in demultiplexed mode. The B bus is in high impedance state in full rate CMOS mode.

**OGND (Pins 31 and 50):** Output Driver Ground.

**$OV_{DD}$  (Pins 32 and 49):** Positive Supply for the Output Drivers. Bypass to ground with 1 $\mu$ F capacitor.

**OFB (Pin 39):** Over/Under Flow Digital Output for the B Bus. OFB is high when an over or under flow has occurred on the B bus. At high impedance state in full rate CMOS mode.

**CLKOUTB (Pin 40):** Data Valid Output. CLKOUTB will toggle at the sample rate in full rate CMOS mode or at 1/2 the sample rate in demultiplexed mode. Latch the data on the falling edge of CLKOUTB.

**CLKOUTA (Pin 41):** Inverted Data Valid Output. CLKOUTA will toggle at the sample rate in full rate CMOS mode or at 1/2 the sample rate in demultiplexed mode. Latch the data on the rising edge of CLKOUTA.

**DA0-DA15 (Pins 42-48 and 51-59):** Digital Outputs, A Bus. DA15 is the MSB. Output bus for full rate CMOS mode and demultiplexed mode.

**OFA (Pin 60):** Over/Under Flow Digital Output for the A Bus. OFA is high when an over or under flow has occurred on the A bus.

**LVDS (Pin 61):** Data Output Mode Select Pin. Connecting LVDS to 0V selects full rate CMOS mode. Connecting LVDS to 1/3 $V_{DD}$  selects demultiplexed CMOS mode. Connecting LVDS to 2/3 $V_{DD}$  selects Low Power LVDS mode. Connecting LVDS to  $V_{DD}$  selects Standard LVDS mode.

**MODE (Pin 62):** Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects offset binary output format and disables the clock duty cycle stabilizer. Connecting MODE to 1/3 $V_{DD}$  selects offset binary output format and enables the clock duty cycle stabilizer. Connecting MODE to 2/3 $V_{DD}$  selects 2's complement output format and enables the clock duty cycle stabilizer. Connecting MODE to  $V_{DD}$  selects 2's complement output format and disables the clock duty cycle stabilizer.

**RAND (Pin 63):** Digital Output Randomization Selection Pin. RAND low results in normal operation. RAND high selects D1-D15 to be EXCLUSIVE-ORed with D0 (the LSB). The output can be decoded by again applying an XOR operation between the LSB and all other bits. This mode of operation reduces the effects of digital output interference.

**NC (Pin 64):** Not Connected Internally. For pin compatibility with the LTC2208 this pin should be connected to GND or  $V_{DD}$  as required. Otherwise no connection.

**GND (Exposed Pad):** ADC Power Ground. The exposed pad on the bottom of the package must be soldered to ground.

## PIN FUNCTIONS

### For LVDS Mode. STANDARD or LOW POWER

**SENSE (Pin 1):** Reference Mode Select and External Reference Input. Tie SENSE to  $V_{DD}$  to select the internal 2.5V bandgap reference. An external reference of 2.5V or 1.25V may be used; both reference values will set a full-scale ADC range of 2.75V.

**GND (Pins 2, 4, 7, 10, 11, 14, 18):** ADC Power Ground.

**$V_{CM}$  (Pin 3):** 1.575V Output. Optimum voltage for input common mode. Must be bypassed to ground with a minimum of 2.2 $\mu$ F. Ceramic chip capacitors are recommended.

**$V_{DD}$  (Pins 5, 6, 15, 16, 17):** 3.3V Analog Supply Pin. Bypass to GND with 1 $\mu$ F ceramic chip capacitors.

**$A_{IN}^+$  (Pin 8):** Positive Differential Analog Input.

**$A_{IN}^-$  (Pin 9):** Negative Differential Analog Input.

**ENC<sup>+</sup> (Pin 12):** Positive Differential Encode Input. The sampled analog input is held on the rising edge of ENC<sup>+</sup>. Internally biased to 1.6V through a 6.2k $\Omega$  resistor. Output data can be latched on the rising edge of ENC<sup>+</sup>.

**ENC<sup>-</sup> (Pin 13):** Negative Differential Encode Input. The sampled analog input is held on the falling edge of ENC<sup>-</sup>. Internally biased to 1.6V through a 6.2k $\Omega$  resistor. Bypass to ground with a 0.1 $\mu$ F capacitor for a single-ended Encode signal.

**SHDN (Pin 19):** Power Shutdown Pin. SHDN = low results in normal operation. SHDN = high results in powered down analog circuitry and the digital outputs are set in high impedance state.

**DITH (Pin 20):** Internal Dither Enable Pin. DITH = low disables internal dither. DITH = high enables internal dither. Refer to Internal Dither section of the data sheet for details on dither operation.

**D0<sup>-</sup>/D0<sup>+</sup> to D15<sup>-</sup>/D15<sup>+</sup> (Pins 21-30, 33-38, 41-48 and 51-58):** LVDS Digital Outputs. All LVDS outputs require differential 100 $\Omega$  termination resistors at the LVDS receiver. D15<sup>+</sup>/D15<sup>-</sup> is the MSB.

**OGND (Pins 31 and 50):** Output Driver Ground.

**$OV_{DD}$  (Pins 32 and 49):** Positive Supply for the Output Drivers. Bypass to ground with 0.1 $\mu$ F capacitor.

**CLKOUT<sup>-</sup>/CLKOUT<sup>+</sup> (Pins 39 and 40):** LVDS Data Valid Output. Latch data on the rising edge of CLKOUT<sup>+</sup>, falling edge of CLKOUT<sup>-</sup>.

**OF<sup>-</sup>/OF<sup>+</sup> (Pins 59 and 60):** Over/Under Flow Digital Output OF is high when an over or under flow has occurred.

**LVDS (Pin 61):** Data Output Mode Select Pin. Connecting LVDS to 0V selects full rate CMOS mode. Connecting LVDS to 1/3 $V_{DD}$  selects demultiplexed CMOS mode. Connecting LVDS to 2/3 $V_{DD}$  selects Low Power LVDS mode. Connecting LVDS to  $V_{DD}$  selects Standard LVDS mode.

**MODE (Pin 62):** Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects offset binary output format and disables the clock duty cycle stabilizer. Connecting MODE to 1/3 $V_{DD}$  selects offset binary output format and enables the clock duty cycle stabilizer. Connecting MODE to 2/3 $V_{DD}$  selects 2's complement output format and enables the clock duty cycle stabilizer. Connecting MODE to  $V_{DD}$  selects 2's complement output format and disables the clock duty cycle stabilizer.

**RAND (Pin 63):** Digital Output Randomization Selection Pin. RAND low results in normal operation. RAND high selects D1-D15 to be EXCLUSIVE-ORed with D0 (the LSB). The output can be decoded by again applying an XOR operation between the LSB and all other bits. The mode of operation reduces the effects of digital output interference.

**NC (Pin 64):** Not Connected Internally. For pin compatibility with the LTC2208 this pin should be connected to GND or  $V_{DD}$  as required. Otherwise no connection.

**GND (Exposed Pad Pin 65):** ADC Power Ground. The exposed pad on the bottom of the package must be soldered to ground.

**BLOCK DIAGRAM**

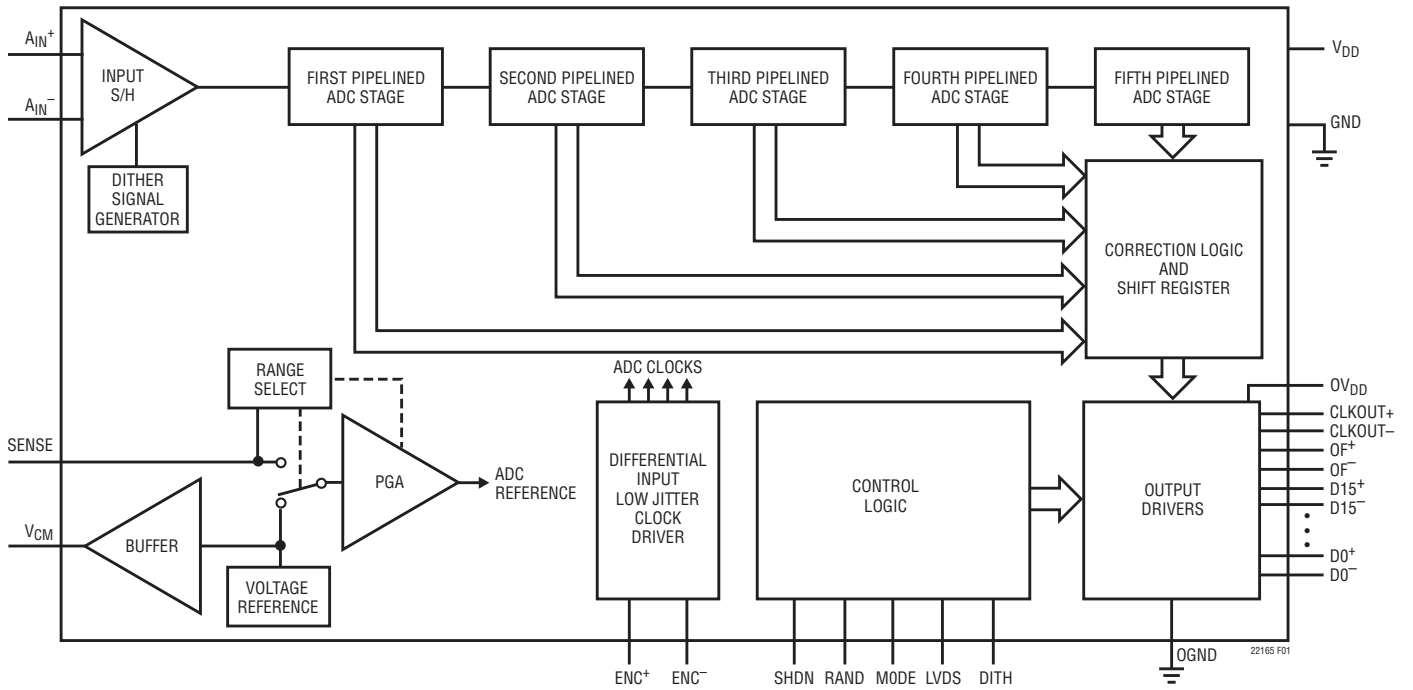


Figure 1. Functional Block Diagram

## OPERATION

### DYNAMIC PERFORMANCE

#### Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N+D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency (Nyquist Frequency).

#### Signal-to-Noise Ratio

The signal-to-noise (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components, except the first five harmonics.

#### Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency (Nyquist Frequency). THD is expressed as:

$$\text{THD} = -20\text{Log}\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_N^2}}{V_1}\right)$$

where  $V_1$  is the RMS amplitude of the fundamental frequency and  $V_2$  through  $V_N$  are the amplitudes of the second through  $n$ th harmonics.

#### Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies  $f_a$  and  $f_b$  are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of  $m f_a \pm n f_b$ , where  $m$  and  $n = 0, 1, 2, 3$ , etc. For example, the 3rd order IMD terms include  $(2f_a + f_b)$ ,  $(f_a + 2f_b)$ ,  $(2f_a - f_b)$  and  $(f_a - 2f_b)$ . The 3rd order IMD is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order IMD product.

#### Spurious Free Dynamic Range (SFDR)

The ratio of the RMS input signal amplitude to the RMS value of the peak spurious spectral component expressed in dBc. SFDR may also be calculated relative to full-scale and expressed in dBFS.

#### Full Power Bandwidth

The Full Power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB from a full-scale input signal.

#### Aperture Delay Time

The time from when a rising  $\text{ENC}^+$  equals the  $\text{ENC}^-$  voltage to the instant that the input signal is held by the sample-and-hold circuit.

#### Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal-to-noise ratio term due to the jitter alone will be:

$$\text{SNR}_{\text{JITTER}} = -20\text{log}(2\pi \cdot f_{\text{IN}} \cdot t_{\text{JITTER}})$$

This formula states SNR due to jitter *alone* at any amplitude in terms of dBc.

## APPLICATIONS INFORMATION

### CONVERTER OPERATION

The LTC2216/LTC2215 are CMOS pipelined multistep converters with a low noise front-end. As shown in Figure 1, these converters have five pipelined ADC stages; a sampled analog input will result in a digitized value seven cycles later (see the Timing Diagram section). The analog input is differential for improved common mode noise immunity and to maximize the input range. Additionally, the differential input drive will reduce even order harmonics of the sample and hold circuit. The encode input is also differential for improved common mode noise immunity.

The LTC2216/LTC2215 have two phases of operation, determined by the state of the differential ENC<sup>+</sup>/ENC<sup>-</sup> input pins. For brevity, the text will refer to ENC<sup>+</sup> greater than ENC<sup>-</sup> as ENC high and ENC<sup>+</sup> less than ENC<sup>-</sup> as ENC low.

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when odd stages are outputting their residue, the even stages are acquiring that residue and vice versa.

When ENC is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the “input S/H” shown in the block diagram. At the instant that ENC transitions from low to high, the voltage on the sample capacitors is held. While ENC is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H amplifier during the high phase of ENC. When ENC goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When ENC goes high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third and fourth stages, resulting in a fourth stage residue that is sent to the fifth stage for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results

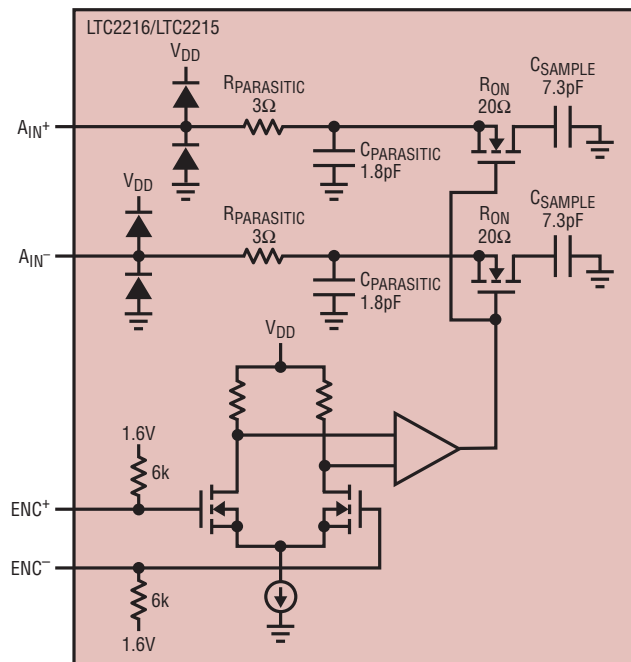
from all of the ADC stages are digitally delayed such that the results can be properly combined in the correction logic before being sent to the output buffer.

### SAMPLE/HOLD OPERATION AND INPUT DRIVE

#### Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC2216/LTC2215 CMOS differential sample and hold. The differential analog inputs are sampled directly onto sampling capacitors ( $C_{\text{SAMPLE}}$ ) through NMOS transistors. The capacitors shown attached to each input ( $C_{\text{PARASITIC}}$ ) are the summation of all other capacitance associated with each input.

During the sample phase when ENC is low, the NMOS transistors connect the analog inputs to the sampling capacitors and they charge to, and track the differential input voltage. When ENC transitions from low to high, the sampled input voltage is held on the sampling capacitors. During the hold phase when ENC is high, the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As ENC transitions for high to low, the inputs are reconnected to



22165 F02

Figure 2. Equivalent Input Circuit

22165f

## APPLICATIONS INFORMATION

the sampling capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time. If the change between the last sample and the new sample is small, the charging glitch seen at the input will be small. If the input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

### Common Mode Bias

The ADC sample-and-hold circuit requires differential drive to achieve specified performance. Each input should swing  $\pm 0.6875V$  for the 2.75V range, around a common mode voltage of 1.575V. The  $V_{CM}$  output pin (Pin 3) is designed to provide the common mode bias level.  $V_{CM}$  can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp differential driver circuit. The  $V_{CM}$  pin must be bypassed to ground close to the ADC with 2.2 $\mu F$  or greater.

### Input Drive Impedance

As with all high performance, high speed ADCs the dynamic performance of the LTC2216/LTC2215 can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and input reactance can influence SFDR. At the falling edge of ENC the sample and hold circuit will connect the sampling capacitor to the input pin and start the sampling period. The sampling period ends when ENC rises, holding the sampled input on the sampling capacitor. Ideally, the input circuitry should be fast enough to fully charge the sampling capacitor during the sampling period  $1/(2 \cdot f_{ENCODE})$ ; however, this is not always possible and the incomplete settling may degrade the SFDR. The sampling glitch has been designed to be as linear as possible to minimize the effects of incomplete settling.

For the best performance it is recommended to have a source impedance of 100 $\Omega$  or less for each input. The source impedance should be matched for the differential inputs. Poor matching will result in higher even order harmonics, especially the second.

## INPUT DRIVE CIRCUITS

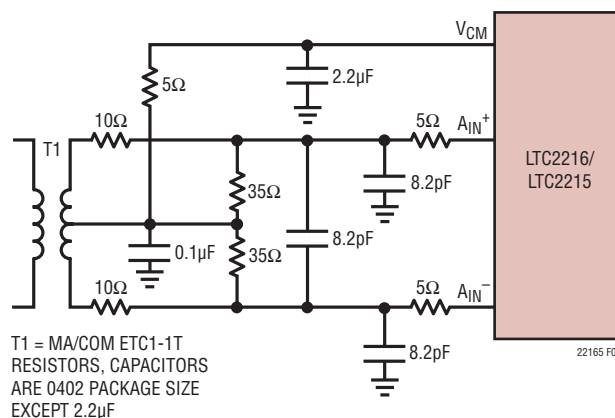
### Input Filtering

A first-order RC low-pass filter at the input of the ADC can serve two functions: limit the noise from input circuitry and provide isolation from ADC S/H switching. The LTC2216/LTC2215 have a very broadband S/H circuit, DC to 400MHz. This can be used in a wide range of applications, therefore, it is not possible to provide a single recommended RC filter.

Figures 3 and 4 show two examples of input RC filtering for two ranges of input frequencies. In general it is desirable to make the capacitors as large as can be tolerated—this will help suppress random noise as well as noise coupled from the digital circuitry. The LTC2216/LTC2215 do not require any input filter to achieve data sheet specifications; however, no filtering will put more stringent noise requirements on the input drive circuitry.

### Transformer Coupled Circuits

Figure 3 shows the LTC2216/LTC2215 being driven by an RF transformer with a center-tapped secondary. The secondary center tap is DC biased with  $V_{CM}$ , setting the ADC input signal at its optimum DC level. Figure 3 shows a 1:1 turns ratio transformer. Other turns ratios can be used; however, as the turns ratio increases so does the impedance seen by the ADC. Source impedance greater than 50 $\Omega$  can reduce the input bandwidth and increase



**Figure 3. Single-Ended to Differential Conversion Using a Transformer. Recommended for Input Frequencies from 5MHz to 100MHz**

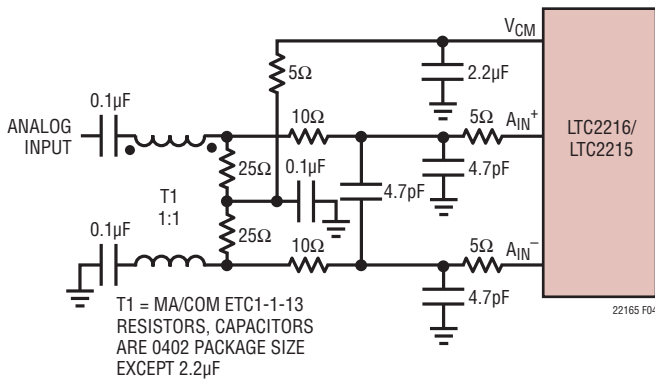


## APPLICATIONS INFORMATION

high frequency distortion. A disadvantage of using a transformer is the loss of low frequency response. Most small RF transformers have poor performance at frequencies below 1MHz.

Center-tapped transformers provide a convenient means of DC biasing the secondary; however, they often show poor balance at high input frequencies, resulting in large 2nd order harmonics.

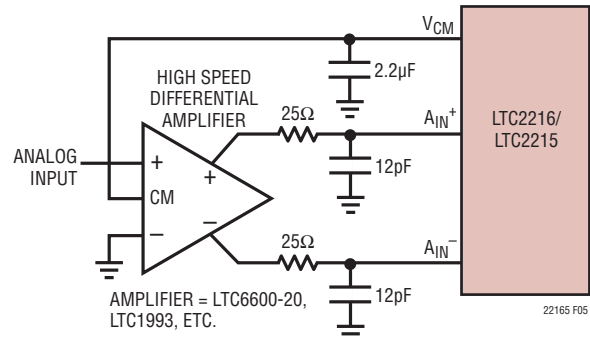
Figure 4 shows transformer coupling using a transmission line balun transformer. This type of transformer has much better high-frequency response and balance than flux coupled center-tap transformers. Coupling capacitors are added at the ground and input primary terminals to allow the secondary terminals to be biased at 1.575V.



**Figure 4. Using a Transmission Line Balun Transformer. Recommended for Input Frequencies from 100MHz to 250MHz**

### Direct Coupled Circuits

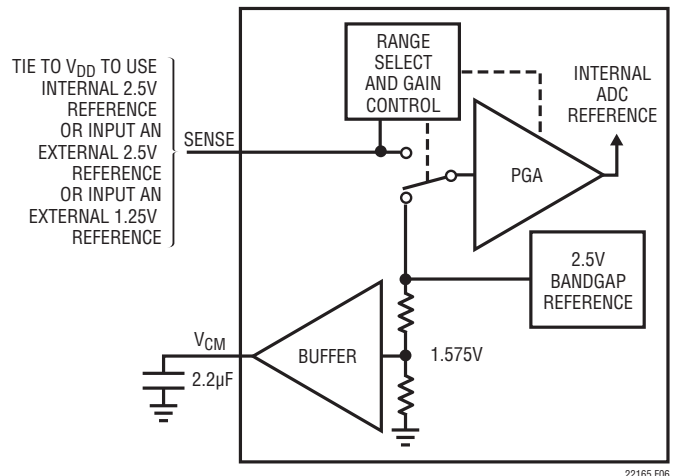
Figure 5 demonstrates the use of a differential amplifier to convert a single ended input signal into a differential input signal. The advantage of this method is that it provides low frequency input response; however, the limited gain bandwidth of any op amp or closed-loop amplifier will degrade the ADC SFDR at high input frequencies. Additionally, wideband op amps or differential amplifiers tend to have high noise. As a result, the SNR will be degraded unless the noise bandwidth is limited prior to the ADC input.



**Figure 5. DC Coupled Input with Differential Amplifier**

### Reference Operation

Figure 6 shows the LTC2216/LTC2215 reference circuitry consisting of a 2.5V bandgap reference, a programmable gain amplifier and control circuit. The LTC2216/LTC2215 has three modes of reference operation: Internal Reference, 1.25V external reference or 2.5V external reference. To use the internal reference, tie the SENSE pin to  $V_{DD}$ . To use an external reference, simply apply either a 1.25V or 2.5V reference voltage to the SENSE input pin. Both 1.25V and 2.5V applied to SENSE will result in a full-scale range of 2.75V<sub>P-P</sub>. A 1.575V output,  $V_{CM}$ , is provided for a common mode bias for input drive circuitry. An external bypass capacitor is required for the  $V_{CM}$  output. This provides a high frequency low impedance path to ground for internal and external circuitry. This is also the compensation capacitor for the reference; which will not be stable without this capacitor. The minimum value required for stability is 2.2µF.



**Figure 6. Reference Circuit**

## APPLICATIONS INFORMATION

The internal programmable gain amplifier provides the internal reference voltage for the ADC. This amplifier has very stringent settling requirements and therefore is not accessible for external use.

The SENSE pin can be driven  $\pm 5\%$  around the nominal 2.5V or 1.25V external reference inputs. This adjustment range can be used to trim the ADC gain error or other system gain errors. When selecting the internal reference, the SENSE pin should be tied to  $V_{DD}$  as close to the converter as possible. If the sense pin is driven externally it should be bypassed to ground as close to the device as possible with 1 $\mu$ F ceramic capacitor.

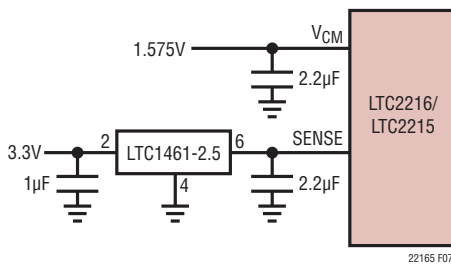


Figure 7. A 2.75V Range ADC with an External 2.5V Reference

### Driving the Encode Inputs

The noise performance of the LTC2216/LTC2215 can depend on the encode signal quality as much as on the analog input. The encode inputs are intended to be driven differentially, primarily for noise immunity from common mode noise sources. Each input is biased through a 6k resistor to a 1.6V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical (high input frequencies), take the following into consideration:

1. Differential drive should be used.
2. Use as large an amplitude possible. If using transformer coupling, use a higher turns ratio to increase the amplitude.

3. If the ADC is clocked with a fixed-frequency sinusoidal signal, filter the encode signal to reduce wideband noise.
4. Balance the capacitance and series resistance at both encode inputs such that any coupled noise will appear at both inputs as common mode noise.

The encode inputs have a common mode range of 1.2V to  $V_{DD}$ . Each input may be driven from ground to  $V_{DD}$  for single-ended drive.

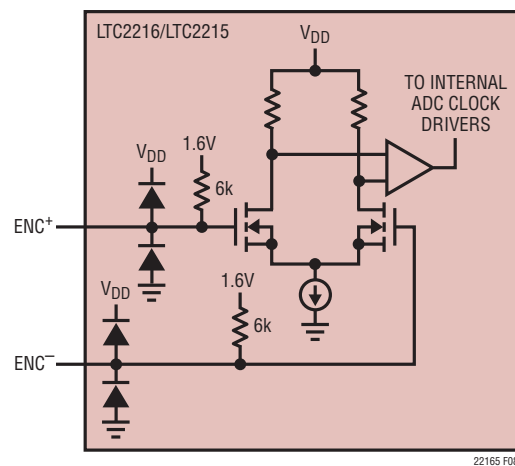
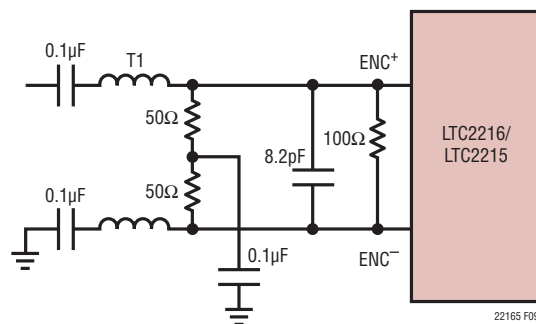


Figure 8. Equivalent Encode Input Circuit



T1 = MA/COM ETC1-1-13  
RESISTORS AND CAPACITORS  
ARE 0402 PACKAGE SIZE

Figure 9. Balun-Driven Encode