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LTC2207, LTC2207-14, LTC2206, LTC2206-14, LTC2205, LTC2205-14, LTC2204

DESCRIPTION

Demonstration circuit 918 supports members of a family of 16/14 BIT 130 MSPS ADCs. Each assembly features one of the following devices: LTC2207, LTC2207-14, LTC2206, LTC2206-14, LTC2205, LTC2205-14, or LTC2204 high speed, high dynamic range ADCs.

Other members of this family include the LTC2208 16-Bit 130Msps ADC with LVDS outputs, as well as the LTC2203 and LTC2202 which are 16-Bit 25Msps and 10Msps single-ended clock versions. These 7x7mm QFN devices are supported by Demonstration Circuit 919 (for single-ended clock input).

Several versions of the 918C demo board supporting the LTC2207 16-Bit and LTC2207-14 14-Bit series of A/D converters are listed in Table 1. Depending on the required resolution, sample rate and input frequency, the DC918 is supplied with the appropriate ADC and with an optimized input circuit. The circuitry on the analog inputs is optimized for analog input frequencies below 70MHz or from 70MHz to 140MHz. For higher input frequencies, contact the factory for support.

Design files for this circuit board are available. Call the LTC factory.

Table 1. DC918C Variants

DC918 VARIANTS	ADC PART NUMBER	RESOLUTION*	MAXIMUM SAMPLE RATE	INPUT FREQUENCY
918C-A	LTC2207	16-Bit	105Msps	1MHz - 70MHz
918C-B	LTC2207	16-Bit	105Msps	70MHz -140MHz
918C-C	LTC2206	16-Bit	80Msps	1MHz - 70MHz
918C-D	LTC2206	16-Bit	80Msps	70MHz -140MHz
918C-E	LTC2205	16-Bit	65Msps	1MHz - 70MHz
918C-F	LTC2205	16-Bit	65Msps	70MHz -140MHz
918C-G	LTC2204	16-Bit	40Msps	1MHz - 70MHz
918C-H	LTC2207-14	14-Bit	105Msps	1MHz - 70MHz
918C-I	LTC2207-14	14-Bit	105Msps	70MHz -140MHz
918C-J	LTC2206-14	14-Bit	80Msps	1MHz - 70MHz
918C-K	LTC2206-14	14-Bit	80Msps	70MHz -140MHz
918C-L	LTC2205-14	14-Bit	65Msps	1MHz - 70MHz

Table 2. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Supply Voltage	Depending on sampling rate and the A/D converter provided, this supply must provide up to 500mA.	Optimized for 3.3V [3.15V ⇔3.45V min/max]
Analog input range	Depending on PGA Pin Voltage	1.5V_{PP} to 2.25V_{PP}
Logic Input Voltages	Minimum Logic High	2.4V
	Maximum Logic Low	0.8V
Logic Output Voltage (74VCX245 output buffer, V_{cc} = 2.5V)	Minimum Logic High @ -1.6mA	2.3V (33Ω Series terminations)
	Maximum Logic Low @ 1.6mA	0.7V (33Ω Series terminations)
Sampling Frequency (Convert Clock Frequency)	See Table 1	
Convert Clock Level	50 Ω Source Impedance, AC coupled or ground referenced (Convert Clock input is capacitor coupled on board and terminated with 50Ω.)	2V_{P-P} ⇔2.5V_{P-P} Sine Wave or Square wave
Resolution	See Table 1	
Input frequency range	See Table 1	
SFDR	See Applicable Data Sheet	
SNR	See Applicable Data Sheet	

QUICK START PROCEDURE

Demonstration circuit 918 is easy to set up to evaluate the performance of the LTC2207/LTC2207-14, LTC2206/LTC2206-14, LTC2205/LTC2205-14, LTC2204 A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

SETUP

If a DC718 QuickDAACS Data Analysis and Collection System was supplied with the DC918 demonstration circuit, follow the DC718 Quick Start Guide to install the required software and for connecting the DC718 to the DC918 and to a PC running Windows98, 2000 or XP.

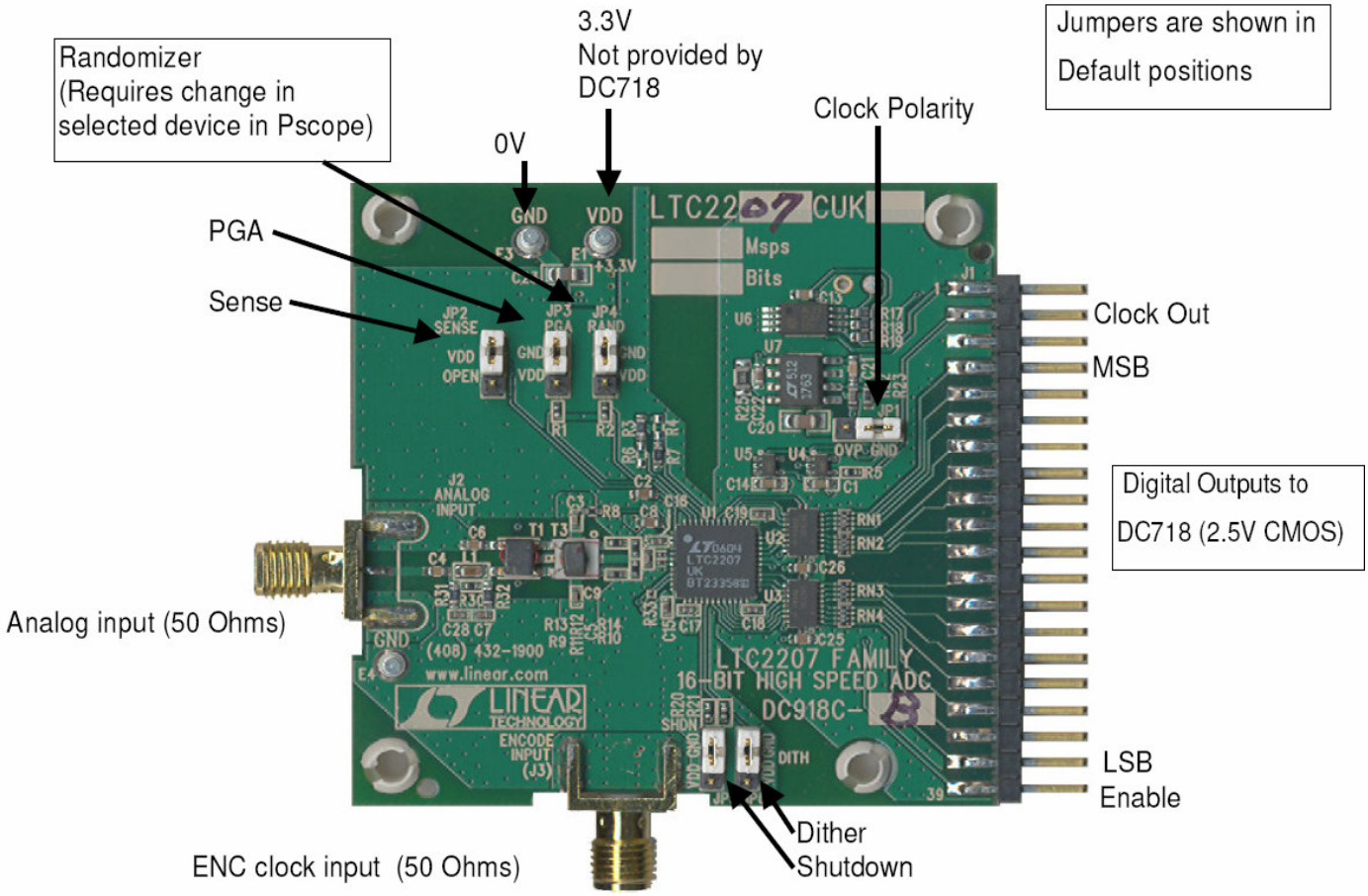


Figure 1. DC918 Setup (zoom for detail)

DC918DEMONSTRATION CIRCUIT BOARD JUMPERS

The DC918 demonstration circuit board should have the following jumper settings as default: (as per figure 1)

JP1: Output clock polarity: GND
JP2: SENSE: VDD, (Internal reference)
JP3: PGA: GND 2.25V range
JP4: RAND: GND Not randomized
JP5: SHDN: GND Not Shutdown
JP6: DITH: GND No internal dithering

APPLYING POWER AND SIGNALS TO THE DC918 DEMONSTRATION CIRCUIT

If a DC718 is used to acquire data from the DC918, the DC718 must FIRST be connected to a powered USB port or provided an external 6-9V BEFORE applying +3.3V across the pins marked "+3.3V" and "PWR GND" on the DC918. The DC918 demonstration circuit requires up to 500mA depending on the sampling rate and the A/D converter supplied.

The DC718 data collection board is powered by the USB cable and does not require an external power supply unless it must be connected to the PC through an un-powered hub in which case it must be supplied an external 6-9V on turrets G7(+) and G1(-) or the adjacent 2.1mm power jack.

ENCODE CLOCK

NOTE: This is not a logic compatible input. It is terminated with 50 Ohms. Apply an encode clock to the SMA connector on the DC918 demonstration circuit board marked "J3 ENCODE INPUT".

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter source. When using a sinusoidal generator, the amplitude should be large, up to $3V_{P-P}$ or 13dBm. Using band pass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. Datasheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broad band noise. Low phase noise Agilent 8644B generators are used with TTE band pass filters for both the Clock input and the Analog input.

Apply the analog input signal of interest to the SMA connectors on the DC918 demonstration circuit board marked "J2 ANALOG INPUT". These inputs are capacitive coupled to Balun transformers ETC1-1-13, or directly coupled through Flux coupled transformers ETC1-1T.

An internally generated conversion clock output is available on pin 3 of J1 and the data samples are available on Pins 7-37 for 16-Bits (or 7-33 for 14-Bits) of J1 which can be collected via a logic analyzer, cabled to a development system through a SHORT 2 to 4 inch long 40-pin ribbon cable or collected by the DC718 QuickEval-II Data Acquisition Board using the *PScope System Software* provided or down loaded from the Linear Technology website at http://www.linear.com/software/. If a DC718 was provided, follow the DC718 Quick Start Guide and the instructions below.

To start the data collection software if "*PScope.exe*", is installed (by default) in \Program Files\LTC\PScope\, double click the PScope Icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC918 demonstration circuit is properly connected to the DC718, PSCOPE should automatically detect the DC918, and configure itself accordingly. If necessary the procedure below explains how to manually configure PSCOPE.

Configure PScope for the appropriate variant of the DC918 demonstration circuit by selecting the correct A/D Converter as installed on the DC918. Under the "Configure" menu, go to "Device." Under the "Device" pull down menu, select device, either LTC2207, LTC2207-14, LTC2206, LTC2206-14, LTC2205, LTC2205-14, or LTC2204. Select the part in the Device List and PScope will automatically blank the last two LSBs when using a DC918 supplied with a 14-Bit part. You may also manually configure Pscope as follows:

User configure

16-Bit (or 14-Bit if using -14 versions)

Alignment: Left-16

Bipolar (2's complement)

Positive clock edge

Type: CMOS

If everything is hooked up properly, powered and a suitable convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for *PScope* is available in the DC718 Quick Start Guide and in the online help available within the *PScope* program itself.

ANALOG INPUT NETWORK

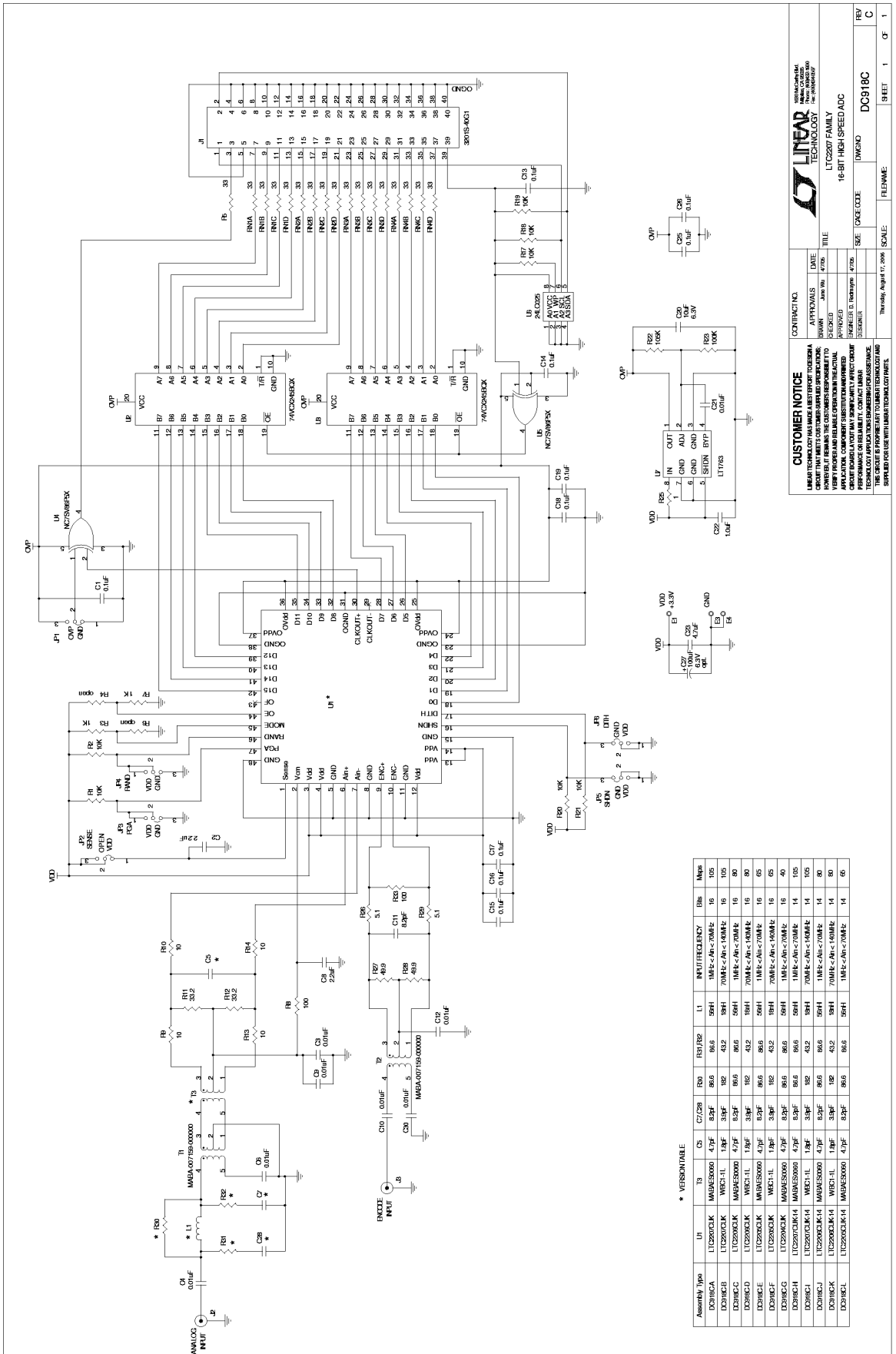
For optimal distortion and noise performance the RC network on the analog inputs should be optimized for different analog input frequencies. For input frequencies below 70MHz a capacitor with the value of 4.7pF should be used for C5. For input frequencies from 70MHz to 140MHz a capacitor with the value of 8.2pF should be used for C5. These two input networks cover a broad bandwidth and are not optimized for operation at a specific input frequency. For input frequencies less than 5MHz, or greater than 150MHz, other input networks may be more appropriate.

In almost all cases, filters will be required on both analog input and encode clock to provide data sheet SNR.

Narrow band high Q filters may produce poor results with preliminary silicon. 10% band-pass would be preferred over 5% band-pass on the analog input, although narrow band filters can be used on the clock input. The filters should be located close to the inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50 ohms outside the passband.

In some cases, 3-10dB pads may be required to obtain low distortion.

If your generator cannot deliver full-scale signals without distortion, you may benefit from a medium power amplifier based on a Gallium Arsenide Gain block prior to the final filter. This is particularly true at higher frequencies where IC based operational amplifiers may be unable to deliver the combination of low noise figure and High IP3 point required. A high order filter can be used prior to this final amplifier, and a relatively lower Q filter used between the amplifier and the demo circuit.



Assembly Typo	U1	T3	C5	C7/C28	R30	R31/R32	L1	INPUT FREQUENCY	Bits	Msps
DC918CA	LTC2207/CLK	MABAES0060	4.7pF	8.2pF	86.6	86.6	56nH	1MHz<Ain<70MHz	16	105
DC918CB	LTC2206/CLK	WBC1-1L	1.8pF	3.9pF	182	43.2	18nH	70MHz<Ain<140MHz	16	105
DC918CC	LTC2208/CLK	MABAES0060	4.7pF	8.2pF	86.6	86.6	56nH	1MHz<Ain<70MHz	16	80
DC918CD	LTC2208/CLK	WBC1-1L	1.8pF	3.9pF	182	43.2	18nH	70MHz<Ain<140MHz	16	80
DC918CE	LTC2206/CLK	MABAES0060	4.7pF	8.2pF	86.6	86.6	56nH	1MHz<Ain<70MHz	16	65
DC918CF	LTC2206/CLK	WBC1-1L	1.8pF	3.9pF	182	43.2	18nH	70MHz<Ain<140MHz	16	65
DC918CG	LTC2204/CLK	MABAES0060	4.7pF	8.2pF	86.6	86.6	56nH	1MHz<Ain<70MHz	16	40
DC918CH	LTC2207/CLK14	MABAES0060	4.7pF	8.2pF	86.6	86.6	56nH	1MHz<Ain<70MHz	14	105
DC918CI	LTC2207/CLK14	WBC1-1L	1.8pF	3.9pF	182	43.2	18nH	70MHz<Ain<140MHz	14	105
DC918CJ	LTC2206/CLK14	MABAES0060	4.7pF	8.2pF	86.6	86.6	56nH	1MHz<Ain<70MHz	14	80
DC918CK	LTC2206/CLK14	WBC1-1L	1.8pF	3.9pF	182	43.2	18nH	70MHz<Ain<140MHz	14	80
DC918CL	LTC2205/CLK14	MABAES0060	4.7pF	8.2pF	86.6	86.6	56nH	1MHz<Ain<70MHz	14	65

★ VERSION TABLE