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diVa

# ARM Cortex-A8 CPU Module Family

## *LITE Line*

# HARDWARE MANUAL

DAVE Embedded Systems www.dave.eu info@dave.eu

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# Table of Contents

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# Illustration Index

# 1 Preface

## 1.1 About this manual

This Hardware Manual describes the DIVA CPU module series, their design and functions.

Precise specifications for the Texas Instruments AM335x processors can be found in the CPU datasheets and/or reference manuals.

## 1.2 Copyrights/Trademarks

Ethernet® is a registered trademark of XEROX Corporation.

All other products and trademarks mentioned in this manual are property of their respective owners.



## 1.3 Standards

**DAVE Embedded Systems** is certified to ISO 9001 standards.

## 1.4 Disclaimers

**DAVE Embedded Systems** does not assume any responsibility for availability, supply and support related to all products mentioned in this manual that are not strictly part of the DIVA CPU module.

DIVA CPU Modules are not designed for use in life support appliances, devices, or systems where malfunctioning of these products can reasonably be expected to result in personal injury. **DAVE Embedded Systems** customers who are using or selling these products for use in such applications do so at their own risk and agree to fully indemnify **DAVE Embedded Systems** for any damage resulting from such improper use or sale.

## 1.5 Warranty

DIVA is guaranteed against defects in material and workmanship for the warranty period from the shipment date. During the warranty period, **DAVE Embedded Systems** will at its discretion decide to repair or replace defective products. Within the warranty period, the repair of products is free of charge provided that warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the customer, unauthorized modification or misuse, operation outside of the product's specifications or improper installation or maintenance.

**DAVE Embedded Systems** will not be responsible for any defects or damages to other products not supplied by **DAVE Embedded Systems** that are caused by a faulty DIVA module.

## 1.6 Technical Support

We are committed to making our products easy to use and will help customers use our CPU modules in their systems.

Technical support is delivered through email for registered kits owners. Support requests can be sent to support-diva@dave.eu. Software upgrades are available for download in the restricted download area of **DAVE Embedded Systems** web site: http://www.dave.eu/reserved-area. An account is required to access this area.

Please refer to our Web site at http://www.dave.eu/dave-cpu-module-am335x-diva.html for the latest product documents, utilities, drivers, Product Change Notices, Board Support Packages, Application Notes, mechanical drawings and additional tools and software.

## 1.7 Related documents

| Document | Location |
|---|---|
| **DAVE Embedded Systems** Developers Wiki | http://wiki.dave.eu/index.php/Main_Page |
| AM335x Technical Reference Manual | http://www.ti.com/lit/ug/spruh73h/spruh73h.pdf |
| AM335x Portal (on TI Embedded Processors Wiki ) | http://processors.wiki.ti.com/index.php/Sitara_AM335x_Portal |
| Integration guide (on **DAVE Embedded Systems** Developers Wiki) | http://wiki.dave.eu/index.php/Integration_guide_%28Diva%29 |

**Tab. 1**: Related documents

## 1.8 Conventions, Abbreviations, Acronyms

| Abbreviation | Definition |
|---|---|
| BTN | Button |
| DIVELK | DIVA Embedded Linux Kit |
| EMAC | Ethernet Media Access Controller |
| GPI | General purpose input |
| GPIO | General purpose input and output |
| GPO | General purpose output |
| PCB | Printed circuit board |
| PMIC | Power Management Integrated Circuit |
| PRU | Programmable Real-Time Unit |
| PSU | Power supply unit |

| Abbreviation | Definition |
|---|---|
| RTC | Real time clock |
| SOC | System-on-chip |
| SO-DIMM | Small Outline Dual In-line Memory Module |
| SOM | System-on-module |
| WDT | Watchdog |
| | |
| | |
| | |
| | |

**Tab. 2**: Abbreviations and acronyms used in this manual

## Revision History

| *Version* | *Date* | *Notes* |
|---|---|---|
| 0.9.0 | October 2012 | First Draft |
| 1.0.0 | June 2013 | First official release |
| 1.0.1 | September 2013 | Minor fixes |
| 1.0.2 | October 2013 | Fixed RTC_PWRONRSTn direction<br>VAUX33 added to pinout table<br>Fixed PMIC_VBACKUP information<br>Fixed section 8.1 and 8.2 tables<br>Added I2C pull-up/pull-down information<br>Minor fixes |
| 1.0.3 | April 2014 | Minor fixes |
| 1.0.4 | August 2014 | Updated block diagram<br>Fixed PGOOD (VAUX33) description<br>Minor fixes |
| 1.0.5 | October 2013 | Pinout table fixes<br>Minor fixes |
| 1.0.6 | June 2015 | Minor Fixes<br>Updated mechanical drawings |

# 2 Introduction

DIVA is a family of system-on-modules (SOM) that belongs to **DAVE Embedded Systems LITE Line** product class. DIVA is based on Texas Instruments "Sitara" AM335x Cortex-A8 application processor and is built with SO-DIMM 204 pin form factor.

**Fig. 1**: DIVA CPU module

DIVA offers lots of graphics, processing, peripherals and industrial interface options, allowing customers to implement cost-effective design. The Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS) adds further flexibility and enables additional peripheral interfaces and real-time protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink.

Typical applications for DIVA are:

- Industrial sensors and I/O units
- Industrial drives with integrated communications and multi-axis motor control
- Programmable logic/automation controllers (PLC/PAC) with integrated industrial communications such as PROFIBUS, CAN and Ethernet
- Home and Building Automation

**Fig. 2**: DIVA plugged on DIVAEVB-Lite

## 2.1 Product Highlights

- ARM Cortex-A8 architecture @ 275/500/600/720 MHz
  - LITE Line
  - "No-frills" CPU module
  - SO-DIMM connector
  - Great cost-efficiency
- Extended power supply range [3.6 - 5.5]V, power regulation on board
- Coprocessing modules
  - NEON
  - PowerVR SGX
  - Crypto accelerator
- Industrial specification compliance
  - Extended temperature range (-40°C/+85°C)
  - Industrial-oriented interfaces set
- Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS)
  - Supports protocols such as EtherCAT, PROFIBUS, PROFINET, EtherNet/IP™, and more
  - Peripherals Inside the PRU-ICSS: UART port with flow control pins, MII Ethernet ports, MDIO port, ...

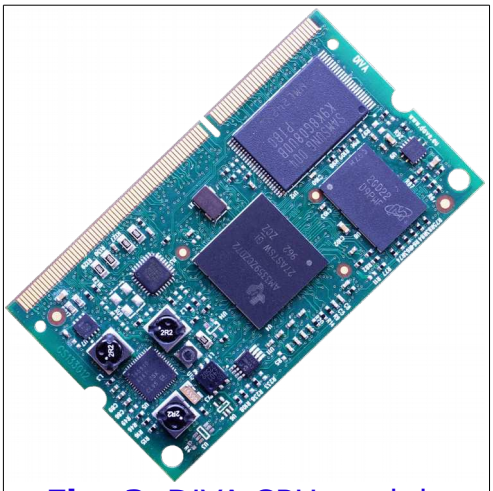
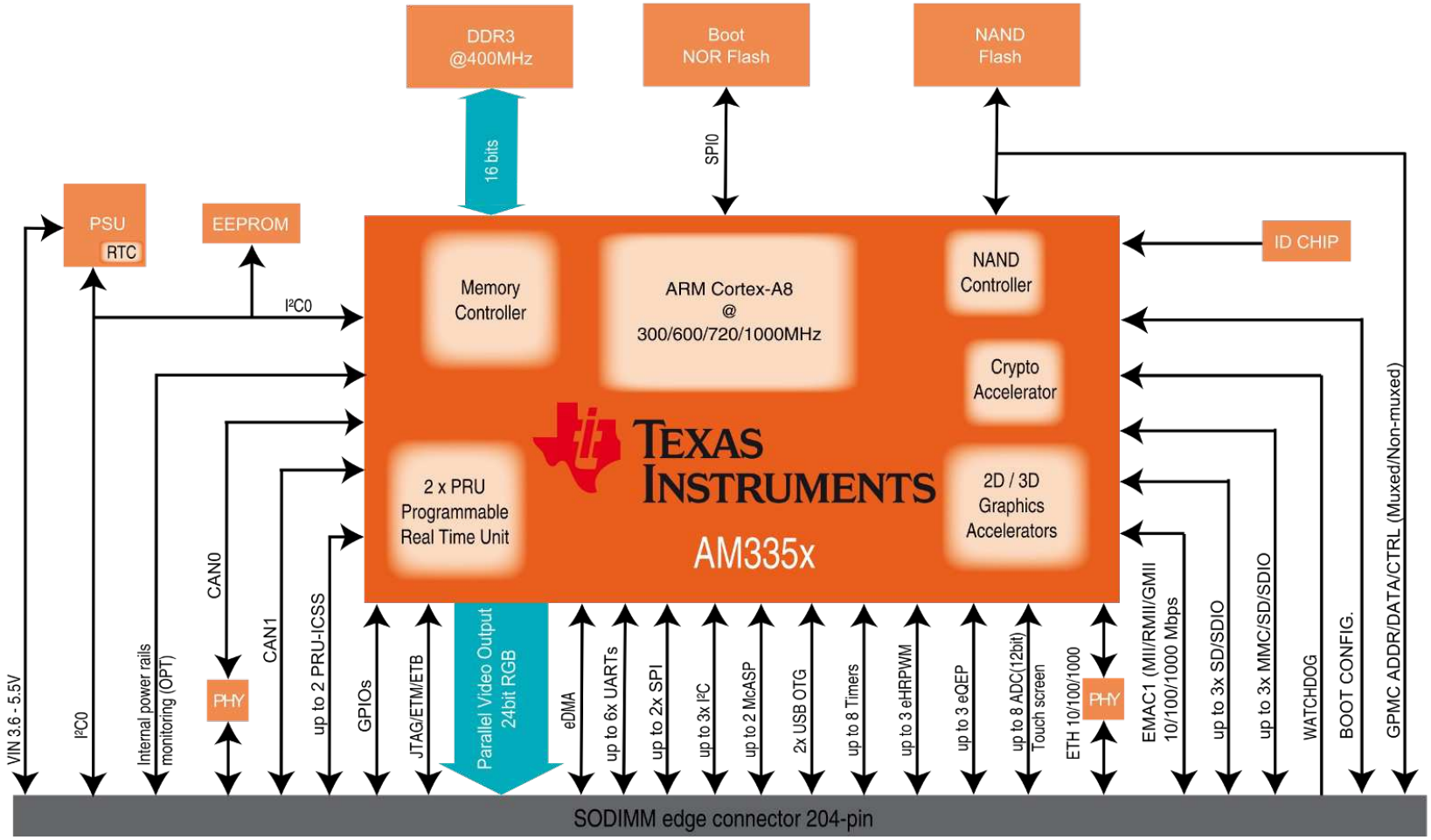


**Fig. 3**: DIVA CPU module

## 2.2 Block Diagram



## 2.3 Feature Summary

| Feature | Specifications | Options |
|---|---|---|
| CPU | "Sitara" AM335x<br>ARMv7 architecture<br>Cortex A8 @ 300/600/800/1000 | |
| RAM | 16-bit DDR3 @ 333 MHz<br>Up to 512 MB | |
| Storage | Flash NOR SPI<br>Flash NAND on Local bus<br>I²C 32 kbit EEPROM | |

**Tab. 3**: CPU, Memories, Busses

| Feature | Specifications | Options |
|---|---|---|
| Graphics Controller | Up to 24-Bits Data Output<br>Resolution Up to 2048x2048 (With Maximum 126-MHz Pixel Clock)<br>TFT/RGB support | |
| 2D/3D Engines | NEON Multimedia SIMD coprocessor<br>PowerVR SGX 530 3D Accelerator | |
| Coprocessors | Crypto Hardware Accelerator (AES, SHA, PKA, RNG)<br>Up to 2x Programmable Realtime Units (PRUs) | |
| USB | Up to 2x 2.0 OTG ports | |
| UARTs | Up to 6x UART ports | |
| GPIO | Up to 118 lines, shared with other functions (interrupts available) | |
| Input interfaces | Integrated 4/5/8-wire resistive touch screen controller | |
| Networking | Fast Ethernet with PHY<br>Additional MII/RMII/RGMII interface | |
| CAN | Dual CAN controller (version 2 part A, B) | |
| SD/MMC | Up to 3x MMC/SD/SDIO Serial interfaces (up to 48 MHz) | |
| Serial busses | Up to 3x I²C channels<br>Up to 2x SPI channels | |
| Audio | Up to 2x McASP interface | |
| Timers/PWM | Up to 4 programmable general purpose | |

| Feature | Specifications | Options |
|---|---|---|
| | timers (PWM function available)<br>PWMSS (Pulse width modulation subsystem) with 3x eHRPWM, 3x eCap, 3x eQEP | |
| RTC | On board, external battery powered | |
| Debug | JTAG IEEE 1149.1 Test Access Port<br>ETM Port<br>ETB Port | |
| Miscellaneous | Up to 8x 12-bit ADC channels | |

**Tab. 4**: Peripherals

| Feature | Specifications | Options |
|---|---|---|
| Supply Voltage | [3.6 - 5.5] V, voltage regulation on board | |
| Active power consumption | Please refer to Power consumption section | |
| Dimensions | 67.5 mm x 38.3 mm | |
| Weight | <tbd> | |
| MTBF | <tbd> | |
| Operation temperature | 0..70 °C<br>-40..+85 °C | |
| Shock | <tbd> | |
| Vibration | <tbd> | |
| Connectors | 204-pin SO-DIMM | |
| Connectors insertion/removal | <tbd> | |

**Tab. 5**: Electrical, Mechanical and Environmental Specifications

# 3 Design overview

The heart of DIVA module is composed by the following components:

- Texas Instruments AM335x processor
- Power supply unit
- DDR2 memory bank
- NOR and NAND flash banks
- 204 pin SO-DIMM connector with interfaces signals

This chapter shortly describes the main DIVA components.

## 3.1 “Sitara” AM335x CPU

Sitara™ ARM Cortex-A8 microprocessors (MPUs) are designed to optimize performance and peripheral support for customers in a variety of markets. AM335x Sitara™ are highly-integrated, scalable and programmable CPU families from Texas Instruments and are enhanced with image, graphics processing, peripherals and industrial interface options such as EtherCAT and PROFIBUS. The following subsystems are part of the processor:

- Microprocessor unit (MPU) subsystem based on the ARM® Cortex™-A8 architecture:
  - ARM Cortex-A8 RISC processor, with Neon™ Floating-Point Unit, 32KB L1 Instruction Cache, 32KB L1 Data Cache and 256KB L2 Cache
  - VFP coprocessor
- Debug subsystem (JTAG, CoreSight Embedded Trace Macrocell (ETM))
- General-Purpose Memory Controller (GPMC)
- PowerVR SGX 530 subsystem for vector/3D graphics acceleration to support display and gaming effects
- LCD and Touchscreen Controller

- Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS)
- Integrated peripherals (USBs, EMACs, UARTs, ...)

The following table shows a **comparison** between the devices, highlighting the differences:

| Processor | PowerVR SGX 3D | PRU-ICSS | Ethercat | Crypto | Clock speed (MHz) |
|---|---|---|---|---|---|
| AM3359 | YES | YES | YES | YES | 800 |
| AM3358 | YES | YES | N.A. | YES | 600<br>800<br>1000 |
| AM3357 | N.A. | YES | YES | YES | 300<br>600<br>800 |
| AM3356 | N.A. | YES | N.A. | YES | 300<br>600<br>800 |
| AM3354 | YES | N.A. | N.A. | YES | 600<br>800<br>1000 |
| AM3352 | N.A. | N.A. | N.A. | YES | 300<br>600<br>800<br>1000 |

**Tab. 6**: AM335x part number comparison

## 3.2 DDR3 memory bank

DDR3 SDRAM memory bank is composed of a 16-bit width chip. The following table reports the SDRAM specifications:

| | |
|---|---|
| **CPU connection** | SDRAM bus |
| **Size min** | 64 MB |
| **Size max** | 512 MB |
| **Width** | 16 bit |
| **Speed** | 333 MHz |

**Tab. 7**: DDR3 specifications

## 3.3 NOR flash bank

NOR flash is a Serial Peripheral Interface (SPI) device. This feature is optional and, when populated, the device is connected to AM335X_SPI0 and can act as boot memory. The chip select is AM335X_SPI0_CS0.

The following table reports the NOR flash specifications:

| | |
|---|---|
| **CPU connection** | AM335X_SPI0 (CS0n) |
| **Size min** | 4 MByte |
| **Size max** | 128 MByte |
| **Bootable** | Yes |

**Tab. 8**: NOR flash specifications

## 3.4 NAND flash bank

On board main storage memory is a 8-bit wide NAND flash. This feature is optional and, when populated, the device is connected to the GPMC bus. The chip select is AM335X_GPMC_CS0n.

The following table reports the NAND flash specifications:

| | |
|---|---|
| **CPU connection** | GPMC bus (CS0n) |
| **Page size** | 512 byte, 2 kbyte or 4 kbyte |
| **Size min** | 32 MByte |
| **Size max** | 2 GByte |
| **Width** | 8 bit |
| **Bootable** | Yes |

**Tab. 9**: NAND flash specifications

## 3.5 Memory Map

This section will be completed in a future version of this manual.

## 3.6 Power supply unit

DIVA, as the other LITE Line CPU modules, embeds all the

elements required for powering the unit, therefore power sequencing is self-contained and simplified. Nevertheless, power must be provided from carrier board, and therefore users should be aware of the ranges power supply can assume as well as all other parameters. For detailed information, please refer to Section 5.1.

## 3.7 CPU module connectors

All interface signals provided by DIVA are routed through a 204 pin SO-DIMM connector. The host board must mount the mating connector and connect the desired peripheral interfaces according to DIVA pinout specifications.

For mechanical information, please refer to Section 4 (Mechanical specifications). For pinout and peripherals information, please refer to Sections 6 (Pinout table) and 7 (Peripheral interfaces).

# 4 Mechanical specifications

This chapter describes the mechanical characteristics of the DIVA module.

*Mechanical drawings are available in DXF format from the DIVA page on DAVE Embedded Systems website http://http//www.dave.eu/dave-cpu-module-am335x-diva.html*

## 4.1 Board Layout

The following figure shows the physical dimensions of the DIVA module:

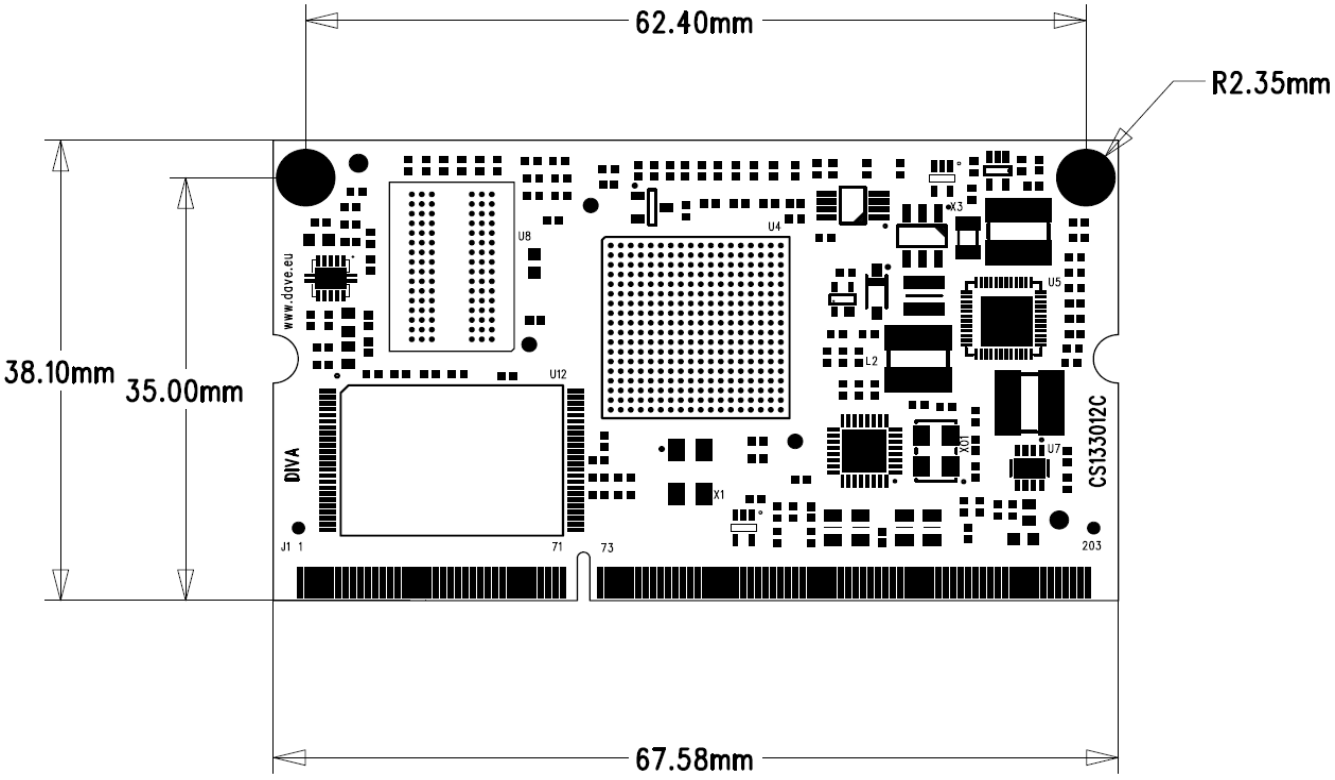



**Fig. 4**: Board layout - top view

- Board height: 38.3 mm

- Board width: 67.6 mm
- Height of all components is < 2.8 mm.
- PCB thickness is 1 mm.

The following figure highlights the maximum components' heights on DIVA module:

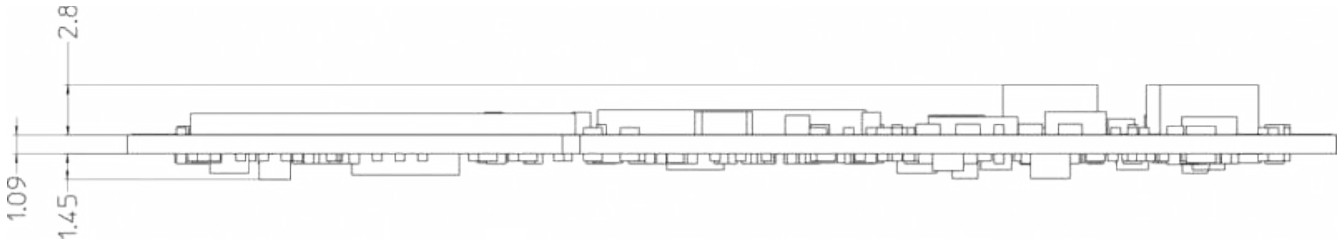



**Fig. 5**: DIVA module - Side view

## 4.2 Connectors

The following figure shows the DIVA SODIMM connector layout:

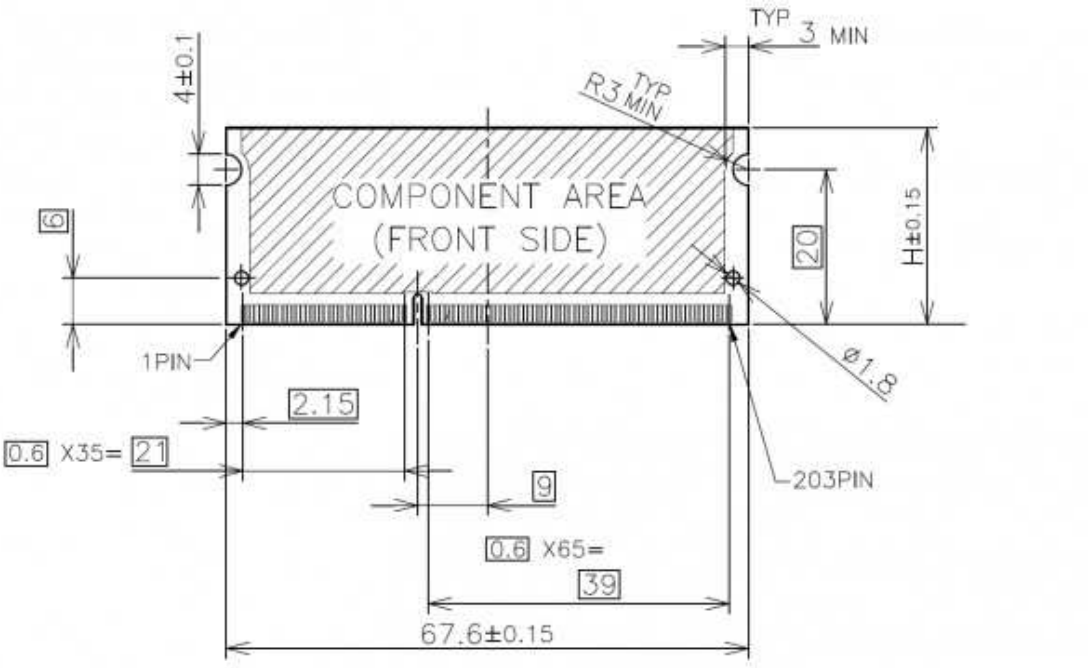



**Fig. 6**: Connectors layout

The following table reports the connectors specifications:

| | |
|---|---|
| **Part number** | Standard SO-DIMM 204-pin (DDR3) |
| **Mating connectors** | DDR3 SO-DIMM SOCKET<br>Part number : TE Connectivity 2013289-1 (used on DIVAEVB-Lite) |

# 5 Power, reset and control

## 5.1 Power Supply Unit (PSU) and recommended power-up sequence

Implementing correct power-up sequence for AM335x processors family is not a trivial task because several power rails are involved. DIVA SOM simplifies this task and embeds all the needed circuitry. The following picture shows a

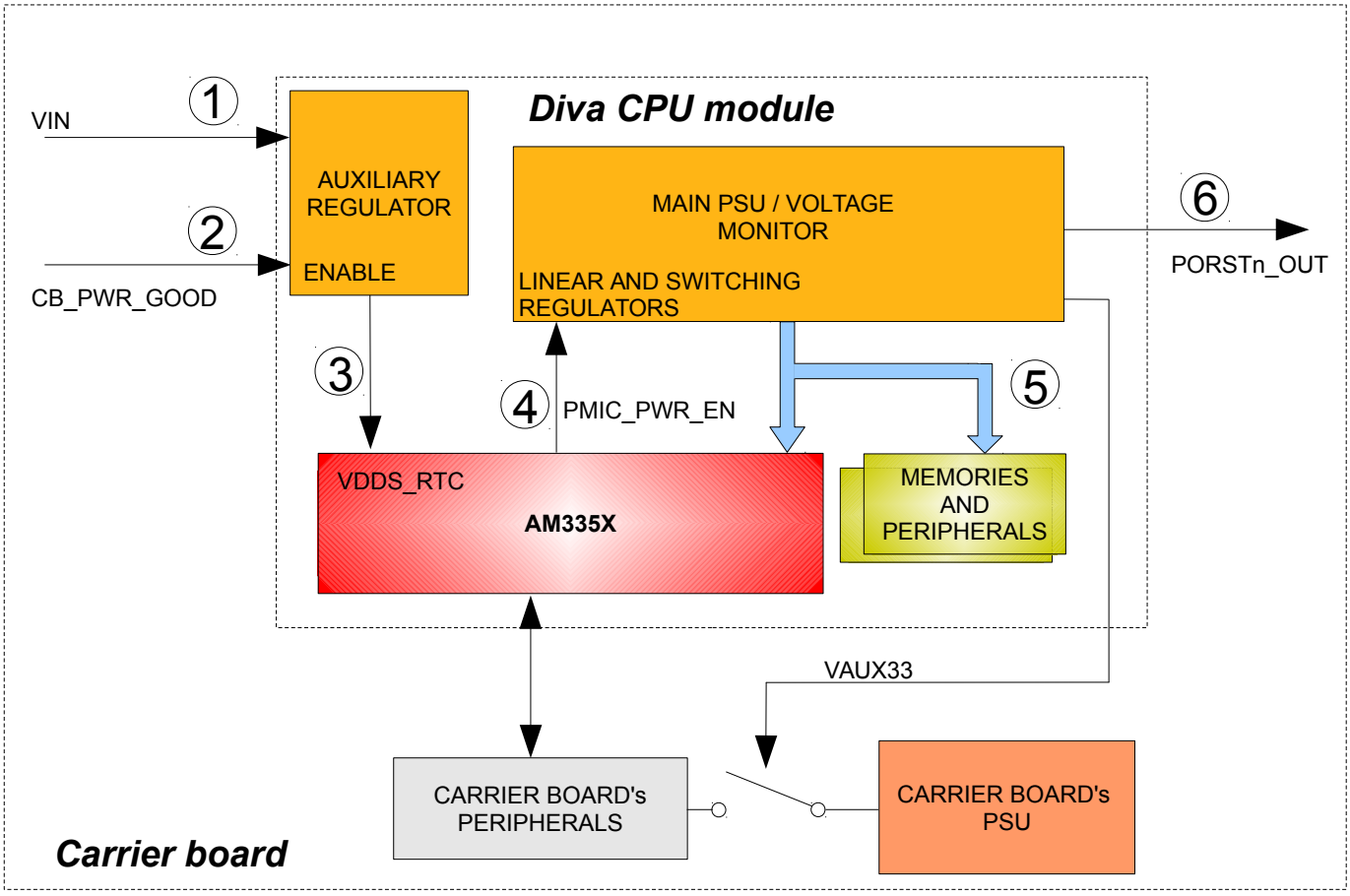



**Fig. 7**: DIVA power-up sequence

simplified block diagram of PSU/voltage monitoring circuitry:

The recommended power-up sequence is:

1. main power supply rail (VIN) ramps up
2. carrier board circuitry raises CB_PWR_GOOD; this indicates VIN rail is stable ([1])
3. auxiliary regulator is enabled, thus processor's VDDS_RTC domain is powered
4. processor raises PMIC_PWR_EN signal to start main PSU
5. this step is composed of two events:
   - main PSU enables several voltage rails to complete CPU, memories and peripheral power up sequence
   - VAUX33 signal is raised; this active-high signal indicates that SoM's I/O is powered. This signal can be used to manage carrier board power up sequence in order to prevent back powering (from SoM to carrier board or vice versa)
6. PORSTn_OUT signal is raised to indicate that all power rails of SOM are stable

## 5.2 PMIC

Main PSU subsystem of DIVA SOM is based on Power Management Integrated Circuit (PMIC) Texas Instruments TPS65910A3A1. PMIC controls processor's power up sequence and sources the majority of power rails needed by AM335x.

Once processors is booted, it can control PMIC via the I2C0 bus to:

- set all the voltage needed by CPU in all operating conditions
- set RTC and control it
- manage power modes.

Besides I2C bus, PMIC has several control signals including:

- PWRHOLD (input): This signal is connected to

1 This step is not mandatory and VIN and CB_PWR_GOOD can be connected together. CB_PWR_GOOD is provided to prevent, if necessary, DIVA's PSU to turn on during ramp of carrier board VIN rail.

processor's PMIC_PWR_EN and is used to initiate power up sequence.

- PMIC_PWRON (input): A rising edge of this pin (automatically done at startup) the PMIC performs an OFF-to-ACTIVE state transition. On a falling edge of this pin, the PMIC performs an ACTIVE-to-OFF state transition. This signal is pulled-up to VIN through 10kOhm resistor.

## 5.3 Reset scheme and voltage monitoring

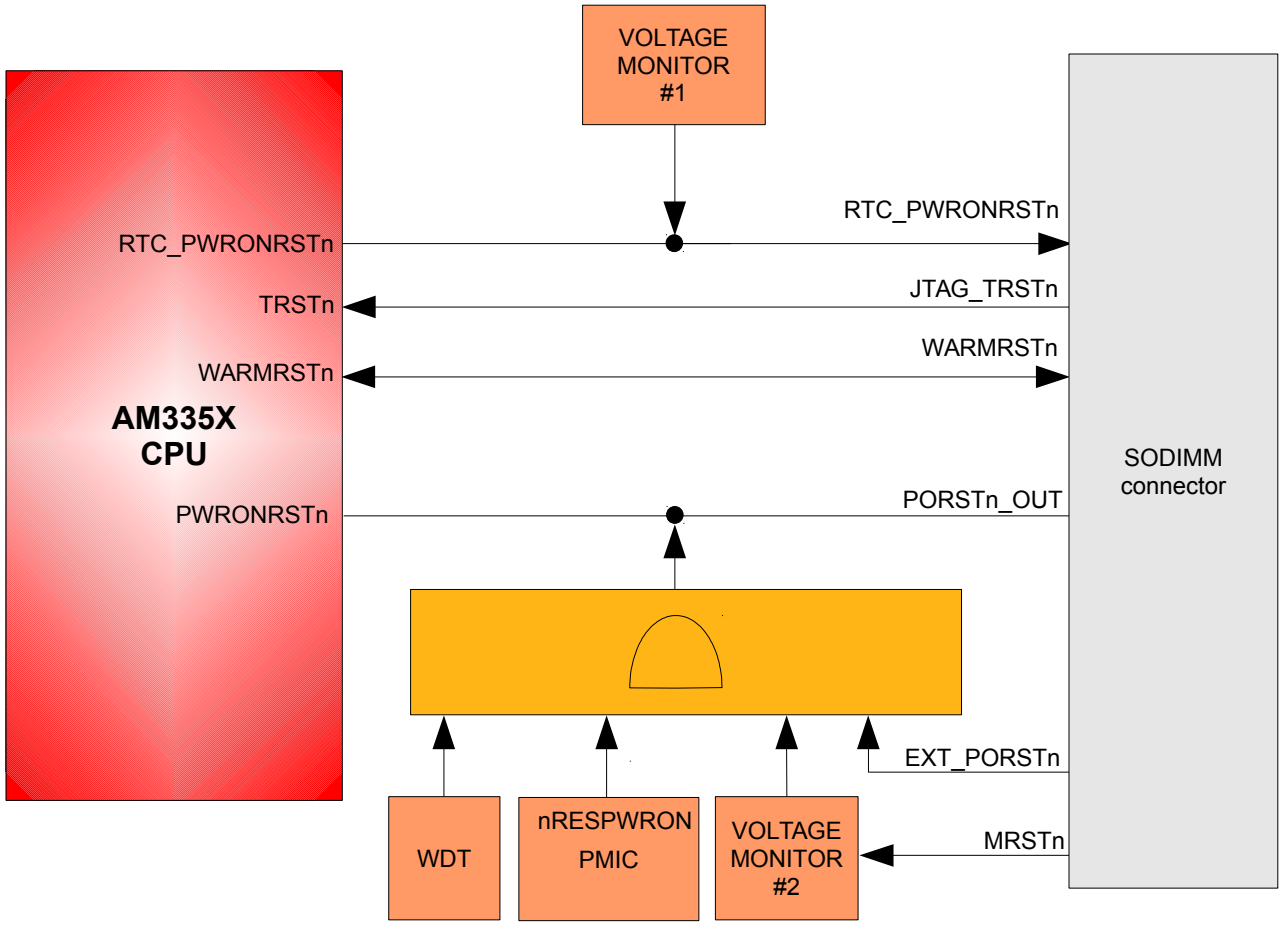



**Fig. 8**: DIVA Reset scheme

DIVA implements a flexible reset scheme that offers several different solutions for system integrators at carrier board level. The following picture shows a diagram of the reset scheme: