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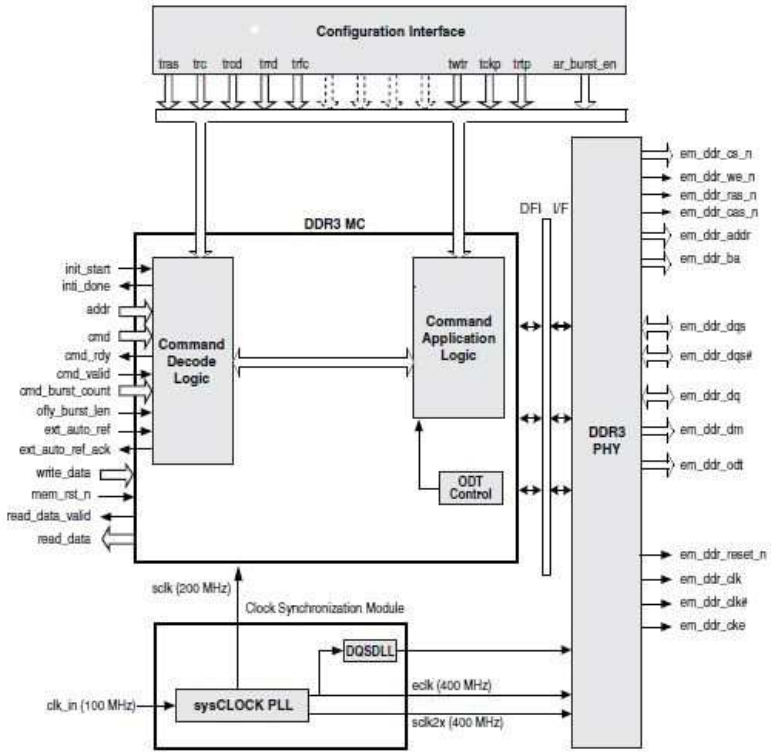
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

DDR3 SDRAM Controller

Overview

The Lattice Double Data Rate (DDR3) Synchronous Dynamic Random Access Memory (SDRAM) Controller is a general-purpose memory controller that interfaces with industry standard DDR3 memory devices/modules compliant with JESD79-3, DDR3 SDRAM Standard, and provides a generic command interface to user applications. The DDR3 SDRAM is the next-generation DDR SDRAM memory technology which features faster speed, mitigated SSO, and reduced routing due to "fly-by" routing signals to SDRAM instead of low skew tree distribution. This core reduces the effort required to integrate the DDR3 memory controller with the remainder of the application and minimizes the need to directly deal with the DDR3 memory interface.



Features

- Support for all LatticeECP3 "EA" devices
- Interfaces to Industry Standard DDR3 SDRAM components and modules compliant with JESD79-3, DDR3 SDRAM Standard
- Interfaces to DDR3 SDRAM at speeds up to 400 MHz / 800 Mbps in -8 speed grade devices
- Supports memory data path widths of -8, -16, -24, -32, -40, -48, -56, -64 and -72 bits
- Supports x4, x8, and x16 device configurations
- Support for unbuffered DDR3 DIMM and DDR3 RDIMM module
- Supports up to one DIMM and two ranks per DIMM
- Programmable burst lengths of 8 (fixed), chopped 4 or 8 (on-the-fly), or chopped 4 (fixed)
- Programmable CAS latency
- Programmable CAS Write Latency
- Read burst type of nibble sequential or interleave
- Supports automatic DDR3 SDRAM initialization and refresh
- Automatic Write Leveling for each DQS for DIMM applications. Option to switch of write leveling for On-board memory applications.
- Supports Power Down Mode
- Supports Dynamic On-Die Termination (ODT) controls
- Termination Data Strobe (TDQS) for x8 widths only
- LatticeECP3 I/O primitives manage read skews (Read Leveling equivalent)
- Automatic Programmable Interval Refresh or User Initiated Refresh
- Option for controlling memory reset outside the controller

The DDR3 SDRAM Controller is available as an IPexpress user configurable IP core, which allows the configuration of the IP and generation of a netlist and simulation file for use in designs. Please note that generating a bitstream may be prevented or the bitstream may have time logic present unless a license for the IP is purchased.

Performance and Resource Utilization

LatticeECP3[1, 2]

Parameters	SLICEs	LUTs	Registers	I/O	f_{MAX} (MHz)
Data Bus Width: 8 (x8)	1741	2526	1772	42	400 MHz (800 Mbps)
Data Bus Width: 16 (x8)	1924	2672	2096	53	400 MHz (800 Mbps)
Data Bus Width: 24 (x8)	2108	2800	2439	64	400 MHz (800 Mbps)
Data Bus Width: 32 (x8)	2303	2913	2789	75	400 MHz (800 Mbps)
Data Bus Width: 40 (x8)	2298	2966	2692	86	400 MHz (800 Mbps)
Data Bus Width: 48 (x8)	2438	3055	2909	97	400 MHz (800 Mbps)
Data Bus Width: 56 (x8)	2553	3114	3123	108	400 MHz (800 Mbps)
Data Bus Width: 64 (x8)	2683	3224	3329	119	400 MHz (800 Mbps)
Data Bus Width: 72 (x8)	2820	3399	3477	130	333 MHz (666 Mbps)

1. Performance and utilization data are generated targeting an LFE3-150EA-8FN1156C device using Lattice Diamond 1.2 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.
2. EA silicon support only.
3. The DDR3 IP core can operate at 400 MHz (800 DDR3) in the fastest speed-grade (-8) when the data width is 64 bits or less and one chip select is used.
4. I/O count includes only the primary I/O (memory side I/O).

Ordering Information

Family	Part Number
LatticeECP3 (EA)	DDR3-P-E3-U1

IP Version: 1.3
Evaluate: To download a full evaluation version of this IP, go to the IPexpress tool and click the IP Server button in the toolbar. All LatticeCORE IP cores and modules available for download will be visible. For more information on viewing/downloading IP please read the **IP Express Quick Start Guide**.
Purchase: To find out how to purchase the IP Core, please contact your **local Lattice Sales Office**.