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LatticeCORE

DDR3 PHY IP Core User Guide

IPUG96 Version 2.1, October 2016

The Double Data Rate (DDR3) Physical Interface (PHY) IP core is a general purpose IP core that provides connectivity between a DDR3 Memory Controller (MC) and DDR3 memory devices compliant with JESD79-3 specification. This DDR3 PHY IP core provides the industry standard DDR PHY Interface (DFI) bus at the local side to interface with the memory controller. The DFI protocol defines the signals, signal relationships, and timing parameters required to transfer control information and data to and from the DDDR3 devices over the DFI bus.

The DDR3 PHY IP core minimizes the effort required to integrate any available DDR3 memory controller with the Lattice FPGA's DDR3 primitives and thereby enables the user to implement only the logical portion of the memory controller in the user design. The DDR3 PHY IP core contains all the logic required for memory device initialization, write leveling, read data capture and read data de-skew that are dependent on Lattice FPGA DDR I/O primitives.

Quick Facts

Table 1-1 gives quick facts about the DDR3 SDRAM Controller IP core for ECP5™.

Table 1-1. DDR3 PHY IP Core Quick Facts for ECP5[1, 2]

		DDR3 PHY IP Configuration								
		x8 2cs	**x16 2cs**	**x24 2cs**	**x32 2cs**	**x40 2cs**	**x48 2cs**	**x56 2cs**	**x64 2cs**	**x72 2cs**
Core Requirements	FPGA Families Supported	ECP5								
	Minimal Device Needed[1]	LFE5UM-85F-8MG285C	LFE5UM-85F-8MG285C	LFE5UM-85F-8MG381C	LFE5UM-85F-8MG381C	LFE5UM-85F-8BG554C	LFE5UM-85F-8BG756C	LFE5UM-85F-8BG756C	LFE5UM-85F-8BG756C	LFE5UM-85F-8BG756C
Resource Utilization	Targeted Device	LFE5UM-85F-8BG756C								
	Data Path Width	8	16	24	32	40	48	56	64	72
	LUTs	940	1070	1040	1140	1260	1360	1380	1440	1550
	sysMEM EBRs	0								
	Registers	740	970	1000	1180	1360	1510	1690	1850	2020
Design Tool Support	Lattice Implementation	Lattice Diamond® 3.3								
	Synthesis	Synopsys® Synplify Pro® for Lattice I-2014.03L-SP1								
	Simulation	Aldec® Active-HDL™ 9.3 Lattice Edition								
		Mentor Graphics® ModelSim® 6.6								

1. Device configuration x8 is considered. For x4 or x16 configurations, the minimal device may be different.
2. The LFE5U and LFE5UM devices have the same Resource Utilization values.

Table 1-2 gives quick facts about the DDR3 PHY IP core for LatticeECP3™.

Table 1-2. DDR3 PHY IP Core Quick Facts for LatticeECP3

		DDR3 PHY IP Configuration								
		x8 2cs	**x16 2cs**	**x24 2cs**	**x32 2cs**	**x40 2cs**	**x48 2cs**	**x56 2cs**	**x64 2cs**	**x72 2cs**
Core Requirements	FPGA Families Supported	LatticeECP3								
	Minimal Device Needed[1]	LFE3-17EA-6FN256C	LFE3-17EA-6FN256C	LFE3-17EA-6FN484C	LFE3-17EA-6FN484C	LFE3-17EA-6FN484C	LFE3-35EA-6FN484C	LFE3-35EA-6FN672C	LFE3-70EA-6FN672C	LFE3-70EA-6FN1156C
Resource Utilization	Targeted Device	LFE3-150EA-8FN1156C								
	Data Path Width	8	16	24	32	40	48	56	64	72
	LUTs	929	1060	1180	1320	1320	1430	1520	1620	1730
	sysMEM EBRs	0								
	Registers	820	1130	1430	1740	1560	1740	1920	2090	2300
Design Tool Support	Lattice Implementation	Lattice Diamond 3.3								
	Synthesis	Synopsys Synplify Pro for Lattice I-2014.03L-SP1								
	Simulation	Aldec Active-HDL 9.3 Lattice Edition								
		Mentor Graphics ModelSim 6.6								

1. Device configuration x8 is considered. For x4 or x16 configurations, the minimal device may be different.

Features

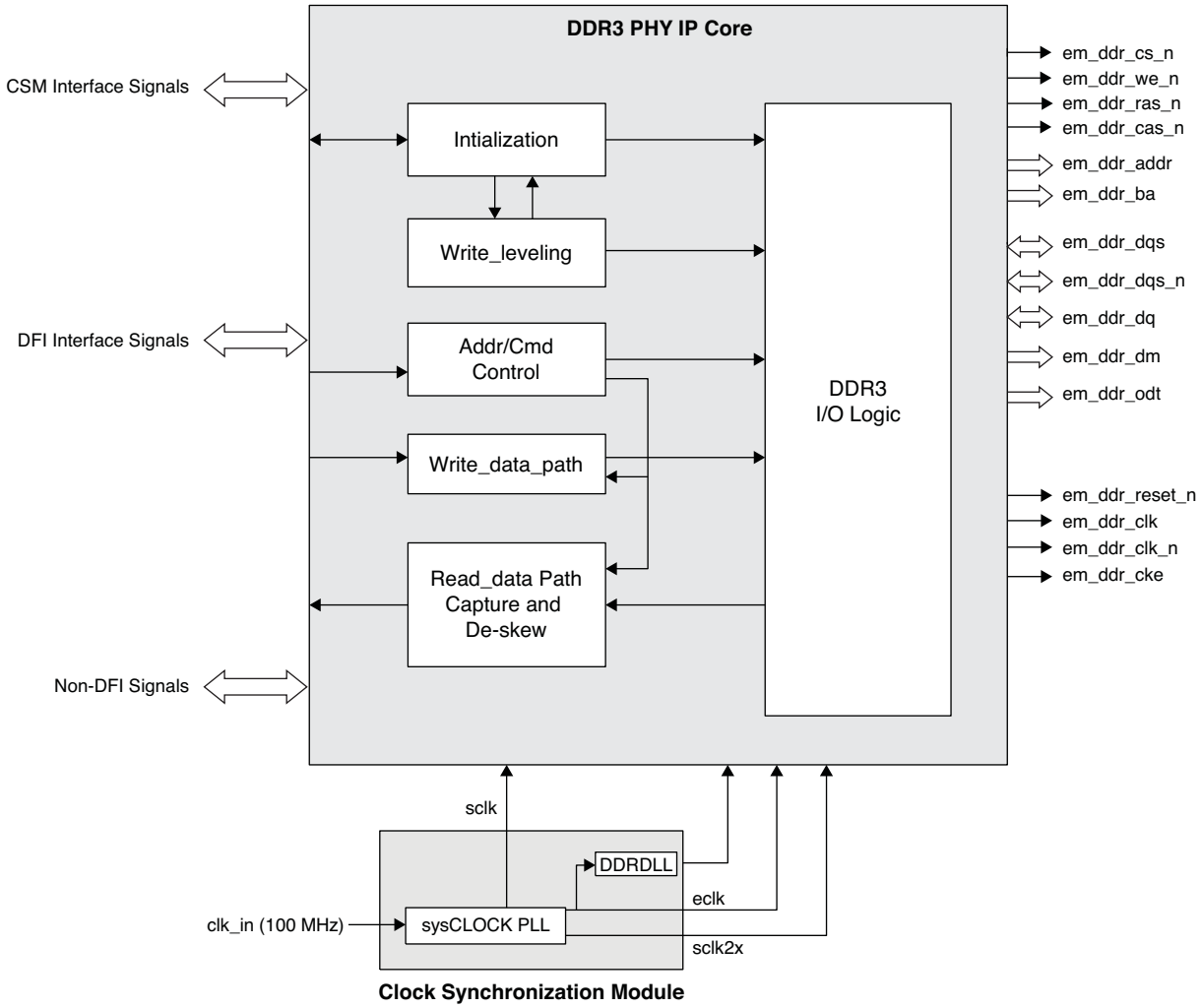
The DDR3 PHY IP core supports the following features:

- Interfaces to any DDR3 memory controller (MC) through the DDR PHY Interface (DFI) industry specification
- Interfaces to industry standard DDR3 SDRAM components and modules compliant with JESD79-3 specification
- Support for all ECP5 devices (LFE5U/LFE5UM) and all LatticeECP3 “EA” devices
- High-performance DDR3 operation up to 400 MHz/800 Mbps
- Supports memory data path widths of 8, 16, 24, 32, 40, 48, 56, 64 and 72 bits
- Supports x4, x8, and x16 device configurations
- Supports one unbuffered DDR3 DIMM or DDR3 RDIMM module with up to two ranks per DIMM
- Supports on-board memory (up to two chip selects)
- Programmable burst lengths of 8 (fixed), chopped 4 or 8 (on-the-fly), or chopped 4 (fixed)
- Supports automatic DDR3 SDRAM initialization with user mode register programming
- Supports write leveling for each DQS group. Option to switch off write leveling for on-board memory applications.
- Supports all valid DDR3 commands
- Supports dynamic On-Die Termination (ODT) controls
- I/O primitives manage read skews (read leveling equivalent)
- Option for controlling memory reset outside the IP core
- 1:1 frequency ratio interface between MC and DFI, 1:2 ratio between DFI and PHY

Overview

The DDR3 PHY IP core consists of the following sub-modules: initialization module, write leveling module, write data path, read data path, address/cmd control module and I/O logic module. This section briefly describes the operation of each of these modules. Figure 2-1 provides a high-level block diagram illustrating these main functional blocks and the technology used to implement the DDR3 PHY IP core functions.

Figure 2-1. DDR3 PHY IP Block Diagram



Along with the DDR3 PHY IP core, a separate module called the Clock Synchronization Module (CSM) is provided which generates all the clock signals, such as system clock (sclk), edge clock (eclk) and high-speed system clock (sclk2x) for the DDR3 PHY IP core. The CSM logic ensures that the domain crossing margin between eclk and sclk stays the same for the IDDR and ODDR buses that produce 2:1 gearing. Without proper synchronization, the bit order on different elements can become off sync and the entire data bus scrambled. Clock synchronization ensures that all DDR components start from exactly the same edge clock cycle.

The DDR3 PHY IP core works in a 1:1 frequency ratio between the MC and DFI. Inside the DDR3 PHY IP core, the initialization module, write leveling module, address/cmd control module, write data logic and read data capture

and de-skew logic operate using the sclk. These functional modules are implemented as soft logic in the FPGA fabric. This implies that the DFI of the DDR3 PHY IP core follows the 1:1 frequency ratio with the MC.

The DDR3 PHY IP core implements a 1:2 frequency ratio between the functional modules and the DDR I/O primitives. These I/O primitives are the hard logic of the FPGA and they use all the clocks (sclk, eclk and sclk2x) to implement a 1:2 gearing ratio between the functional block and the PHY memory interface. All transfers from the sclk to eclk domains and vice-versa happen within the DDR I/O primitives.

In a typical case, if the memory controller operates with a 200 MHz system clock (sclk), the functional modules of the DDR3 PHY IP core also operate with the same 200 MHz sclk while the DDR I/O logic of the IP core work primarily with the 400 MHz edge clock (eclk).

The combination of this operating clock ratio and the double data rate transfer leads to a user side data bus in the DFI that is four times the width of the memory side data bus. For example, a 32-bit memory side data width requires a 128-bit read data bus and a 128-bit write data bus at the user side interface.

Initialization Module

The Initialization Module performs the DDR3 memory initialization sequence as defined by JEDEC protocol. After power-on or after a normal reset of the DDR3 PHY IP core, memory must be initialized before sending any command to the IP core. It is the user's responsibility to assert the dfi_init_start input to the DDR3 PHY IP core to start the memory initialization sequence. The completion of initialization is indicated by the dfi_init_complete output provided by this block.

Since the DDR3 PHY IP core does not use the dfi_data_byte_disable or dfi_freq_ratio DFI signals, the input signal dfi_init_start needs to be asserted by the memory controller to trigger only a memory initialization process. It should be noted that this dfi_init_start signal is not used to change the frequency ratio.

Write Leveling

The write leveling block adjusts the DQS-to-CLK relationship for each memory device, using the write level mode of the DDR3 SDRAM when the fly-by wiring is implemented. Write leveling is always done immediately after a memory initialization sequence if write leveling is not disabled through the GUI. When the dfi_init_complete signal is asserted after the initialization process it also indicates the completion of write leveling. Along with the assertion of dfi_init_complete, the signal wl_err is also asserted if the write leveling process is not successful.

The main purpose of write leveling is to provide better signal integrity by using fly-by topology for the address, command, control and clock signals, and then by de-skewing the DQS signal delays to those signals at the DDR3 DRAM side. Since DDR3 memory modules have adapted fly-by topology, write leveling must be enabled for DIMM based applications. For on-board memory applications, the GUI provides the write leveling function as a user option. When enabled, the PCB for the on-board memory application must be routed using the fly-by topology. Otherwise, write leveling failures may occur due to the lack of guaranteed DQS to CLK edge relationship at the beginning of write level training. Due to this reason, the write leveling option must be disabled if the PCB does not utilize fly-by routing for write leveling.

The write leveling scheme of the DDR3 PHY IP core follows all the steps stipulated in the JEDEC specification. For more details on write leveling, refer to the JEDEC specification JESD79-3.

Read Training (Only for ECP5 Device)

For every read operation, the DDR3 I/O primitives of the ECP5 device must be initialized at the appropriate time to identify the incoming DQS preamble. Upon proper detection of the preamble, the primitive DQSBUFI extracts a clean dqs signal out of the incoming dqs signal from the memory and generates the DATAVALID output signal that indicates the correct timing window of the valid read data.

The DDR3 PHY IP generates an internal pulse signal, READ[3:0], to the primitive DQSBUFI that is used for the above-mentioned operation. In addition to the READ[3:0] input, another input signal READCLKSEL[2:0] and an

output signal, BURSTDET, of the DQSBUFI block are provided to the PHY IP to accomplish the READ signal positioning.

Due to the DQS round trip delay that includes PCB routing and I/O pad delays, proper positioning of the READ signal with respect to the incoming preamble is crucial for successful read operations. The ECP5 DQSBUFI block supports a dynamic READ signal positioning function called read training that enables the PHY IP to position the READ signal within an appropriate timing window by progressively shifting the READ signal and monitoring the positioning result.

This read training is performed as part of the memory initialization process after the write leveling operation is complete. During the read training, the PHY IP generates the READ[3:0] pulse, positions this signal using READCLKSEL[2:0] and monitors the BURSTDET output of DQSBUFI for the result of the current position. The READ signal is set high before the read preamble starts. When the READ pulse is properly positioned, the preamble is detected correctly and the BURSTDET will go high. This will guarantee that the generated DATAVALID signal is indicating the correct read valid time window.

The READ signal is generated in the system clock (SCLK) domain and stays asserted for the total burst length of the read operation.

A minimum burst length of four on the memory bus is used in the read training process. The PHY IP can determine the proper position alignment when there is not a single failure on BURSTDET assertions during the multiple trials. If there is any failure, the PHY IP shifts the READ signal position and tries again until it detects no BURSTDET failure.

The PHY IP stores the delay value of the successful position of the READ signal for each DQS group. It uses these delay values during a normal read operation to correctly detect the preamble first, followed by the generation of DATAVALID signal.

Selecting READ_PULSE_TAP Value (Only for LatticeECP3 Device)

For every read operation, the DDR3 I/O primitives must be initialized at the appropriate time to identify the incoming DQS preamble in order to generate the data valid signal. For this purpose the PHY IP internally generates a signal called dqs_read in such a way that this signal's trailing edge is positioned within the incoming DQS preamble window.

Due to PCB routing delays, DIMM module routing delays and routing delays within the FPGA, the incoming DQS signal's delay varies from board to board. To compensate for this variability in DQS delay, the PHY IP shifts the internal signal dqs_read in such a way to position it within the preamble time.

Each shift (step) moves the dqs_read signal by one half period of the eclk (1.25 ns for 400 MHz memory clock).

A port, read_pulse_tap, is provided in the Core top level file ddr3_sdram_mem_top_wrapper.v for the user to load the shift count for each DQS group. Each DQS group is assigned a 3-bit shift count value in this port, starting with LSB 3 bits for DQS_0. This count can be any value from 0 to 7.

For the core to work properly on the board, it is recommended that the dqs_read signal be shifted by two steps for UDIMMs, by four steps for RDIMMs or by one step for on-board memory. Since the Eval simulation environment is provided without the PCB and FPGA internal routing delays, the recommended values for Eval simulation are: zero steps for UDIMMs, two steps for RDIMMs or zero steps for on-board memory.

A parameter READ_PULSE_TAP in ddr_p_eval\testbench\tests\ecp3\tb_config_params.v is made available to the user as an example. This parameter may be loaded to the port read_pulse_tap with appropriate values for simulation and synthesis.

In almost all cases the recommended value is good enough for stable read operations on the board and it is highly unlikely that the user has to change this value. If there are frequent read errors on the board, the user should try adjusting the shift count value loaded to the port read_pulse_tap.

Should there be a need to change the READ_PULSE_TAP value, it is suggested that the user starts with changing the value of DQS7 groups first and then move to adjacent group, if required.

Note: *The DDR3 PHY IP may fail to generate or improperly generate the read_data_valid signal if the parameter READ_PULSE_TAP is not loaded to the read_pulse_tap input port or the values are not correct.*

Data Path Logic

The Data Path Logic (DPL) block interfaces with the DDR3 I/O modules and is responsible for generating the read data and read data valid signals during read operations. This block implements all the logic needed to ensure that the data write/read to and from the memory is transferred to the local user interface in a deterministic and coherent manner.

Write Data Path

The write data path block interfaces with the DDR3 I/O modules and is responsible for loading the write data along with write data control signals to the DDR3 I/O primitives during write operations. This block implements all the logic needed to ensure that the data write to the memory is transferred from the DFI in a deterministic and coherent manner.

Read Data Path

The read data path block interfaces with the DDR3 I/O modules and is responsible for extracting the read data and read data valid signals during read operations. This block implements all the logic needed to ensure that the data read from the memory is transferred to the DFI in a deterministic and coherent manner. In addition, this block has the logic to deskew the read data delays between different data lanes.

DDR3 I/O Logic

The DDR3 I/O logic block provides the physical interface to the memory device. This block consists mainly of the LatticeECP3 or ECP5 device DDR3 I/O primitives supporting compliance to DDR3 electrical and timing requirements. These primitives implement all the interface signals required for memory access and convert the single data rate (SDR) DFI data to double data rate DDR3 data for the write operations. In read mode, they perform the DDR3-to-SDR conversion.

Signal Descriptions

Table 2-1 describes the user interface and memory interface signals at the top level.

Table 2-1. DDR3 PHY IP Core Top-Level I/O List

Port Name	Active State	I/O	Description
clk_in	N/A	Input	Reference clock to the PLL of the CSM block.
Clock Synchronization Module (CSM) Interface Signals			
sclk	N/A	Input	System clock used by the PHY IP core. This clock can be used for the DDR3 memory controller.
eclk	N/A	Input	Edge clock used by the DDR3 PHY IP core. Usually twice the frequency of sclk.
sclk2x	N/A	Input	High-speed system clock used by the IP core. Usually twice the frequency of sclk. (Only for LatticeECP3.)
wl_rst_datapath	High	Input	Signal from the IP core to the CSM module requesting a reset to the DDR primitive after a write leveling process is done. If multiple PHY IP cores are implemented in a design, use an AND gate to feed the wl_rst_datapath signals from all PHY IP cores and connect the output of the AND gate to the wl_rst_datapath input of the CSM module. (Only for LatticeECP3.)
dqsbufd_rst	High	Output	Signal from the CSM module to the IP core to reset the DDR primitive. (Only for LatticeECP3.)

Table 2-1. DDR3 PHY IP Core Top-Level I/O List (Continued)

Port Name	Active State	I/O	Description
clocking_good	High	Input	Signal from the CSM module indicating a stable clock condition.
dqsdel	High	Input	Master DQSDLL delay control line from CSM to the slave DLL delay in the IP core. (Only for LatticeECP3.)
uddcntln	Low	Output	DQSDLL update request from the IP core to the CSM logic. (Only for LatticeECP3.)
dll_update	High	Output	DQSDLL update request from the IP core to the CSM logic. (Only for ECP5.) Remains asserted till update_done is set high.
dqsbuf_pause	High	Input	Pause signal from CSM to the DDR3 I/O logic. (Only for ECP5.)
ddr_rst	High	Input	Reset signal from CSM to the DDR3 I/O logic. (Only for ECP5.)
ddrdel	High	Input	Master DQSDLL delay control line from CSM to the slave DLL delay in the IP core. (Only for ECP5.)
ddrdel_br	High	Input	Eclk bridge DQSDLL delay control line from CSM to the slave DLL delay in the IP core. (Only for ECP5.)
update_done	High	Input	Signal to indicate DQSDLL update is completed. (Only for ECP5.) dll_update is de-asserted once this signal is sampled as high.
Non-DFI Interface Signals			
mem_rst_n	Low	Input	Asynchronous reset signal from the user to reset only the memory device. This signal will not reset the DDR3 PHY IP core's functional modules. Refer to the Reset Handling section for more details.
read_pulse_tap [3*(`DQS_WIDTH) -1:0]	N/A	Input	Read pulse tap – Counts the value from 0 to 7 by which the IP core's internal read pulse signal, dqs_read, is to be shifted for proper read_data_valid signal generation. Three bits are allocated for each DQS. Refer to the Netlist Simulation section for more details. (Only for LatticeECP3 DDR3 IP.)
phy_init_act	High	Output	Signal to indicate that the memory initialization process is active (in progress).
wl_act	High	Output	Signal to indicate that the memory write leveling process is active (in progress).
wl_err	High	Output	Write leveling error. Indicates failure in write leveling. The IP core will not work properly if there is a write leveling error. This signal should be checked when the init_done signal is asserted at the end of the initialization procedure.
rt_err	High	Output	Read Training error. Indicates failure in Read Training process. The PHY IP will not work properly if there is a Read Training error. This signal should be checked when init_done signal is asserted. (Only for ECP5 DDR3 IP.)
DFI Interface signals			
dfi_reset_n	Low	Input	Asynchronous reset. By default, when asserted, this signal resets the entire IP core and also the DDR3 memory. Refer to the Reset Handling section for more details.
dfi_address	N/A	Input	DFI address bus. This signal defines the address information that is intended for the DRAM memory devices for all control commands. The IP core preserves the bit ordering of the dfi_address signals when reflecting this data to the DRAM devices.
dfi_bank	N/A	Input	DFI bank bus. This signal defines the bank information that is intended for the DRAM devices for all control commands. The IP core preserves the bit ordering of the dfi_bank signals when reflecting this data to the DRAM devices.
dfi_cas_n	Low	Input	DFI column address strobe input. This signal defines the CAS information that is intended for the DRAM devices for all control commands.
dfi_cke[CKE_WIDTH-1:0]	High	Input	DFI clock enable input. This signal defines the CKE information that is intended for the DRAM devices for all control commands.

Table 2-1. DDR3 PHY IP Core Top-Level I/O List (Continued)

Port Name	Active State	I/O	Description
dfi_cs_n[CS_WIDTH-1:0]	Low	Input	DFI chip select input. This signal defines the chip select information that is intended for the DRAM devices for all control commands.
dfi_odt[CS_WIDTH-1:0]	High	Input	DFI on-die termination control input. This signal defines the ODT information that is intended for the DRAM devices for all control commands.
dfi_ras_n	Low	Input	DFI row address strobe bus. This signal defines the RAS information that is intended for the DRAM devices for all control commands.
dfi_we_n	Low	Input	DFI write enable input. This signal defines the WEN information that is intended for the DRAM devices for all control commands.
dfi_wrdata[DSIZE-1:0]	N/A	Input	Write data bus. Refer to the Write Data Interface section for more information.
dfi_wrdata_en	High	Input	Write data and data mask enable input. Refer to the Write Data Interface section for more information.
dfi_wrdata_mask[(DSIZE/8)[1:0]	High	Input	Write data byte mask input. Refer to the Write Data Interface section for more information.
dfi_rddata[DSIZE-1:0]	N/A	Output	Read data bus output. Refer to the Read Data Interface section for more information.
dfi_rddata_valid	High	Output	Read data valid indicator. Refer to the Read Data Interface section for more information.
dfi_init_complete	High	Output	This output signal is asserted for one clock period after the core completes memory initialization and write leveling. When sampled high, the input signal dfi_init_start must be immediately deasserted at the same edge of the sampling clock. Refer to the Initialization Control section for more details.
dfi_init_start	High	Input	Initialization start request input to the IP core. dfi_init_start should be asserted to initiate memory initialization either right after the power-on reset or before sending the first user command to the IP core. Since the DDR3 PHY IP core provides no support for dfi_data_byte_disable or dfi_freq_ratio, this input signal dfi_init_start is provided to the MC only to trigger a memory initialization process. Refer to the Initialization Control section for more details.
DDR3 SDRAM Memory Interface			
em_ddr_reset_n	Low	Output	Asynchronous reset signal from the controller to the memory device. Asserted by the controller for the duration of power on reset or active rst_n or active mem_rst_n. Refer to the Reset Handling section for more details.
em_ddr_clk[CLKO_WIDTH-1:0]	N/A	Output	Up to 400 MHz memory clock generated by the core. Lattice software automatically generates an additional complimentary port (em_ddr_clk_n) for each clock output port.
em_ ddr_cke[CKE_WIDTH -1 :0]	High	Output	Memory clock enable generated by the core.
em_ ddr_addr[ROW_WIDTH-1:0]	N/A	Output	Memory address bus – multiplexed row and column address information to the memory.
em_ ddr_ba[2:0]	N/A	Output	Memory bank address.
em_ ddr_data[DATA_WIDTH-1:0]	N/A	In/Out	Memory bi-directional data bus.
em_ ddr_dm[(DATA_WIDTH/8)-1:0]	High	Output	DDR3 memory write data mask
em_ ddr_dqs[DQS_WIDTH-1:0]	N/A	In/Out	Memory bi-directional data strobe. Lattice software automatically generates an additional complimentary port (em_ddr_dqs_n) for each dqs port.
em_ ddr_dqs_n[DQS_WIDTH-1:0]	N/A	In/Out	Memory complimentary bi-directional data strobe
em_ ddr_cs_n[`CS_WIDTH_BB -1 :0]	Low	Output	Memory chip select.
em_ ddr_cas_n	Low	Output	Memory column address strobe.

Table 2-1. DDR3 PHY IP Core Top-Level I/O List (Continued)

Port Name	Active State	I/O	Description
em_ ddr_ras_n	Low	Output	Memory row address strobe.
em_ ddr_we_n	Low	Output	Memory write enable.
em_ ddr_odt[`CS_WIDTH_BB -1 :0]	High	Output	Memory on-die termination control.

Using the DFI

The DFI specification includes a list of signals required to drive the memory address, command, and control signals to the DFI bus. These signals are intended to be passed to the DRAM devices in a manner that maintains the timing relationship of these signals on the DFI.

The DFI is subdivided into the following interface groups:

- Control Interface
- Write Data Interface
- Read Data Interface
- Update Interface (optional)
- Status Interface (optional)
- Training Interface (optional)
- Low Power Control Interface (optional)

The DDR3 PHY IP core provides support for the Control Interface, Write Data Interface and Read Data Interface. The other optional interfaces are not supported.

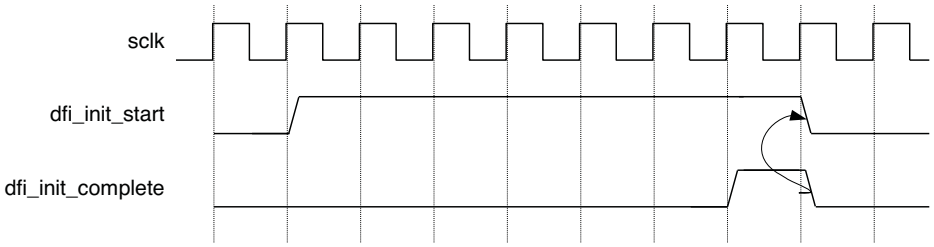
The Control Interface is a reflection of the DRAM control interface including address, bank, chip select, row strobe, column strobe, write enable, clock enable and ODT control, as applicable for the memory technology. The Write Data Interface and Read Data Interface are used to send valid write data as well as to receive valid read data across the DFI.

Initialization Control

DDR3 memory devices must be initialized before the memory controller accesses the devices. The DDR3 PHY IP core starts the memory initialization sequence when the dfi_init_start signal is asserted by the memory controller. Once asserted, the dfi_init_start signal needs to be held high until the initialization process is completed. The output signal dfi_init_done is asserted high by the core for only one clock cycle period indicating that the core has completed the initialization sequence and is now ready to access the memory. The dfi_init_start signal must be deasserted as soon as dfi_init_done is sampled high at the rising edge of sclk. If the dfi_init_start is left high at the next rising edge of sclk, the core sees this as another request for initialization and starts the initialization process again. Memory initialization is required only once, immediately after the system reset. As part of the initialization process the core performs write leveling for all the available DQS lanes and stores the write level delay values for each of those lanes. The core ensures a minimum gap of 500 µs between em_ddr_reset_n deassertion and the subsequent em_ddr_cke assertion. It is the user's responsibility to ensure minimum reset duration of 200 µs as required by the JEDEC specification.

Figure 2-2 shows the timing diagram of the initialization control signals.

Figure 2-2. Memory Initialization Control Timing



Command and Address

The DFI control signals dfi_address, dfi_bank, dfi_cas_n, dfi_cke, dfi_cs_n, dfi_reset_n, dfi_odt, dfi_ras_n and dfi_we_n correlate to the DRAM control signals.

These control signals are expected to be driven to the memory devices. The timing relationship of the control signals at the DFI bus are maintained at the PHY-DRAM boundary; meaning that all delays are consistent across all signals.

The DDR3 PHY IP core supports all the DDR3 memory commands. Refer to the DDR3 SDRAM Command Description and Operation table of the JESD79-3, DDR3 SDRAM Standard for more details about DDR3 memory commands.

Figure 2-3 shows the timing diagram for the Active command and Write/Read command when Additive Latency is selected as 0. The gap between the Active and Write/Read commands is derived from the t_{RCD} value of the memory device. Since the t_{RCD} value is expressed in terms of memory clocks, the corresponding System Clock count at the DFI bus is calculated as (t_{RCD} + 1) / 2. In this calculation, (t_{RCD} + 1) is used to round off the memory clock to sclk conversion.

Figure 2-4 shows the timing diagram for the Active command and Write/Read command when Additive latency is selected as 1 or 2.

On the memory side, the gap between the Active command and the Write/Read command will be 0, 1 or 2 memory clocks more than the t_{RCD} value. This extra delay is due to the combined effect of the 1:2 gearing in the DDR3 PHY IP core and the write/read latency value, odd or even.

Figure 2-3. Active to Write/Read Command Timing for AL=0

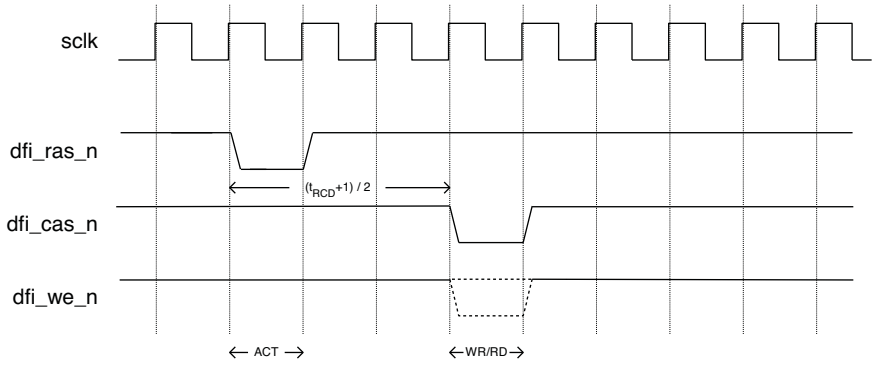
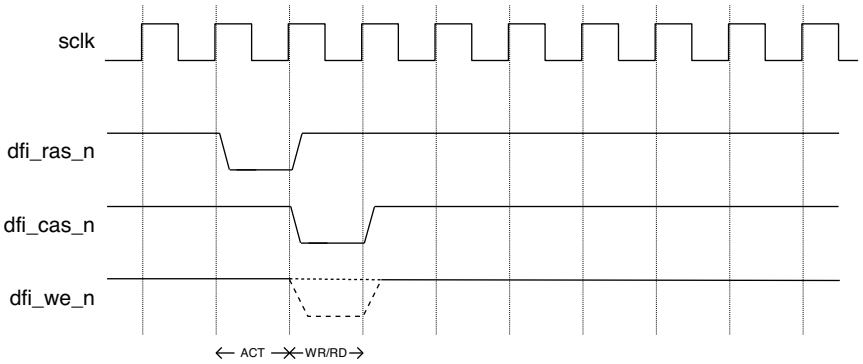


Figure 2-4. Active to Write/Read Command Timing for AL=1 and AL=2



Write Data Interface

The write transaction interface of the DFI includes the write data (dfi_wrdata), write data mask (dfi_wrdata_mask), and write data enable (dfi_wrdata_en) signals as well as the tphy_wrlat and tphy_wrdata delay timing parameters.

In the DDR3 PHY IP core, the parameter tphy_wrlat has a constant value which is the write latency in terms of the system clock (sclk). The tphy_wrlat is calculated using the equation, tphy_wrlat = (wr_lat +1) / 2 where wr_lat is write latency in terms of memory clock. (wr_lat+1) is used to round off the memory clock to sclk conversion.

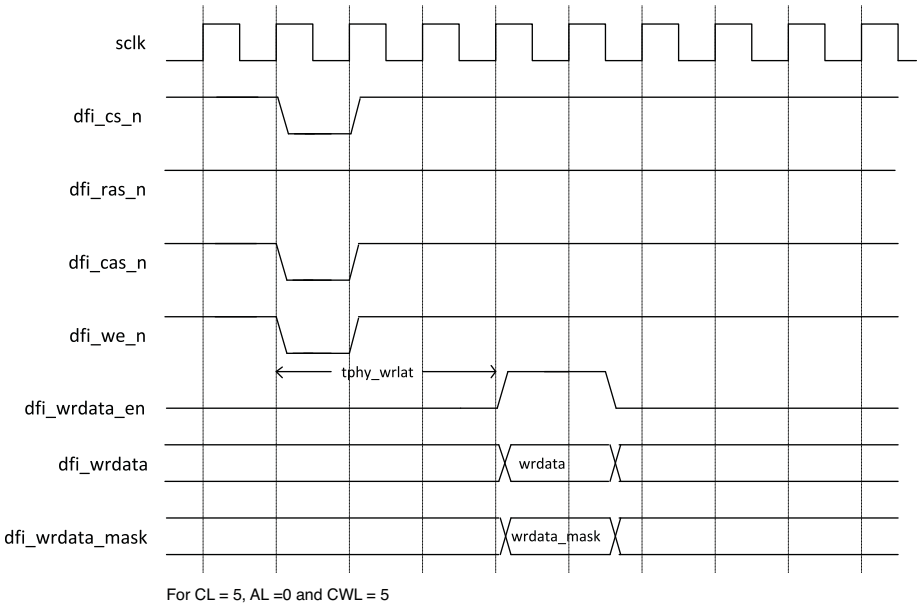
The parameter tphy_wrdata is always 0, therefore dfi_wrdata is valid from the time dfi_wrdata_en is asserted.

For a typical write operation, the memory controller asserts the dfi_wrdata_en signal tphy_wrlat cycles after the assertion of the corresponding write command on the DFI, and for the number of cycles required to complete the write data transfer sent on the DFI control interface. For contiguous write commands, the dfi_wrdata_en signal is to be asserted tphy_wrlat cycles after the first write command of the stream and is to remain asserted for the entire length of the data stream.

The associated write data (dfi_wrdata) and data masking (dfi_wrdata_mask) are sent along with the assertion of the dfi_wrdata_en signal on the DFI.

The write data timing on the DFI is shown in Figure 2-5. Refer to the evaluation simulation waveform for the DFI bus signal timing for different types of write operations (single, back-to-back, BC4 fixed, BL8 fixed and on-the-fly).

Figure 2-5. DFI Bus Write Timing



Read Data Interface

The read transaction portion of the DFI is defined by the read data enable (dfi_rddata_en), read data (dfi_rddata) bus and the valid (dfi_rddata_valid) signals as well as the trddata_en and tphy_rdlat timing parameters.

Since Lattice FPGAs support a preamble detect feature that automatically identifies read data valid timing, the signal dfi_rddata_en is not required for the DDR3 PHY IP core. The timing parameter trddata_en is also not required. The read command is accepted by the core when the dfi command input signal condition indicates a read command.

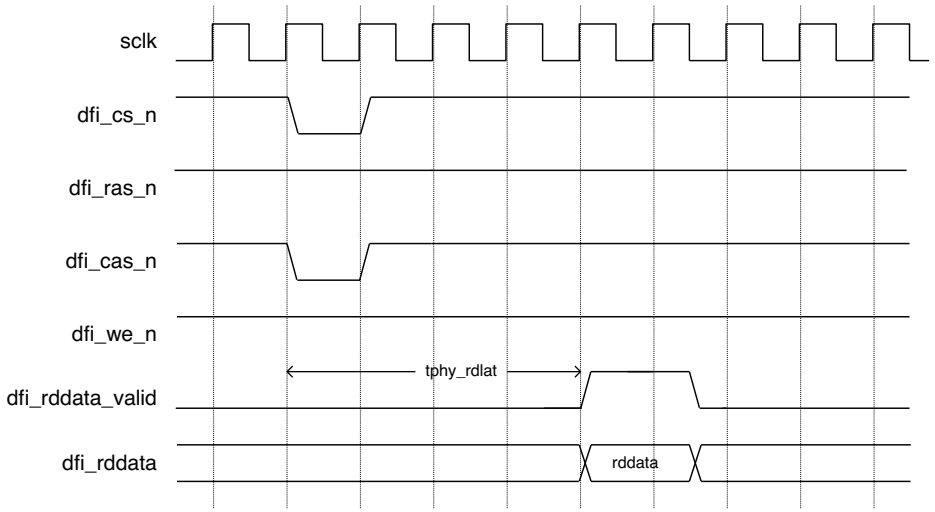
The DDR3 PHY IP core uses a total of nine sclks as core latency for the read command transmission, read data extraction and read data de-skewing. To calculate the tphy_rdlat value the memory device's read latency, in terms

of sclk, is added to this IP core's latency. For a memory read latency (RL) of six memory clocks, the corresponding tphy_rdlat is 12 sclks which is 9 + ((RL+1)/2). In this calculation, (RL+1) is used to round off the memory clock to sclk conversion.

The read data will be returned, along with the signal dfi_rddata_valid asserted, after tphy_rdlat cycles from the time the read command is asserted.

The read data timing on the DFI is shown in Figure 2-6. Refer to the evaluation simulation waveform for the DFI bus signal timing for the different types of read operations (single, back-to-back, BC4 fixed, BL8 fixed and on-the-fly).

Figure 2-6. DFI Bus Read Timing



Mode Register Programming

The DDR3 SDRAM memory devices are programmed using the mode registers MR0, MR1, MR2 and MR3. The bank address bus (dfi_bank) is used to choose one of the mode registers, while the programming data is delivered through the address bus (dfi_address). The memory data bus cannot be used for the mode register programming.

The initialization process uses the mode register initial values selected in the PHY IP GUI. If these mode registers are not re-programmed by the user logic, using the LMR command, they will remain in the same configurations as programmed during the initialization process. Table 2-2 shows the list of available parameters and their initial default values from GUI if they are not changed by the user.

Table 2-2. Initialization Default Values for Mode Register Settings

Type	Register	Value	Description	Local Address	GUI Setting
MR0	Burst Length	2'b00	Fixed 8	addr[1:0]	Yes
	Burst Type	1'b0	Sequential	addr[3]	Yes
	CAS Latency	3'b000	CL = 5	addr[6:4], addr[2]	Yes
	Test Mode	1'b0	Normal	addr[7]	No
	DLL Reset	1'b1	DLL Reset = Yes	addr[8]	No
	WR Recovery	3'b010	6	addr[11:9]	Yes
	DLL Control for precharge PD	1'b1	Fast	addr[12]	Yes
	All Others	0		addr[ROW_WIDTH-1:13]	No

Table 2-2. Initialization Default Values for Mode Register Settings (Continued)

Type	Register	Value	Description	Local Address	GUI Setting
MR1	DLL Enable	1'b0	DLL Enable	addr[0]	No
	ODI Control	2'b00	RZQ/6	Addr[5],addr[1]	Yes
	RTT_nom	3'b001	RZQ/4	Addr[9],addr[6],addr[2]	Yes
	Additive Latency	2'b00	Disabled	addr[4:3]	Yes
	Write Level Enable	1'b0	Disabled	addr[7]	No
	TDQS Enable	1'b0	Disabled	addr[11]	No
	Qoff	1'b0	Enable	addr[12]	No
	All Others	0		addr[ROW_WIDTH-1:13]	No
MR2	CAS Write Latency	3'b000	5	addr[5:3]	Yes
	Rtt_WR	2'b01	RZQ/4	Addr[10:9]	Yes
	All Others	0			No
MR3	All	0		addr[ROW_WIDTH-1:0]	No

Parameter Settings

DDR3 PHY IP core Configuration GUI in IPexpress (for ECP3) or in Clarity Designer (for ECP5) tool is used to create IP and architectural modules in the Lattice Diamond software. Refer to IP Core Generation and Evaluation for LatticeECP3 DDR3 PHY or IP Core Generation and Evaluation for ECP5 DDR3 PHY for a description of how to generate the IP core.

Table 3-1 provides a list of user-configurable parameters for the DDR3 PHY IP core. The parameter settings are specified using the DDR3 PHY IP core Configuration GUI in IPexpress. The numerous DDR3 PHY IP parameter options are partitioned across multiple GUI tabs as shown in this chapter.

Table 3-1. IP Core Parameters

Parameter	Range/Options	Default
Type Tab		
Device Information		
Select Memory	Micron DDR3 1Gb-25E / Micron DDR3 2Gb-25E / Micron DDR3 4Gb-25E / Custom	Micron DDR3 1Gb-25E
Clock	400 / 333 / 300 MHz (for -8, -8L or -9 device) 333 / 300 MHz (for -7 or -7L device) 300 MHz (for -6 or -6L device)	400 (for -8, -8L or -9 device) 333 (for -7 or -7L device) 300 (for -6 or -6L device)
Memory Configuration		
Memory Type	Unbuffered DIMM / On-board Memory/ Registered DIMM	Unbuffered DIMM
Memory Data Bus Size	8 / 16 / 24 / 32 /40 /48 / 56 / 64 / 72	32
Configuration	x4/ x8/ x16	x8
DIMM Type (or Chip Select Width)	Single Rank / Double Rank (or 1 / 2)	Single Rank (or 1)
Address Mirror	Enable / Disable	Disabled
Clock Width	1 / 2 / 4	1
CKE Width	1 / 2	1
2T Mode	Unselected/Selected	Unselected
Write Leveling	Unselected/Selected	Selected
Controller Reset to Memory	Unselected/Selected	Selected
Setting Tab		
Address		
Row Size	12 - 16	14
Column Size	10 -1 2	10
Mode Register Initial Setting		
Burst Length	Fixed 4, On the fly, Fixed 8	Fixed 8
CAS Latency	5,6,7,8	5
Burst Type	Sequential/Interleave	Sequential
Write Recovery	5,6,7,8,10,12	6
DLL Control for PD	Slow Exit/Fast Exit	Fast Exit
ODI Control	RZQ/6, RZQ/7	RZQ/6
RTT_Nom (ohm)	Disabled, RZQ/4, RZQ/2, RZQ/6, RZQ/12, RZQ/8	RZQ/4
Additive Latency	0, CL-1, CL-2	0
CAS Write Latency	5 / 6	5
RTT_WR	Off, RZQ/4, RZQ/2	RZQ/4

Table 3-1. IP Core Parameters (Continued)

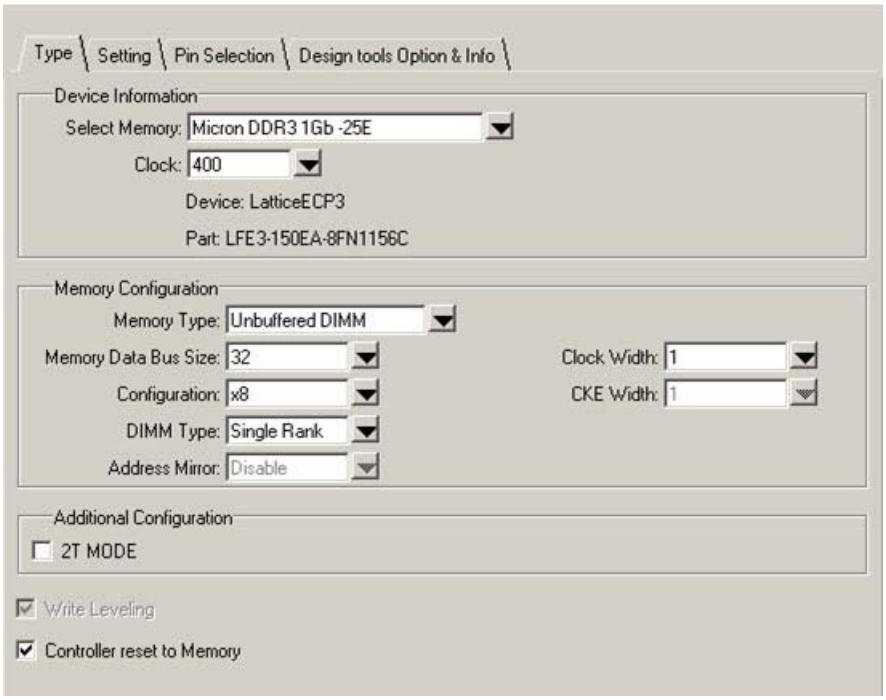
Parameter	Range/Options	Default
Pin Selection Tab (Only for LatticeECP3)		
Manually Adjust	Unselected / Selected	Unselected
Pin Side		
Left side	Unselected / Selected	Selected
Right side	Unselected / Selected	Unselected
clk_in / PLL Locations[1]		
clk_in pin	Refer Locate constraints[1]	U6[1]
PLL used	Refer Locate constraints[1]	PLL_R61C5[1]
DDR3 SDRAM Memory Clock Pin Location		
em_ddr_clk	(Bank 1[2] /Bank 2 /Bank 3) or (Bank 0[2] /Bank 6 /Bank 7)	Bank 6
DQS Locations		
DQS_0	Refer Locate constraints[1]	L10[1]
DQS_1	Refer Locate constraints[1]	M10[1]
DQS_2	Refer Locate constraints[1]	T9[1]
DQS_3	Refer Locate constraints[1]	W6[1]
DQS_4	Refer Locate constraints[1]	N/A[1]
DQS_5	Refer Locate constraints[1]	N/A[1]
DQS_6	Refer Locate constraints[1]	N/A[1]
DQS_7	Refer Locate constraints[1]	N/A[1]
DQS_8	Refer Locate constraints[1]	N/A[1]
Design Tools Option and Info Tab		
Design Tools Option		
Support Synplify	Unselected / Selected	Selected
Support ModelSim	Unselected / Selected	Selected
Support ALDEC	Unselected / Selected	Selected
Memory I/F Pins		
Number of BiDi Pins	Pin count for selected configuration	Pin count for selected configuration
Number of Output Pins	Pin count for selected configuration	Pin count for selected configuration
User I/F Pins		
Number of Input Pins	Pin count for selected configuration	Pin count for selected configuration
Number of Output Pins	Pin count for selected configuration	Pin count for selected configuration

1. The default values for the Pin Selection tab are target device-dependent. Default values provided in the table are for a LatticeECP3-150EA 1156-ball fpBGA device. Refer to Appendix C, LatticeECP3 DDR3 PHY IP Locate Constraints for further details.
2. The Bank 0 or Bank 1 option is available only for 333 MHz and 300 MHz speeds.

Type Tab

The Type tab allows the user to select a DDR3 PHY IP core configuration for the target memory device as well as the core functional features. These parameters are considered to be static parameters since the values for these parameters can only be set in the GUI. The DDR3 PHY IP core must be regenerated to change the value of any of these parameters. Figure 3-1 shows the contents of the Type tab.

Figure 3-1. DDR3 PHY IP Core Type Options



The Type tab supports the following parameters:

Select Memory

The Micron DDR3 1GB -25E is provided as the default DDR3 memory DIMM. The evaluation package comes with the memory model of this DIMM. The other option, Custom, provides a way to select timing and configuration settings for any other DIMM or on-board memory designs.

RefClock (Only for ECP5 DDR3 IP)

Refresh input clock to PLL which generates the system clock (SCLK) and memory clock (em_ddr_clk).

*ECP3 DDR3 PHY IP can only work with a refresh input clock to PLL which is one fourth of the memory clock selected in the next field **Clock** in this **Type** tab.*

Clock (for ECP3) **MemClock** (for ECP5)

This parameter specifies the frequency of the memory clock to the DIMM or on-board memory. The allowed range is from 300 MHz to 400 MHz. The default value is linked to the speed grade of Lattice device selected. For example, the default memory clock for ECP5 -8 devices is 400 MHz. The corresponding value for ECP5 -7 devices is 333 MHz, and the corresponding value for ECP5 -6 devices it is 300 MHz.

In addition to the default value, the -8 device also has 2 more clock frequency options (333 MHz and 300 MHz) and the -7 device has one more frequency option (300 MHz).

Memory Type

This option is used to select the DDR3 memory type: Unbuffered DIMM module (UDIMM or SODIMM) or Registered DIMM module. Users can also choose “On-board Memory” for designs that implement on-board devices instead of DIMMs.

Memory Data Bus Size

This option allows the user to select the data bus width of the DDR3 memory to which the DDR3 PHY IP core is connected. If the memory module has a wider data bus than required, only the required data width has to be selected.

Configuration

This option is used to select the device configuration of the DIMM or on-board memory. The DDR3 PHY IP core supports device configurations x4, x8, and x16.

DIMM0 Type or Chip Select Width

When Unbuffered DIMM or Registered DIMM is selected as the Memory Type, this option allows the user to select the number (Single/Dual) of ranks available in the selected DIMM.

When On-board Memory is selected as the Memory Type, this option allows the user to select the number of chip selects required for the on-board memory.

Address Mirror

This option allows the user to select an address mirroring scheme for rank1 if a Dual DIMM module is used. This option is not available for on-board memory.

Clock Width

This field shows the number of clocks with which the DDR3 PHY IP core drives the memory. The IP core provides one differential clock per rank/chip select, as default. Users can select up to two differential clocks per rank/chip select.

CKE Width

This field shows the number of Clock Enable (CKE) signals with which the PHY IP drives the memory. The IP core provides one CKE signal per Rank/Chip select, as default.

2T Mode

This option allows the user to enable or disable the 2T timing for command signals when Unbuffered DIMM or Onboard Memory is selected. This option is not available for Registered DIMM modules.

Write Leveling

This option allows the user to enable or disable the write leveling operation of the DDR3 PHY IP core. This option to enable/disable write leveling is available only when the Memory Type is selected as On-board Memory. For unbuffered DIMM or registered DIMM, write leveling is always enabled.

Refer to Initialization Module section for more information.

Controller Reset to Memory

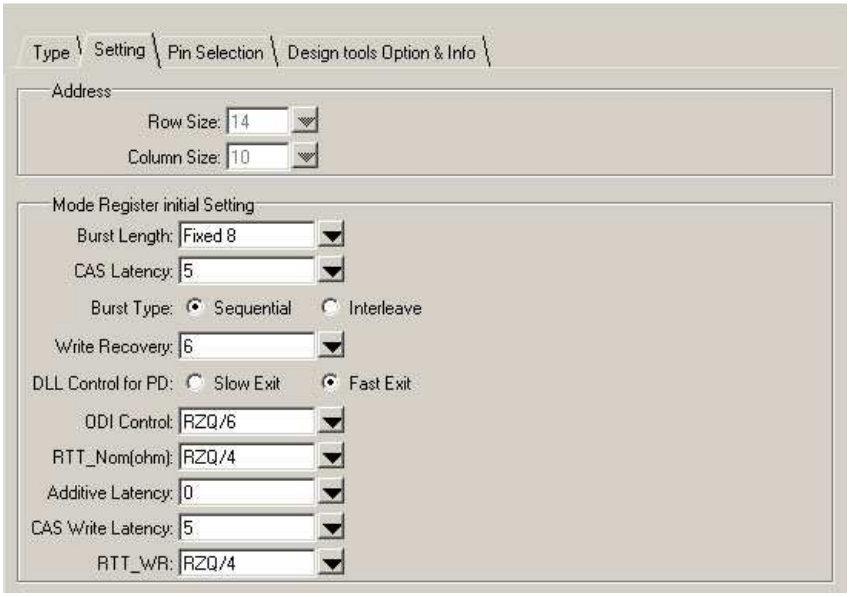
When this option is enabled, the asynchronous reset input signal, rst_n, to the DDR3 PHY IP core resets both the core and the memory devices. If this option is disabled (unchecked), the rst_n input of the core resets only the core, not the memory device. Refer to the Reset Handling section for more information.

Setting Tab

The Setting tab enables the user to select various configuration options for the target memory device/module. Parameters under the group, Mode Register Initial Setting, are dynamic parameters. Initialization values are set from the GUI. These values are dynamically changeable using LOAD_MR commands. Refer to the JESD79-3, DDR3 SDRAM Standard, for allowed the values.

Figure 3-2 shows the contents of the Setting tab.

Figure 3-2. DDR3 PHY IP Core Setting Options



The Setting tab supports the following parameters:

Row Size

This option indicates the default row address size used in the selected memory configuration. If the option “Custom” is selected in the Select Memory field of the Type tab, the user can choose a value other than the default value.

Column Size

This option indicates the default column address size used in the selected memory configuration. If the option “Custom” is selected in the Select Memory field of the Type tab, the user can choose a value other than the default value.

Burst Length

This option sets the Burst Length value in Mode Register 0 during initialization. This value remains until the user writes a different value to Mode Register 0.

CAS Latency

This option sets the CAS Latency value in Mode Register 0 during initialization. This value remains until the user writes a different value to Mode Register 0.

Burst Type

This option sets the Burst Type value in Mode Register 0 during initialization. This value remains until the user writes a different value to Mode Register 0.

Write Recovery

This option sets the Write Recovery value in Mode Register 0 during initialization. It is set in terms of the memory clock. This value remains until the user writes a different value to Mode Register 0.

DLL Control for PD

This option sets the DLL Control for Precharge PD value in Mode Register 0 during initialization. This value remains until the user writes a different value to Mode Register 0.

ODI Control

This option sets the Output Driver Impedance Control value in Mode Register 1 during initialization. This value remains until the user writes a different value to Mode Register 1.

RTT_Nom

This option sets the nominal termination, Rtt_Nom, value in Mode Register 1 during initialization. This value remains until the user writes a different value to Mode Register 1.

Additive Latency

This option sets the Additive Latency, AL, value in Mode Register 1 during initialization. This value remains until the user writes a different value to Mode Register 1.

CAS Write Latency

This option sets the CAS Write Latency, CWL, value in Mode Register 2 during initialization. This value remains until the user writes a different value to Mode Register 2.

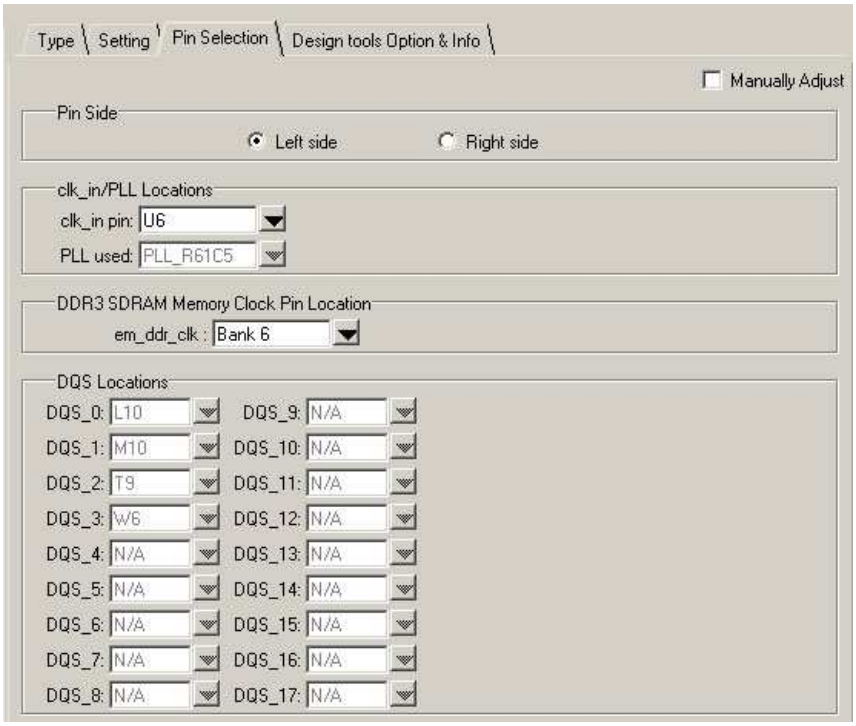
RTT_WR

This option sets the Dynamic ODT termination, Rtt_WR, value in Mode Register 2 during initialization. This value remains until the user writes a different value to Mode Register 2.

Pin Selection Tab

The Pin Selection tab enables users to assign device pin locations for reference input clock and DQS memory strobe signals. For each DQS location selected through this tab, the Lattice software automatically assigns pin locations for the associated DQ and DM signals. Figure 3-3 shows the contents of the Pin Selection tab. Refer to Appendix C: “DDR3 PHY IP Locate Constraints” for additional information.

Figure 3-3. DDR3 PHY IP Core Pin Selection Options (Only for LatticeECP3 Device)



Manually Adjust

The pin locations displayed in this tab are the default pin locations when the user selects the device LFE3-150EA-8FN1156C in the IPexpress GUI.

Users can specify alternate pin locations specific to their application and hardware implementation by selecting the Manually Adjust checkbox.

Pin Side

In LatticeECP3-EA devices, only the left or right side I/O banks can be used for DDR3 Data (DQ), Data Strobe (DQS) and Data Mask (DM) signals. The top and bottom I/O banks cannot be used for these signals.

This parameter allows the user to select the device side (left or right) for locating these DDR3 signals.

clk_in/PLL Locations

This parameter supports two options: clk_in pin and PLL used.

clk_in pin

In LatticeECP3-EA devices, there is a dedicated clock input pad for each PLL. This option provides, through a pull-down menu, a list of legal clock input pins allowed for the DDR3 PHY IP core on the selected side. Refer to Appendix C: “DDR3 PHY IP Locate Constraints” for additional clock input pin options.