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diDo

ARM Cortex-A8 CPU Module Family

ULTRA *Line*

HARDWARE MANUAL

DAVE Embedded Systems www.dave.eu info@dave.eu

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Table of Contents

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Illustration Index

1 Preface

1.1 About this manual

This Hardware Manual describes the DIDO CPU modules family design and functions.
Precise specifications for the Texas Instruments DM814x and AM387x processors can be found in the CPU datasheets and/or reference manuals.

1.2 Copyrights/Trademarks

1.3 Standards

DAVE Embedded Systems Srl is certified to ISO 9001 standards.

1.4 Disclaimers

DAVE Embedded Systems does not assume any responsibility about availability, supplying and support regarding all the products mentioned in this manual that are not strictly part of the DIDO CPU module.
DIDO CPU Modules are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. **DAVE Embedded Systems** customers who are using or selling these products for use in such applications do so at their own risk and agree to fully indemnify **DAVE Embedded Systems** for any damage resulting from such improper use or sale.

1.5 Warranty

DIDO is warranted against defects in material and

workmanship for the warranty period from the date of shipment. During the warranty period, **DAVE Embedded Systems** will at its discretion decide to repair or replace defective products. Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.
The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.
DAVE Embedded Systems will not be responsible for any defects or damages to other products not supplied by **DAVE Embedded Systems** that are caused by a faulty DIDO module.

1.6 Technical Support

We are committed to making our product easy to use and will help customers use our CPU modules in their systems.
Technical support is delivered through email to our valued customers. Support requests can be sent to support-dido@dave.eu.
Software upgrades are available for download in the restricted access download area of **DAVE Embedded Systems** web site: http://www.dave.eu/reserved-area. An account is required to access this area and is provided to customers who purchase the development kit (please contact support-dido@dave.eu for account requests)..
Please refer to our Web site at http://www.dave.eu/dave-cpu-module-dm814x-dido.html for the latest product documentation, utilities, drivers, Product Change Notifications, Board Support Packages, Application Notes, mechanical drawings and additional tools and software.

1.7 Related documents

Document	Location
DAVE Embedded Systems Developers Wiki	http://wiki.dave.eu/index.php/Main_Page
TMS320DM814x DaVinci Technical Reference Manual	http://www.ti.com/litv/pdf/sprugz8d
DM814x Overview (on TI Embedded Processors Wiki)	http://processors.wiki.ti.com/index.php/DM814x_Overview
Integration guide (on **DAVE Embedded Systems** Developers Wiki)	http://wiki.dave.eu/index.php/Integration_guide_%28Dido%29

Tab. 1: Related documents

1.8 Conventions, Abbreviations, Acronyms

Abbreviation	Definition
BTN	Button
DSP	Digital Signal Processor
DVO	Digital Video Output
GPI	General purpose input
GPIO	General purpose input and output
GPO	General purpose output
HDVPSS	HD Video Processing Subsystems
HDVCIP	HD Video Image Coprocessing
NELK	NAON Embedded Linux Kit
PCB	Printed circuit board

Abbreviation	Definition
RTC	Real time clock
SOM	System on module
VIP	Video Input Port
PMIC	Power Management Integrated Circuit
ZFF	Z Form Factor

Tab. 2: Abbreviations and acronyms used in this manual

Revision History

Version	Date	Notes
0.9.0	March 2013	First Draft
0.9.1	March 2013	First Release
0.9.2	March 2013	First Release with DIDO development kit Minor fixes
1.0.0	April 2013	Released with NELK 4.0.0 Minor fixes
1.0.1	May 2013	Added information on EMAC_RMREFCLK signal Minor fixes
1.0.2	December 2013	Fixed JTAG_TDO and JTAG_TCK pinout table entries
1.0.3	January 2014	Updated pin J2.97 information Minor fixes
1.0.4	April 2014	SPI2: removed J2.36 from the muxable signals Added HDMI CEC and HPDET information
1.0.5	August 2014	Added EMAC_RMREFCLK termination resistors information Updated block diagram Minor fixes

2 Introduction

DIDO is a ready-to-use CPU module/SOM family, based on Texas Instruments Cortex-A8 high performance application processor from DM814x (“DaVinci”) and AM387x (“Sitara”) models. DIDO is is the cutting edge solution for a high range of applications, including video surveillance cameras, medical video analysis, smart home controllers, security systems, automation and point of service.

Fig. 1: DIDO CPU module

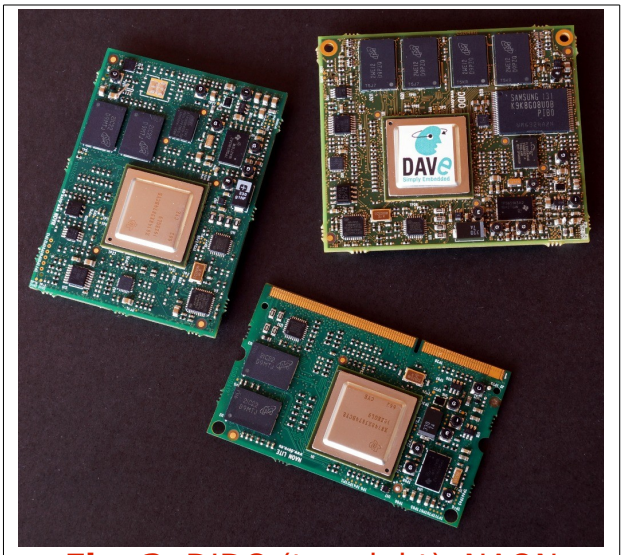


Fig. 2: DIDO (top-right), NAON (top-left) and MAYA (bottom)

DIDO is the first product of **DAVE Embedded Systems ULTRA Line** CPU modules class, which includes best-in-class solutions and full-featured SOMs.

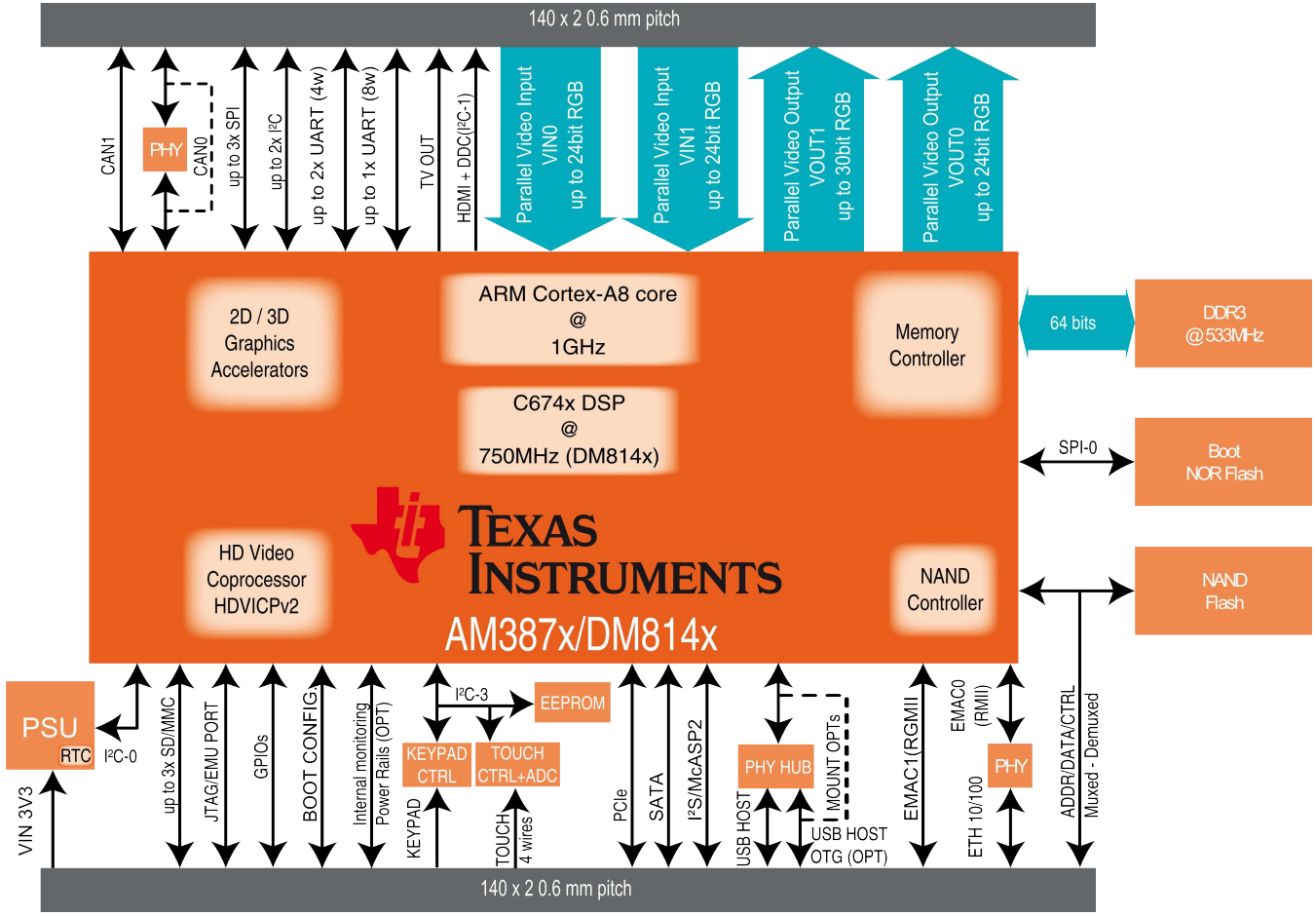
DIDO shares the same DM814x processor with MAYA (LITE Line) and NAON (ESATTA Line) and is built with the same connectors format (ZFF) as NAON and LIZARD (ESATTA Line).

2.1 Product Highlights

- Top class CPU module family based on Texas Instruments DM814x/AM387x processors models.
- ARM Cortex-A8 architecture @ up to 1 GHz
- Up to 2 GB DDR3 @ 533 MHz SDRAM
- HD Video Encoding/Decoding Capabilities (High-Definition Video Image Coprocessing – HDVICP v2 engine)
- Multiple video input and output channels
- C674x DSP engine (available on DM8148)
- NEON Multimedia co-processor and PowerVR® SGX 530 Vector/3D Graphics Engine
- On-board flash (NOR and NAND) storage
- Small form factor
- Rich interfaces set including PCI Express, dual CAN, dual Ethernet, SATA and native 3.3V I/O
- NAON and LIZARD (ESATTA Line) pinout compatible

Fig. 3: DIDO SOM (top view)

2.2 Block DiagramBlock Diagram



2.3 Feature Summary

Feature	Specifications	Options
CPU	“DaVinci” DM814x “Sitara” AM387x ARM v7 architecture Up to 1 GHz	
RAM	DDR3 SDRAM @ 533 MHz Up to 2 GB	
Storage	Flash NOR SPI Flash NAND on Local bus I²C 32 kbit EEPROM	
External local bus	16 bit GPMC	
Expansion bus	One PCI Express 2.0 Port With Integrated PHY (5.0 GT/s Endpoint/Root Complex port)	

Tab. 3: CPU, Memories, Busses

Feature	Specifications	Options
Graphics Controller	HD Video Processing Subsystem (HDVPSS) 1x up to 24 bit HD Video Output port 1x up to 18 bit HD Video Output port 1x HDMI 1.3 channel + DDC Analog TV output TFT/RGB support	
2D/3D Engines	NEON Multimedia SIMD coprocessor PowerVR SGX 530 3D Accelerator	
Coprocessors	Up to 750 MHz C674x VLIW DSP HD Video Coprocessor HDVICP v2	
Video capture	2x HD Video Input port	
USB	2x USB Host 2.0, 480 Mbps, with PHY 1x USB OTG, 480 Mbps (integrated PHY)	
UARTs	3x UARTs	
GPIO	Up to 128 lines, shared with other functions (interrupts available)	
Input interfaces	TSC2003 4-wire resistive touch screen controller	

Feature	Specifications	Options
	Available ADC channel Up to 8x8 keypad controller	
Networks	1x Fast Ethernet with PHY 1x GRMII 10/100/1000 Mbps interface High-end Dual CAN controller	
Storage	Serial ATA 3.0 Gbps with integrated PHY	
SD/MMC	Up to 3x MMC/SD/SDIO Serial interfaces (up to 48 MHz)	
Serial buses	2x I²C, 3x SPI	
Audio	1x McASP channel	
Timers	Up to 6 programmable general purpose timers (PWM function available)	
RTC	On board (provided by TPS659113 PMIC), external battery powered	
Debug	JTAG EMU port	

Tab. 4: Peripherals

Feature	Specifications	Options
Supply Voltage	+3.3V	
Active power consumption	See section 8.3 - Power consumption	
Dimensions	68.6 mm x 59.7 mm	
Weight	<tbd>	
MTBF	<tbd>	
Operation temperature	0..70 °C -40..+85 °C	
Shock	<tbd>	
Vibration	100 G resistance	
Connectors	2x 140 pin	
Connectors insertion/removal	<tbd>	

Tab. 5: Electrical, Mechanical and Environmental Specifications

3 Design overview

The heart of DIDO module is composed by the following components:

- Texas Instruments DM814x/AM387x processor
- Power supply unit
- DDR3 memory banks
- NOR and NAND flash banks
- 2x 140 pin connectors with interfaces signals

This chapter shortly describes the main DIDO components.

3.1 “DaVinci” DM814x / “Sitara” AM387x CPU

DM814x DaVinci™ and AM387x Sitara™ are highly-integrated, scalable and programmable CPU families from Texas Instruments.
DaVinci™ digital media processor solutions are tailored for digital audio, video, imaging, and vision applications.
Sitara™ ARM microprocessors (MPUs) are designed to optimize performance and peripheral support for customers in a variety of markets.
The architecture is designed to provide video, image, graphics and processing power sufficient to support the following:

- Home and Industrial automation
- Test and measurement
- Digital Signage
- Medical instrumentation
- Remote monitoring
- Motion control
- Point-of-Sale
- Single Board Computers

The following subsystems are part of the device:

- Microprocessor unit (MPU) subsystem based on the ARM® Cortex™-A8 architecture:

  - ARM Cortex-A8 RISC processor, with Neon™ Floating-Point Unit, 32KB L1 Instruction Cache, 32KB L1 Data Cache and 512KB L2 Cache
  - CoreSight Embedded Trace Module (ETM)
  - ARM Cortex-A8 Interrupt Controller (AINTC)
  - Embedded PLL Controller (PLL_ARM)
- PowerVR SGX 530 subsystem for vector/3D graphics acceleration to support display and gaming effects
- The HDVICP2 is a Video Encoder/Decoder hardware accelerator supporting a range of encode, decode, and transcode operations for most major video codec standards. The main video Codec standards supported in hardware are MPEG1/2/4 ASP/SP, H.264 BL/MP/HP, VC-1 SP/MP/AP, RV9/10, AVS-1.0, and ON2 VP6.2/VP7.
- The C674x DSP core is the high-performance floating-point DSP generation in the TMS320C6000™ DSP platform and is code-compatible with previous generation C64x Fixed-Point and C67x Floating-Point DSP generation. The C674x Floating-Point DSP processor uses 32KB of L1 program memory with EDC and 32KB of L1 data memory. The DSP has 256KB of L2 RAM with ECC, which can be defined as SRAM, L2 cache, or a combination of both.
- The high definition video processing subsystem (HDVPSS) includes video/graphics display and capture processing using the latest TI developed algorithms, flexible compositing and blending engine, and a full range of external video interfaces in order to deliver high quality video contents to the end devices.

The following table shows a **comparison** between the devices, highlighting the differences:

Processor	DSP	3D	HDVICP	HDVPSS	Max clock speed
DM8148	Yes	Yes	Yes	Yes	1 GHz
DM8147	Yes	n.a.	Yes	Yes	1 GHz

Processor	DSP	3D	HDVICP	HDVPSS	Max clock speed
AM3874	n.a.	Yes	n.a.	Yes	1 GHz
AM3872	n.a.	n.a.	n.a.	Yes	1 GHz
AM3871	n.a.	n.a.	n.a.	n.a.	1 GHz

Tab. 6: DM814x/AM387x comparison

3.2 DDR3 memory bank

DDR3 SDRAM memory bank is composed by 4x 16-bit width chips resulting in 2x 32-bit combined width banks.

The following table reports the SDRAM specifications:

CPU connection	SDRAM bus
Size min	128 MB
Size max	2 GB
Width	32 bit
Speed	533 MHz

Tab. 7: DDR2 specifications

3.3 NOR flash bank

NOR flash is a Serial Peripheral Interface (SPI) device. By default this device is connected to SPI channel 0 and acts as boot memory.
The following table reports the NOR flash specifications:

CPU connection	SPI channel 0
Size min	4 MByte
Size max	128 MByte
Bootable	Yes

Tab. 8: NOR flash specifications

3.4 NAND flash bank

On board main storage memory is a 8-bit wide NAND flash. By default it is connected to GPMC_NCS0 chip select. Optionally it

can be connected to GPMC_NCS7.

CPU connection	GPMC bus
Page size	512 byte, 2 kbyte or 4 kbyte
Size min	32 MByte
Size max	2 GByte
Width	8 bit
Bootable	Yes

Tab. 9: NAND flash specifications

3.5 Memory Map

The total system memory is divided across various processors/subsystems. Due to this “multiprocessor” nature, Memory Mapping for DIDO Module is quite complex, since it involves the Cortex-A8 core, the two Media Controllers (Cortex-M3, that take care of the HDVPSS and HDVCIP subsystems) and the DSP. NELK Memory Map is described in detail on the dedicated page on the Developer's Wiki: http://wiki.dave.eu/index.php/Memory_organization_%28Dido%29

3.6 Power supply unit

DIDO, as the other Performance Line CPU modules, embeds all the elements required for powering the unit, therefore power sequencing is self-contained and simplified. Nevertheless, power must be provided from carrier board, and therefore users should be aware of the ranges power supply can assume as well as all other parameters. For detailed information, please refer to Section 5.1.

3.7 CPU module connectors

All interface signals DIDO provides are routed through two 140 pin 0.6mm pitch stacking connectors (named J1 and J2). The host board must mount the mating connectors and connect the desired peripheral interfaces according to DIDO pinout specifications.
DIDO modules belongs to the ULTRA Line product class, but

the basic connectors pinout (called ZFF, Z Form Factor) is compatible with NAON and LIZARD SOMs. This means that the interfaces that are in common with the modules of the same class are routed on the same connector pins: for example, USB ports (which are implemented on each module) can be found on the same J1 and J2 pins. On the contrary, specific interfaces that are available only on one module are replaced with different interfaces on the other modules. As an example, the following table reports the three configuration of pin J2.33:

Module	*LIZARD*	*NAON*	*DIDO*
Pin	J2.33	J2.33	J2.33
Interface	LATCH	VOUT0	-
Pin name	LATCHED_A2	VOUT0_FLD/CAM_PCLK/GPMC_A12/GP2_02	DGND
Function	Latched address bit 2	Digital Video Output Field ID output	Ground

Tab. 10: ZFF form factor – example of pinout differences

For mechanical information, please refer to Section 4 (Mechanical specifications). For pinout and peripherals information, please refer to Sections 6 (Pinout table) and 7 (Peripheral interfaces).

4 Mechanical specifications

This chapter describes the mechanical characteristics of the DIDO module.

Mechanical drawings are available in DXF format from the DIDO page on DAVE Embedded Systems website (http://www.dave.eu/dave-cpu-module-am387x-dm814x-dido.html).

4.1 Board Layout

The following figure shows the physical dimensions of the DIDO module:

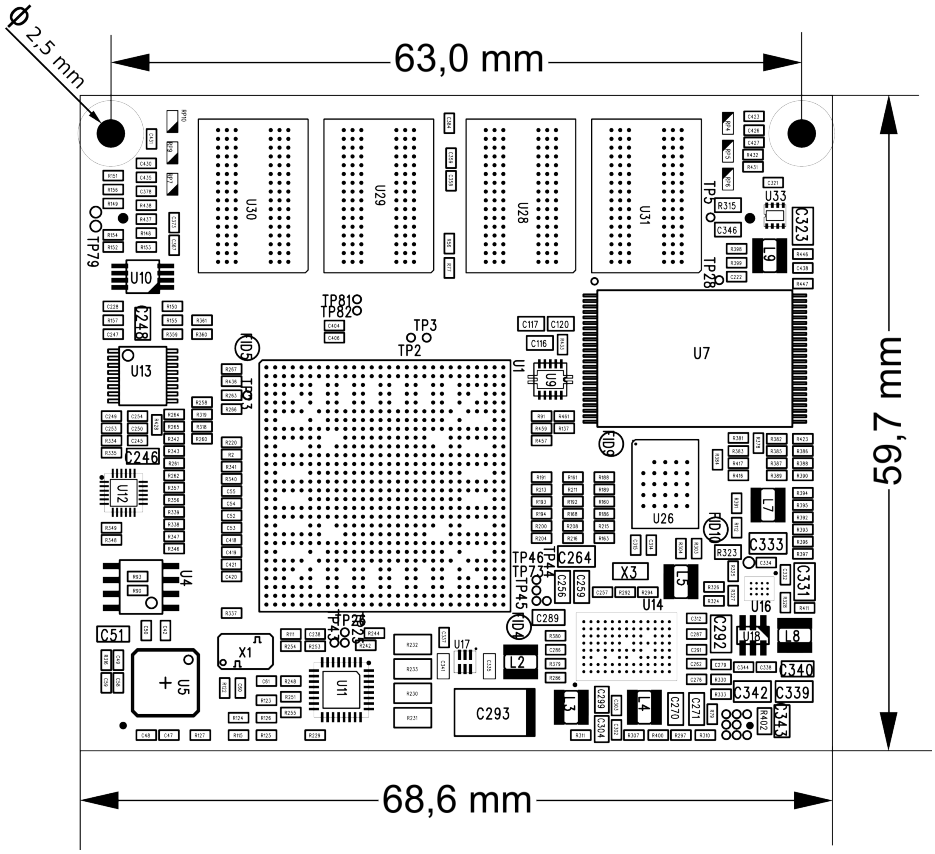


Fig. 4: Board layout - top view

- Board height: 59.7 mm
- Board width: 68.6 mm
- Maximum components height is 3.1 mm.
- PCB thickness is 1.8 mm.

The following figure highlights the maximum components' heights on DIDO module:

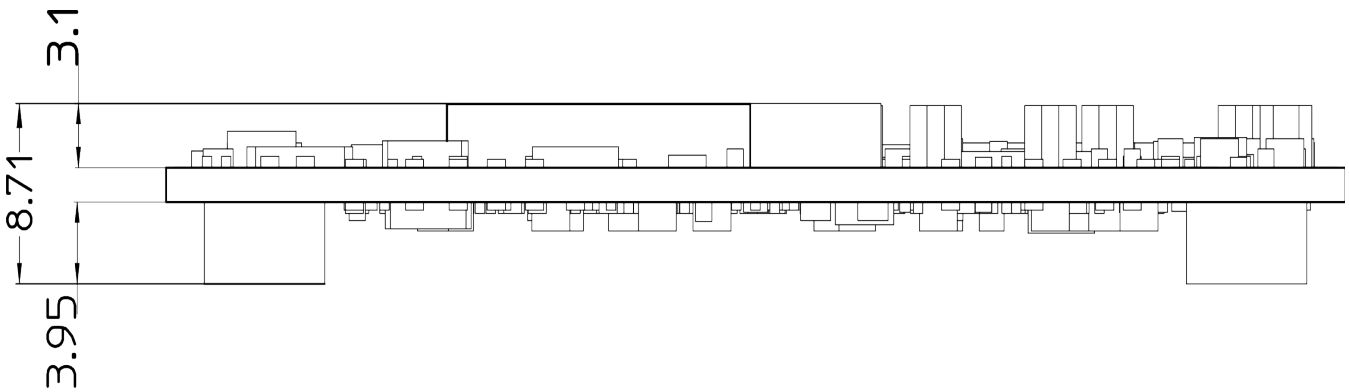


Fig. 5: Board layout - size view

4.2 Connectors

The following figure shows the DIDO connectors layout:

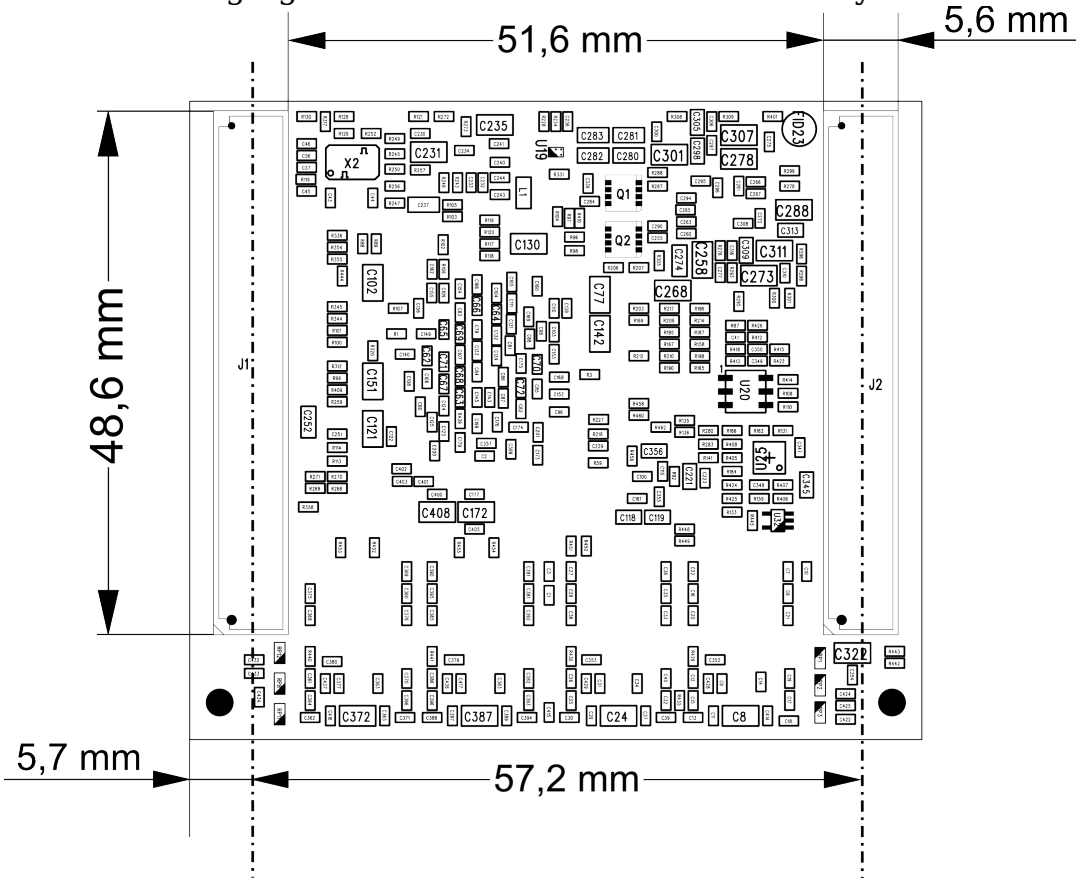


Fig. 6: Connectors layout

The following table reports connectors specifications:

Part number	Hirose FX8C-140S-SV
Height	5.6 mm
Length	48.6 mm
Depth	3.95 mm
Mating connectors	Hirose FX8C-140P-SV (5 mm board-to-board height) Hirose FX8C-140P-SV1 (6 mm board-to-board height) Hirose FX8C-140P-SV2 (7 mm board-to-board height) Hirose FX8C-140P-SV4 (9 mm board-to-board height) Hirose FX8C-140P-SV6 (11 mm board-to-board height)

5 System Logic

5.1 Power

Implementing correct power-up sequence for AM387x/DM814x processor is not a trivial task because several power rails are involved. DIDO hides this complexity because it embeds most of the circuitry required.
In typical applications AM387x/DM814x processor interfaces directly to 3.3V-powered devices that are hosted on carrier board. In order to be compliant with AM387x/DM814x power-up requirements, these devices should be turned on at a specific time during power-up sequence. To achieve this, DIDO provides EN_BCK2_LS signal. When DIDO is powered, this signal is low: this means that carrier board 3.3V-powered devices have to be powered off. During power-up sequence this signal shall be raised by DIDO circuitry, indicating carrier board 3.3V-powered devices have to be turned on. After this rising edge, EN_BCK2_LS shall be kept high.

5.2 PMIC

This section will be completed in a future version of this manual.

5.3 Reset

Five different signals are provided by DIDO SOM. Following sections describes in more detail each one.

5.3.1 MRST (J2.102)

This pin is connected to HDRST signal (cold reset) of PMIC TPS659113. When high, this signals keeps PMIC in off mode and resets TPS659113 to default settings. MRST has a weak internal pulldown.

5.3.2 PORSTn (J2.109)

PORSTn is a bidirectional open-drain signal. It is connected to:

- PORn input (Power-on Reset) of DM8148 processor
- output of voltage monitor (see Section 5.4)
- NRESPWRON2 output of PMIC.

Internal pullup is 10kOhm.

5.3.3 RSTOUTn (J2.91)

This output signal is asserted by DM8148 processor until it gets out of reset. It is usually used to reset external memories and peripherals connected to processor. It is connected to:

- RSTOUT_WD_OUTn pad of DM8148 processor
- 2k2 pull down resistor
- peripherals and memories.

In case it is used to reset devices on carrier board, its driving capability has to be taken into account.

5.3.4 CPU_RESETn (J2.15)

This input signal acts as External Warm Reset. It is connected to processor's RESETn pad. Internal pullup is 2.2kOhm.

5.3.5 JTAG_TRSTn (J2.100)

This input signal acts as Emulation Warm Reset. It is connected to processor's TRSTn pad. Internal pulldown is 4.7kOhm

5.4 Voltage monitor

DIDO SOM is equipped with a multiple-input voltage monitor whose reset output is connected to PORSTn. Monitored voltage rails include 3.3V provided by carrier board.

5.5 Boot options

Thanks to the versatility of internal BootROM, DM814x/AM387x processors provide a rich set of boot options and different configurations selectable via BTMODE[15:0] bootstrap pins. For a detailed explanation on the boot process for DM814x/AM387x processors, please refer to the Technical Reference Manual (available from TI website) at section ROM