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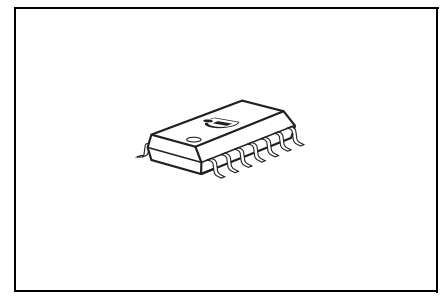
Step-Down DC/DC Controller

TLE 6389

AEC Qualified

RoHS

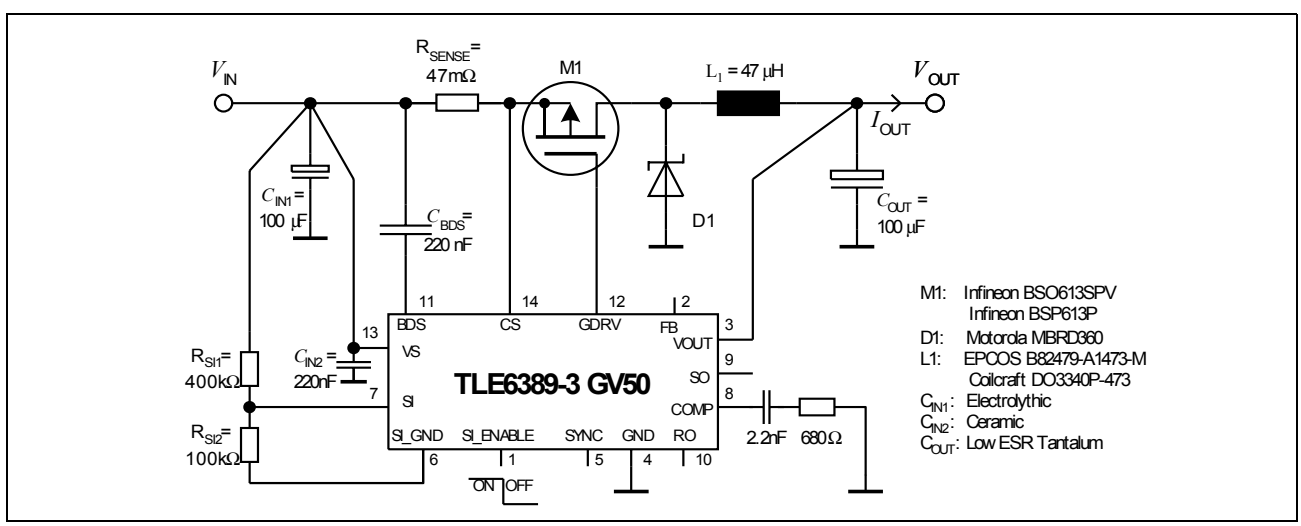
1 Overview



1.1 Features

- Input voltage range from < 5V up to 60V
- Output voltage: 5V fixed or adjustable (7V to 15V)
- Output voltage accuracy: 3%
- Output current up to 2.3A
- 100% maximum duty cycle
- Less than 120µA quiescent current at low loads[1)]
- 2µA max. shutdown current at device off (TLE 6389-2 GV)
- Fixed 360kHz switching frequency
- Frequency synchronization input for external clocks
- Current Mode control scheme
- Integrated output under voltage Reset circuit
- On chip low battery detector (on chip comparator)
- Automotive temperature range -40°C to 150 °C
- Green Product (RoHS compliant)
- AEC qualified

[1)] dependend on external components

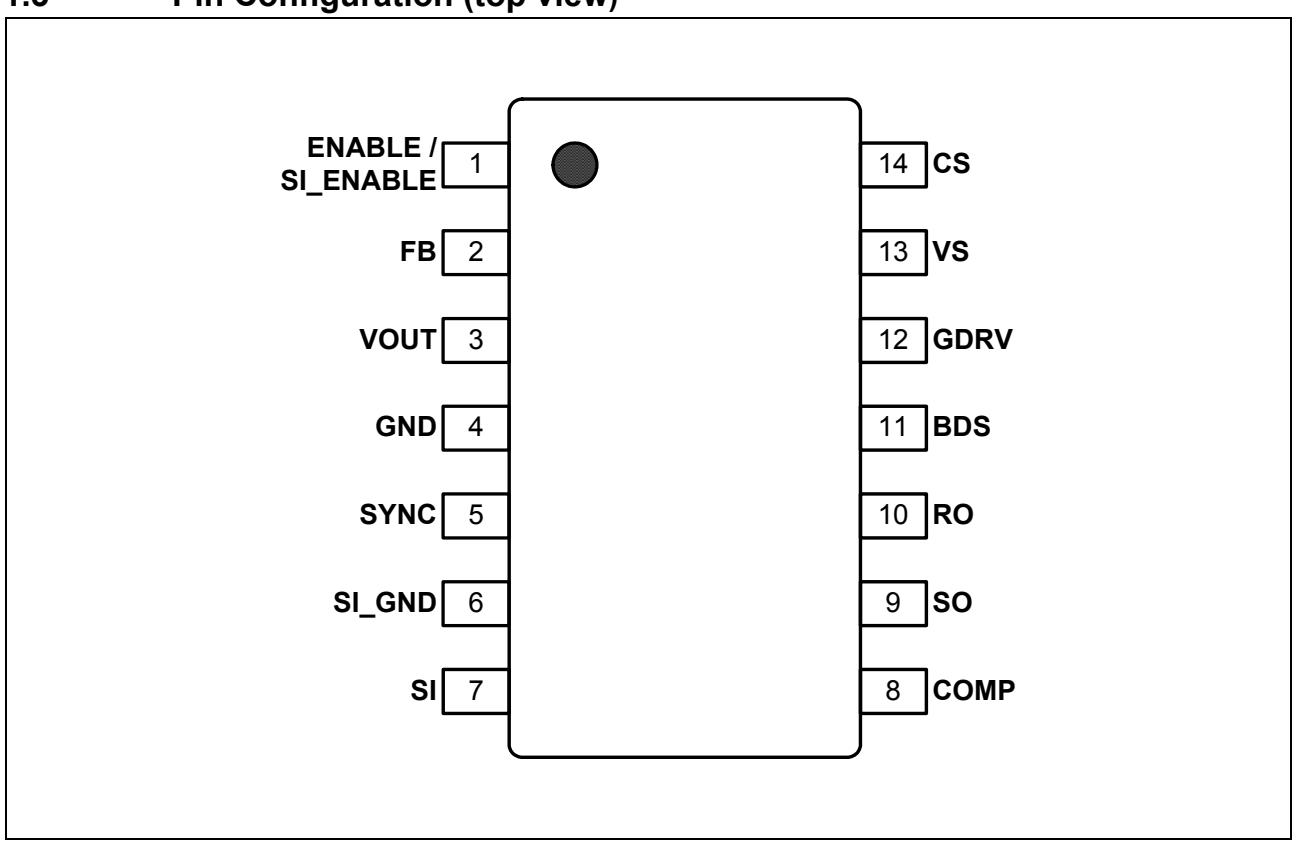


Type	Package	Description
TLE 6389-2 GV	PG-DSO-14-1	adjustable
TLE 6389-2 GV50	PG-DSO-14-1	5V, RO-Hysteresis <<
TLE 6389-3 GV50	PG-DSO-14-1	5V, RO-Hysteresis 1V

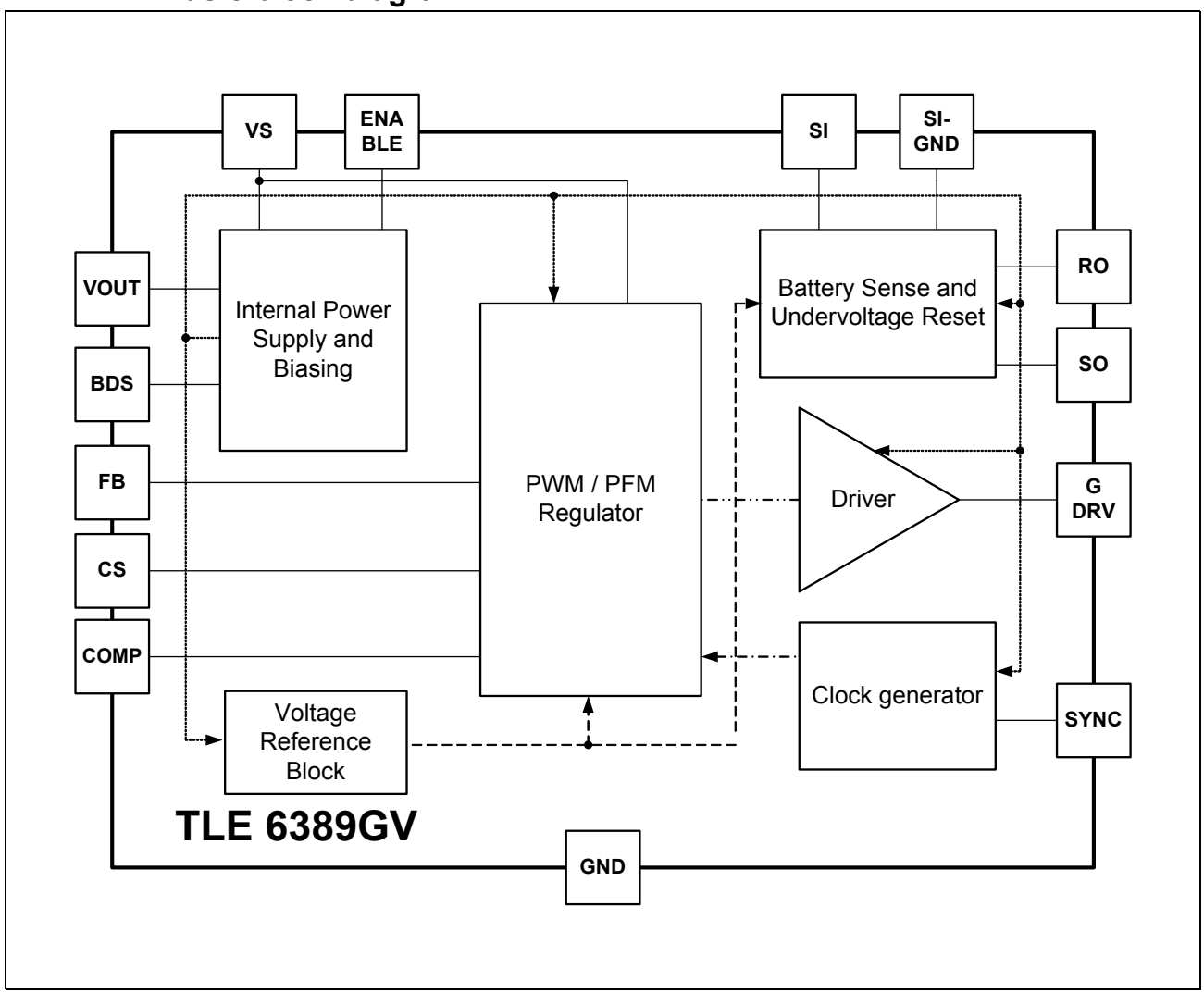
1.2 Short functional description

The TLE 6389 step-down DC-DC switching controllers provide high efficiency over loads ranging from 1mA up to 2.5A. A unique PWM/PFM control scheme operates with up to a 100% duty cycle, resulting in very low dropout voltage. This control scheme eliminates minimum load requirements and reduces the supply current under light loads to 120µA, depending on dimensioning of external components. In addition the adjustable version TLE6389-2 GV can be shut down via the Enable input reducing the input current to <2µA. The TLE 6389 step-down controllers drive an external P-channel MOSFET, allowing design flexibility for applications up to 12.5W of output power. A high switching frequency and operation in continuous-conduction mode allow the use of tiny surface-mount inductors. Output capacitor requirements are also reduced, minimizing PC board area and system costs. The output voltage is preset at 5V (TLE6389-2 GV50 and TLE6389-3 GV50) and adjustable for the TLE6389-2 GV. The version TLE6389-2 GV50 features a reset function with a threshold between 4.5V and 4.8V, including a small hysteresis of typ. 50mV. In the version TLE6389-3 GV50 the device incorporates a reset with a typ. 1V hysteresis. Input voltages of all TLE 6389 can be up to 60V.

1.3 Pin Configuration (top view)



1.4 Basic block diagram



1.5 Pin Definitions and Functions

Pin No	Symbol	Function
1	ENABLE	**Active-High enable input (only at adjustable version, TLE6389-2 GV) for the device.** The device is shut down when ENABLE is driven low. In this shut down-mode the reference, the output and the external MOSFET are turned off. Connect to logic high for normal operation.
1	SI_ENABLE	**Active-High enable input (only at 5V version, TLE6389-2 GV50 and TLE6389-3 GV50) for SI_GND input.** SI_GND is switched to high impedance when SI_ENABLE is low. High level at SI_ENABLE connects SI_GND to GND with low impedance. SO is undefined when SI_ENABLE is low.
2	FB	**Feedback input.** 1. For adjustable version (-2GV) connect this pin to an external voltage divider from the output to GND (see the determining the output voltage, application section). 2. At the 5V fixed output voltage version (-3GV50 and -2GV50) the FB is connected internally to an on-chip voltage divider. It does not have to be connected externally to the output.
3	VOUT	**Buck output voltage input.** Input for the internal supply. Connect always to the output of the buck converter (output capacitor).
4	GND	**Ground connection.** Analog signal ground.
5	SYNC	**Input for external frequency synchronization.** An external clock signal connected to this pin allows switching frequency synchronization of the device. The internal oscillator is clocked then by the frequency applied at the SYNC input.
6	SI_GND	**SI-Ground input.** Ground connection for SI comparator resistor divider. Depending on SI_ENABLE this input is switched to high impedance or low ohmic to GND.
7	SI	**Sense comparator input.** Input of the low-battery comparator. This input is compared to an internal 1.25V reference where SO gives the result of the comparison. Can be used for any comparison, not necessarily as battery sense.
8	COMP	**Compensation input.** Connect via RC-compensation network to GND.
9	SO	**Sense comparator output.** Open drain output from SI comparator at the adjustable version (TLE6389-2 GV), Pull down structure with an internal 20kΩ pull up resistor to VOUT at the 5V version (TLE6389-2 GV50 and TLE6389-3 GV50).

Pin No	Symbol	Function
10	RO	**Reset output.** Open drain output from undervoltage reset comparator at the adjustable version (TLE6389-2 GV), Pull down structure with an internal 20kΩ pull up resistor to VOUT at the 5V version (TLE6389-2 GV50 and TLE6389-3 GV50).
11	BDS	**Buck driver supply input.** Connect a ceramic capacitor between BDS and VS to generate clamped gate-source voltage to supply the driver of the PMOS power stage.
12	GDRV	**Gate drive output.** Connect to the gate of the external P-Channel MOSFET**.** The voltage at GDRV swings between the levels of VS and BDS.
13	VS	**Device supply input.** Connect a 220nF ceramic cap close to the pin in addition to the low ESR tantalum input capacitance.
14	CS	**Current-sense input.** Connect current-sense resistor between VS and CS. The voltage drop over the sense-resistor determines the peak current flowing in the buck circuit. The external MOSFET is turned off when the peak current is exceeded.

2 Absolute Maximum Ratings

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
	Device supply input VS					
2.1	Voltage	V_{VS}	-0.3	61	V	–
2.2	Current	I_{VS}	–	–	–	
	Current sense input CS					
2.3	Voltage	V_{CS}	-0.3	61	V	$\lvert V_{VS} - V_{CS}\rvert < 0.3V$
2.4	Current	I_{CS}	–	–	–	
	Gate drive output GDRV					
2.5	Voltage	V_{GDRV}	– 0.3	61	V	$-0.3V < \lvert V_{VS} - V_{GDRV}\rvert < 6.8V$; $-0.3V < \lvert V_{BDS} - V_{GDRV}\rvert < 6.8V$
2.6	Current	I_{GDRV}	–	–	–	limited internally
	Buck driver supply input BDS					
2.7	Voltage	V_{BDS}	– 0.3	61	V	$-0.3V < \lvert V_{VS} - V_{BDS}\rvert < 6.8V$
2.8	Current	I_{BDS}	–	–	–	
	Feedback input FB					
2.9	Voltage	V_{FB}	– 0.3	6.8	V	
2.10	Current	I_{FB}	–	–	–	
	Enable input SI_ENABLE					
2.11	Voltage	V_{SI_ENABLE}	– 0.3	61	V	TLE6389-2 GV50, TLE6389-3 GV50
2.12	Current	I_{SI_ENABLE}	–	–	–	
	SI-Ground input SI_GND					
2.13	Voltage	V_{SI_GND}	– 0.3	61	V	
2.14	Current	I_{SI_GND}	–	–	–	
	Enable input ENABLE					
2.15	Voltage	V_{ENABLE}	– 0.3	61	V	TLE6389-2 GV
2.16	Current	I_{ENABLE}	–	–	–	

2 Absolute Maximum Ratings (cont'd)

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
	Sense comparator input SI					
2.17	Voltage	V_{SI}	– 0.3	61	V	
2.18	Current	I_{SI}	–	–	–	
	Sense comparator output SO					
2.19	Voltage	V_{SO}	– 0.3	6.8	V	
2.20	Current	I_{SO}	–	–	–	limited internally
	Buck output voltage input VOUT					
2.21	Voltage	V_{VOUT}	– 0.3	15	V	TLE6389-2 GV
2.22	Voltage	V_{VOUT}	– 0.3	6.8	V	TLE6389-2 GV50, TLE6389-3 GV50
2.23	Current	I_{VOUT}	–	–	mA	
	Compensation input COMP					
2.24	Voltage	V_{COMP}	– 0.3	6.8	V	
2.25	Current	I_{COMP}	–	–	mA	
	Reset output RO					
2.26	Voltage	V_{RO}	– 0.3	6.8	V	
2.27	Current	I_{RO}	–	–	mA	limited internally
	Frequency synchronization input SYNC					
2.28	Voltage	V_{SYNC}	– 0.3	6.8	V	
2.29	Current	I_{SYNC}	–	–	mA	
	ESD-Protection					
2.30	Electrostatic discharge voltage	V_{ESD}	–1.5	1.5	kV	HBM[1], pin VOUT
2.31		V_{ESD}	-2	2	kV	HBM[1], all pins except VOUT
2.32		V_{ESDCDM}	–500	500	V	CDM[2]

2 Absolute Maximum Ratings (cont'd)

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
	Temperatures					
2.33	Junction temperature	T_j	-40	150	°C	–
2.34	Storage temperature	T_{stg}	-50	150	°C	–

1) ESD susceptibility HBM according to EIA/JESD 22-A 114B.

2) ESD susceptibility CDM according to JESD 22-C101.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

3 Operating Range

Item	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
3.1	Supply voltage range	V_{VS}	5	60	V	
3.2	Output voltage adjust range TLE 6389-2 GV	V_{OUT}	7	15	V	TLE 6389-2 GV
3.3	Sense Resistor	R_{SENSE}	10	47	mΩ	Calculation see section 7
3.4	PMOS, on+off delay	$t_{on+off\ delay}$	-	t_{min}- 300 [1]	ns	$t_{min}= V_{VOUT}/(V_{VS}*f_{SW})$
3.5	Buck driver supply capacitor	C_{BDS}	220	-	nF	
3.6	Buck inductance	L1	47	-	µH	recommended value
3.7	Buck inductance	L1	22	100	µH	
3.8	Buck output capacitor	C_{OUT}	100	-	µF	
3.9	Junction temperature	T_j	– 40	150	°C	
	Thermal Resistance					
3.10	Junction ambient	R_{thj-a}		140	K/W	Footprint only
3.11	Junction pin	R_{thj-p}		50	K/W	–

[1] A too high PMOS on+off delay might cause an instable output voltage

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4 Electrical Characteristics

5V < V_{VS} < 48V; -40°C < T_j < 150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	Current Consumption[1] TLE6389-2 GV50 and TLE6389-3 GV50						
4.1	Current consumption of VS	I_{VS}		80	150	µA	V_{VS} = 48V; PFM mode;
4.2				70	85	µA	V_{VS} = 13.5V; PFM mode; T_j = 25 °C
4.3	Current consumption of SI_ENABLE	I_{SI_ENABLE}		9	30	µA	V_{VS} = 48V; V_{SI_ENABLE} = 48V; PFM mode;
4.4	Current consumption of VOUT	I_{VOUT}		95	130	µA	V_{SI_ENABLE} = L; V_{VOUT} = 5.5V; V_{VS}=13.5V; PFM mode; T_j = 25°C
4.5				140	220	µA	V_{SI_ENABLE} = H; V_{VOUT} = 5.5V; V_{VS} = 13.5V; V_{SI} > $V_{SI, high}$; PFM mode;
4.6	Current consumption of SI	I_{SI}		0.2	0.5	µA	V_{VS} = 13.5V; V_{SI_ENABLE} = H; V_{SI} = 10V ; PFM mode;

4 Electrical Characteristics (cont'd)

5V < V_{VS} < 48V; -40°C < T_j < 150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	Current Consumption[1] TLE6389-2 GV (variable)						
4.7	Current consumption of VS	I_{VS}		80	150	µA	V_{VS} = 48V; V_{ENABLE} = H; PFM mode; V_{OUT} ≥ 7V
4.8	Current consumption of VS			70	85	µA	V_{VS} = 13.5V; V_{ENABLE} = H; PFM mode; T_j = 25 °C; V_{OUT} ≥ 7V
4.9	Current consumption of VS				2	µA	V_{ENABLE}=0V; T_j < 105°C
4.10	Current consumption of ENABLE	I_{EN}		9	30	µA	V_{VS} = 48V; V_{ENABLE} = H; PFM mode;
4.11	Current consumption of VOUT	I_{VOUT}		140	220	µA	V_{OUT} = 8V; V_{VS} = 13.5V; V_{ENABLE} = H; V_{SI} > $V_{SI, high}$; PFM mode;
4.12	Current consumption of SI	I_{SI}		0.2	0.5	µA	V_{VS} = 13.5V; V_{ENABLE} = H; V_{SI} = 10V ; PFM mode; T_j = 25°C
4.13	Current consumption of FB	I_{FB}		0.2	0.5	µA	V_{VS} = 13.5V; V_{FB} = 1.25V; V_{ENABLE} = H; PFM mode; T_j = 25°C

4 Electrical Characteristics (cont'd)

5V < V_{VS} < 48V; -40°C < T_j < 150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	Buck Controller						
4.14	Output voltage	V_{VOUT}	4.85	5.00	5.15	V	TLE6389-2 GV50, TLE6389-3 GV50; V_{VS}=13.5V& 48V; PWM mode I_{OUT} = 0.5 to 2A; R_{SENSE} = 22mΩ; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;
4.15			4.75	5.00	5.25	V	TLE6389-2 GV50, TLE6389-3 GV50; V_{VS} = 24V;PFM; I_{OUT} = 15mA; R_{SENSE} = 22mΩ; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;
4.16			3.8			V	TLE6389-3 GV50; V_{VS} decreasing from 5.8V to 4.2V; I_{LOAD} = 0mA to 500mA; R_{SENSE} = 22mΩ; R_{M1} = 0.4Ω; R_{L1} = 0.1Ω;
4.17	FB threshold voltage	$V_{FB, th}$	1.225	1.25	1.275	V	TLE6389-2 GV
4.18	Output voltage	V_{VOUT}	9.7	10.0	10.3	V	TLE6389-2 GV; Calibrated divider, see section 7.3; V_{VS} = 13.5V & 48V; I_{OUT} = 0.5 to 2A; PWM Mode; R_{SENSE} = 22mΩ; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;

4 Electrical Characteristics (cont'd)

5V < V_{VS} < 48V; -40°C < T_j < 150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.19	Output voltage	V_{VOUT}	9.5	10.0	10.5	V	TLE6389-2 GV; Calibrated divider, see section 7.3; V_{VS} = 24V; I_{OUT} = 15mA; PFM Mode; R_{SENSE} = 22mΩ; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;
4.20	Buck output voltage adjust range	V_{VOUT}	$V_{FB,th}$		7	V	TLE6389-2 GV, supplied by VS only, complete current to supply the IC drawn from VS, no reset function [2]
4.21	Buck output voltage adjust range	V_{VOUT}	7		15	V	TLE6389-2 GV, current to supply the IC drawn from VS and VOUT, as specified, [2]
4.22	Buck output voltage accuracy	V_{VOUT}	0.97* V_{OUT_nom}		1.03* V_{OUT_nom}		TLE6389-2 GV, PWM mode [2]
4.23	Buck output voltage accuracy	V_{VOUT}	0.95* V_{OUT_nom}		1.05* V_{OUT_nom}		TLE6389-2 GV, PFM mode [2]

4 Electrical Characteristics (cont'd)

5V < V_{VS} < 48V; -40°C < T_j < 150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.24	Line regulation	$\lvert \Delta V_{VOUT} \rvert$			35	mV	TLE6389-2 GV50, TLE6389-3 GV50, V_{VS} = 9V to 16V; I_{OUT} = 1A; R_{SENSE} = 22mΩ; PWM mode
4.25	Line regulation	$\lvert \Delta V_{VOUT} \rvert$			50	mV	TLE6389-2 GV50, TLE6389-3 GV50, V_{VS} = 16V to 32V; I_{OUT} = 1A; R_{SENSE} = 22mΩ; PWM mode
4.26	Line regulation	ΔV_{VOUT} / V_{VOUT}			2.5	%	TLE6389-2 GV, V_{VS} = 12V to 36V; V_{VOUT}=10V I_{OUT} = 1A; R_{SENSE} = 22mΩ; PWM mode

4 Electrical Characteristics (cont'd)

5V < V_{VS} < 48V; -40°C < T_j < 150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.27	Load regulation	ΔV_{VOUT} / ΔI_{LOAD}		40		mV/ A	TLE6389-2 GV50, TLE6389-3 GV50, I_{OUT} = 0.5A to 2A; V_{VS} = 5.8V & 48V; R_{SENSE} = 22mΩ
4.28				8* V_{OUT_nom}/ V		mV/ A	TLE6389-2 GV, I_{OUT} = 0.5 to 2A; V_{VS}= 13.5V & 48V; R_{SENSE} = 22mΩ
4.29	Gate driver, PMOS off	V_{VS} – V_{GDRV}	0		0.2	V	V_{ENABLE/SI_ENABLE} = 5 V C_{BDS} = 220 nF C_{GDRV} = 4.7nF
4.30	Gate driver, PMOS on	V_{VS} – V_{GDRV}	6		8.2	V	V_{ENABLE/SI_ENABLE} = 5 V C_{BDS} = 220 nF C_{GDRV} = 4.7nF[3)]
4.31	Gate driver, UV lockout	V_{VS} – V_{BDS}	2.75		4	V	Decreasing (V_{VS}-V_{BDS}) until GDRV is permanently at VS level
4.32	Gate driver, peak charging current	I_{GDRV}		1		A	PMOS dependent; [2)]
4.33	Gate driver, peak discharging current	I_{GDRV}		1		A	PMOS dependent; [2)]
4.34	Gate driver, gate voltage, rise time	t_r		45	60	ns	V_{ENABLE/SI_ENABLE} = 5 V C_{BDS} = 220 nF C_{GDRV} = 4.7nF

4 Electrical Characteristics (cont'd)

5V < V_{VS} < 48V; -40°C < T_j < 150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.35	Gate driver, gate voltage, fall time	t_f		50	65	ns	V_{ENABLE/SI_ENABLE} = 5 V C_{BDS} = 220 nF C_{GDRV} = 4.7nF
4.36	Peak current limit threshold voltage	V_{LIM} = V_{VS} – V_{CS}	50	70	90	mV	
4.37	Oscillator frequency	f_{OSC}	290	360	420	kHz	PWM mode only
4.38	Maximum duty cycle	d_{MAX}	100			%	PWM mode only
4.39	Minimum on time	t_{MIN}		220	400	ns	PWM mode only
4.40	SYNC capture range	Δf_{sync}	250		530	kHz	PWM mode only
4.41	SYNC trigger level high	$V_{SYNC,h}$	4.0			V	2)
4.42	SYNC trigger level low				0.8	V	2)
	Reset Generator						
4.43	Reset threshold	$V_{VOUT, RT}$	3.5	3.65	3.8	V	TLE6389-3 GV50; V_{VOUT} decreasing
4.44			4.5	4.65	4.8	V	TLE6389-3 GV50; V_{VOUT} increasing
4.45	Reset headroom	$V_{RT,HEAD}$	80			mV	TLE6389-2 GV50; V_{OUT}(V_S=6V, I_{LOAD}=1A) -$V_{VOUT,RT}$
4.46	Reset threshold	$V_{VOUT, RT}$	4.5	4.65	4.8	V	TLE6389-2 GV50; V_{VOUT} increasing/ decreasing
4.47	Reset threshold hysteresis	$\Delta V_{VOUT, RT}$		50		mV	TLE6389-2 GV50 2)

4 Electrical Characteristics (cont'd)

5V < V_{VS} < 48V; -40°C < T_j < 150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
4.48	Reset threshold	$V_{FB, RT}$		1.12		V	TLE6389-2 GV; V_{VOUT} decreasing
4.49				1.17		V	TLE6389-2 GV; V_{VOUT} increasing
4.50	Reset output pull up resistor	R_{RO}	10	20	40	kΩ	TLE6389-2 GV50, TLE6389-3 GV50; Internally connected to V_{OUT}
4.51	Reset output High voltage	$V_{RO, H}$	0.8* V_{VOUT}			V	TLE6389-2 GV50, TLE6389-3 GV50; I_{RO}=0mA
4.52	Reset output Low voltage	$V_{RO,L}$		0.2	0.4	V	$I_{RO, L}$=1mA; 2.5V < V_{VOUT} < V_{RT}
4.53	Reset output Low voltage	$V_{RO,L}$		0.2	0.4	V	$I_{RO, L}$=0.2mA; 1V < V_{VOUT} < 2.5V
4.54	Reset delay time	t_{rd}	17	21	25	ms	TLE6389-2 GV TLE6389-3 GV50
4.55	Reset delay time	t_{rd}	70	82	100	ms	TLE6389-2 GV50
4.56	Reset reaction time	t_{rr}			10	µs	2)
	Overvoltage Lockout						
4.57	Overvoltage threshold	$V_{VOUT, OV}$		V_{OUT_nom}/V +0.1		V	TLE6389-2 GV50, TLE6389-3 GV50; V_{VOUT} increasing
4.58	Overvoltage threshold	$V_{FB, OV}$		V_{FB,th_nom}/V +0.02		V	TLE6389-2 GV; V_{VOUT} increasing

4 Electrical Characteristics (cont'd)

5V < V_{VS} < 48V; -40°C < T_j < 150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	ENABLE Input						
4.59	Enable ON-threshold	$V_{ENABLE, ON}$	4.5			V	
4.60	Enable OFF-threshold	$V_{ENABLE, OFF}$			0.8	V	
	SI_ENABLE Input						
4.61	Enable ON-threshold	$V_{ENABLE, ON}$	4.5			V	
4.62	Enable OFF-threshold	$V_{ENABLE, OFF}$			0.8	V	
	SI_GND Input						
4.63	Switch ON resistance	R_{SW}	50	100	230	Ω	V_{SI_ENABLE} = 5V; I_{SI_GND} = 3mA;
	Battery Voltage Sense						
4.64	Sense threshold	$V_{SI, low}$	1.22	1.25	1.28	V	V_{VS} decreasing
4.65	Sense threshold	$V_{SI, high}$		1.33		V	V_{VS} increasing
4.66	Sense threshold hysteresis	$V_{SI, hys}$	50	80	120	mV	
4.67	Sense output pull up resistor	R_{SO}	10	20	40	kΩ	TLE6389-2 GV50, TLE6389-3 GV50; Internally connected to V_{VOUT}
4.68	Sense out output High voltage	$V_{SO,H}$	0.8* V_{VOUT}			V	$I_{SO,H}$ =0mA
4.69	Sense out output Low voltage	$V_{SO,L}$		0.2	0.4	V	$I_{SO,L}$ = 1mA; 2.5V < V_{VOUT}; V_{SI} < 1.13 V
4.70				0.4	V_{VOUT} /V	V	I_{SOL}=0.2mA; 1V < V_{VOUT} < 2.5V; V_{SI} < 1.13 V

4 Electrical Characteristics (cont'd)

5V < V_{VS} < 48V; -40°C < T_j < 150°C;

All voltages with respect to ground; positive current defined flowing into the pin; unless otherwise specified

Item	Parameter	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
	Thermal Shutdown						
4.71	Thermal shutdown junction temperature	T_{jSD}	150	175	200	°C	2)
4.72	Temperature hysteresis	ΔT		30		K	2)

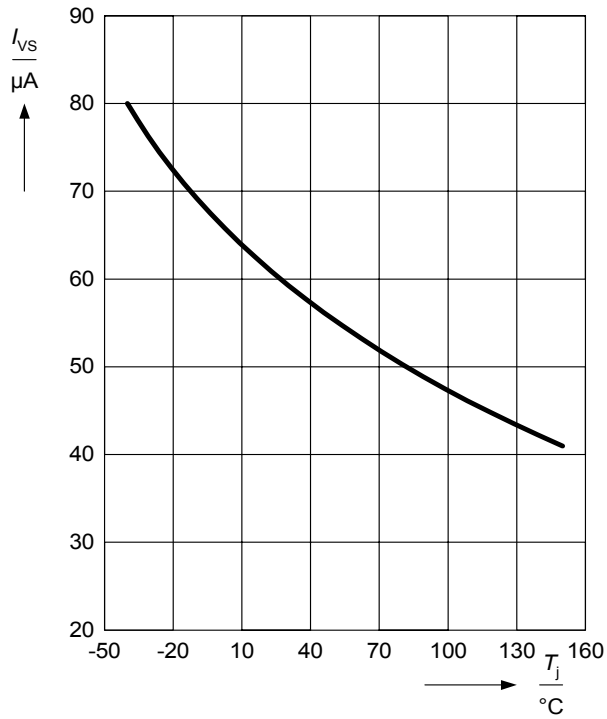
1) The device current measurements for I_{VS} and I_{FB} exclude MOSFET driver currents.

2) Not subject to production test - specified by design

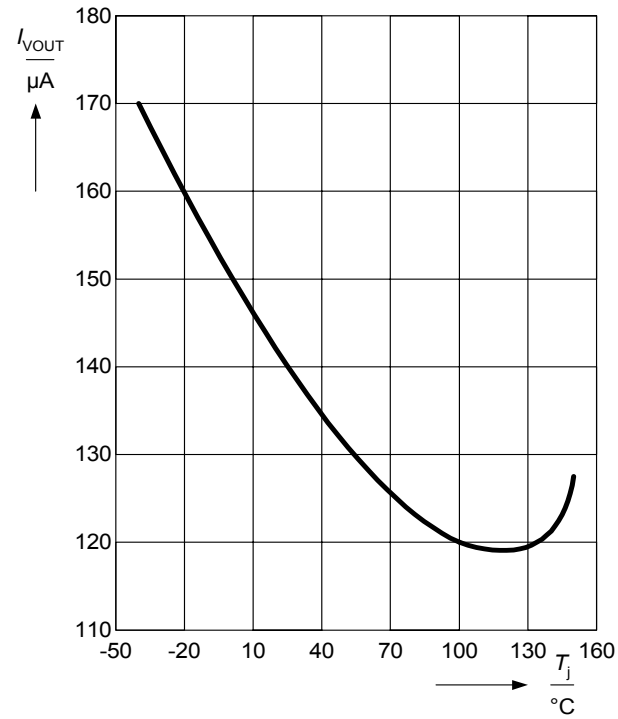
3) For 4V < V_{VS} < 6V: $V_{GDRV} \approx 0V$.

5 Typical Performance Characteristics

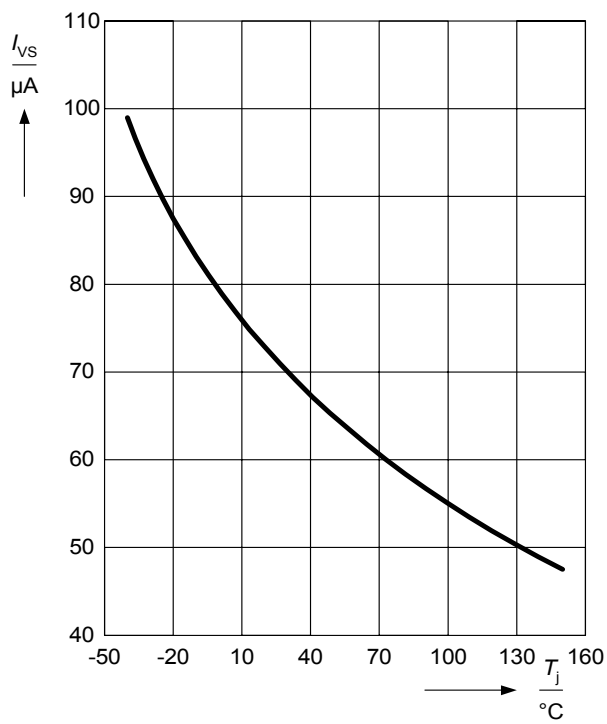
Current consumption I_{VS} vs. temperature T_j at enabled device and V_{VS}=13.5V



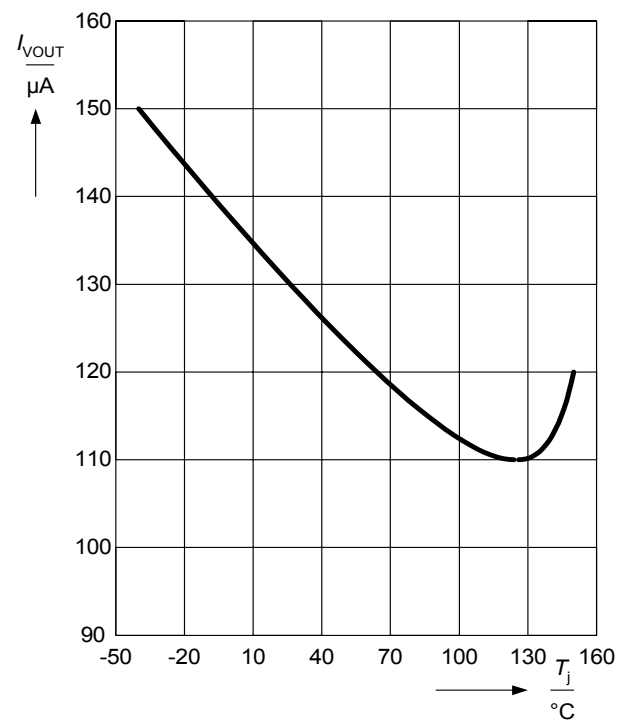
Current consumption I_{VOUT} vs. temperature T_j at enabled device and V_{VOUT}=5.5V



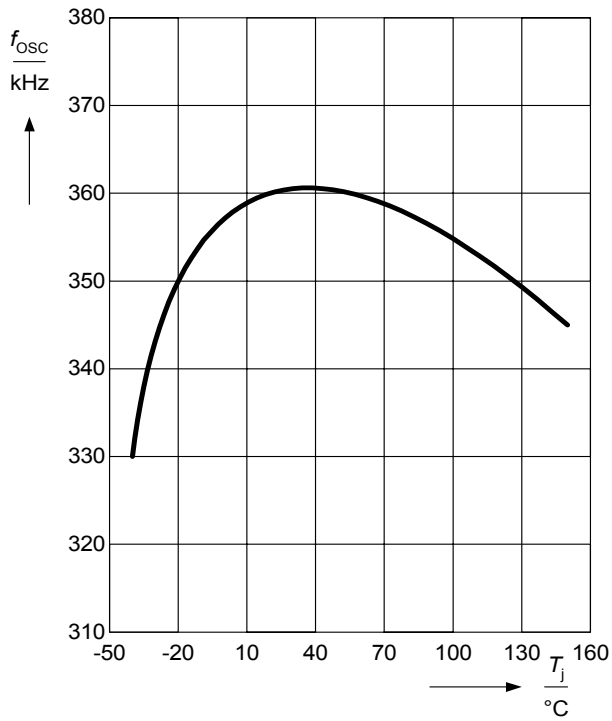
Current consumption I_{VS} vs. temperature T_j at enabled device and V_{VS}=48V



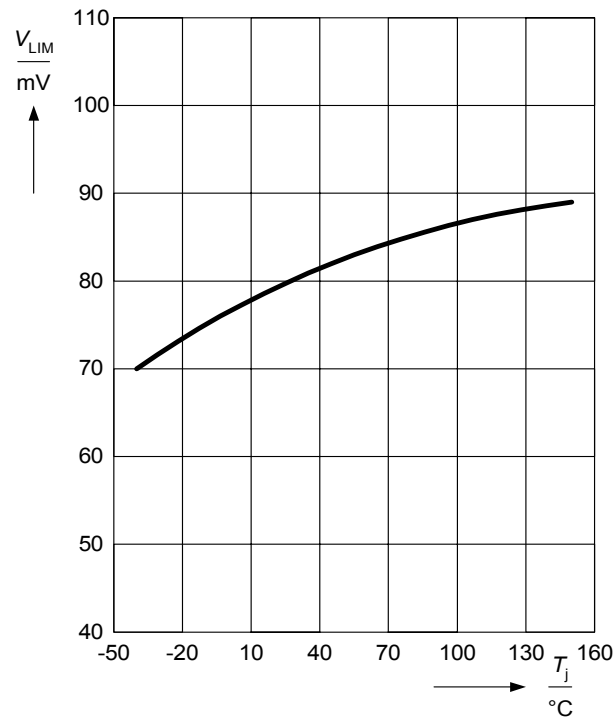
Current consumption I_{VOUT} vs. temperature T_j at enabled device and V_{VOUT}=10V(-2GV)



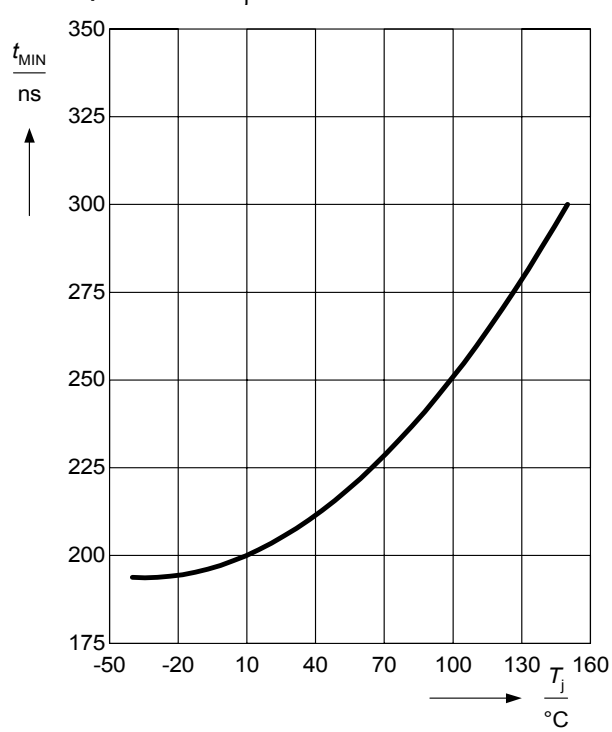
Internal oscillator frequency f_{OSC}
vs. temperature T_j



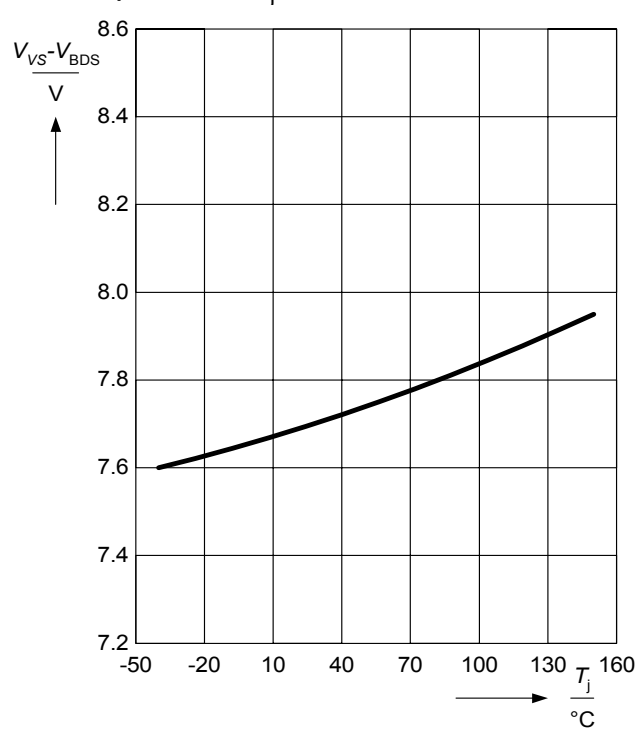
Peak current limit threshold voltage V_{LIM}
vs. temperature T_j



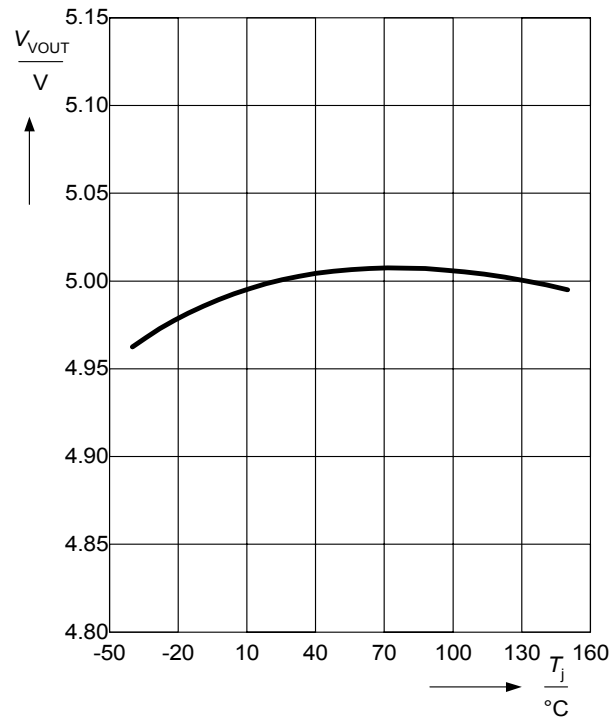
Minimum on time t_{MIN} (blanking)
vs. temperature T_j



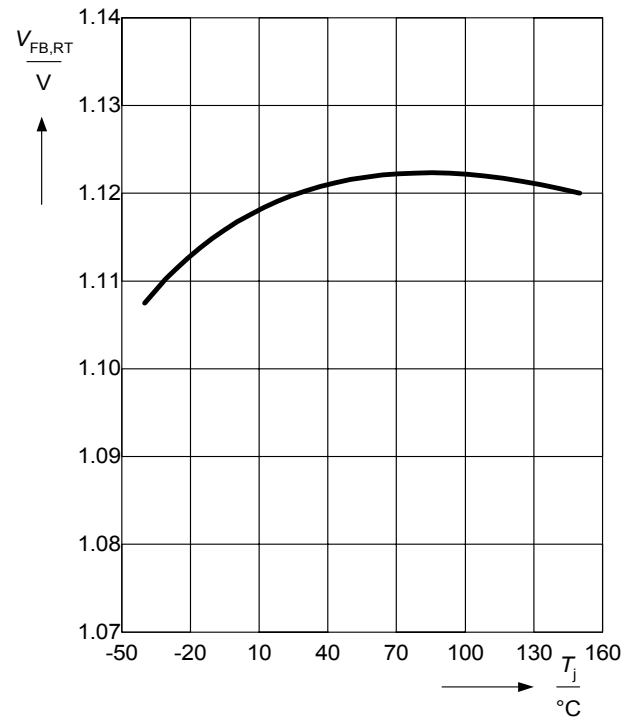
Gate driver supply V_{VS} - V_{BDS}
vs. temperature T_j



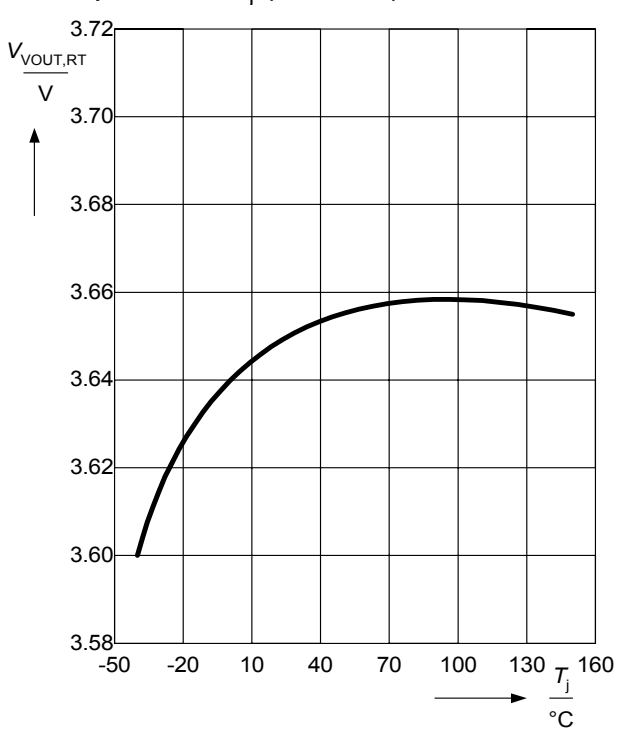
Output voltage V_{VOUT} vs. temperature T_j in PFM mode (V_{VS}=24V,I_{Load}=15mA,-3GV50)



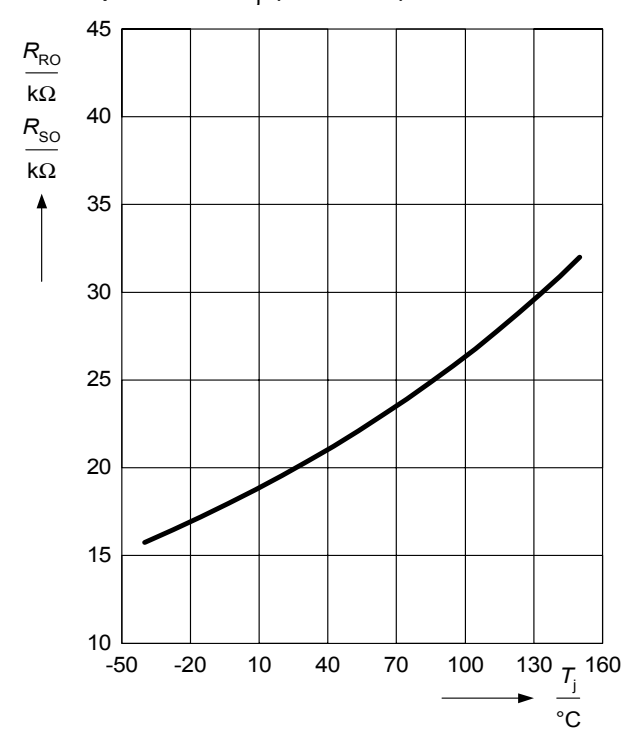
Lower Reset threshold $V_{FB,RT}$ vs. temperature T_j (-2GV)



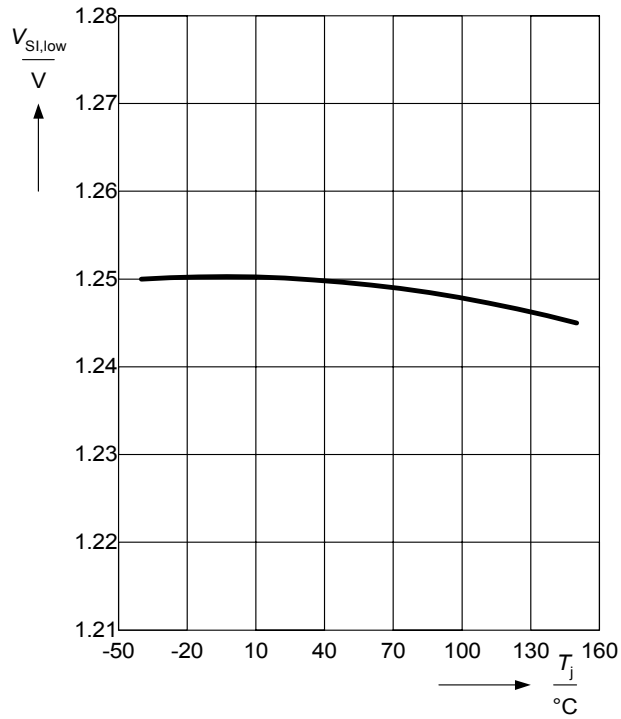
Lower Reset threshold $V_{VOUT, RT}$ vs. temperature T_j (-3GV50)



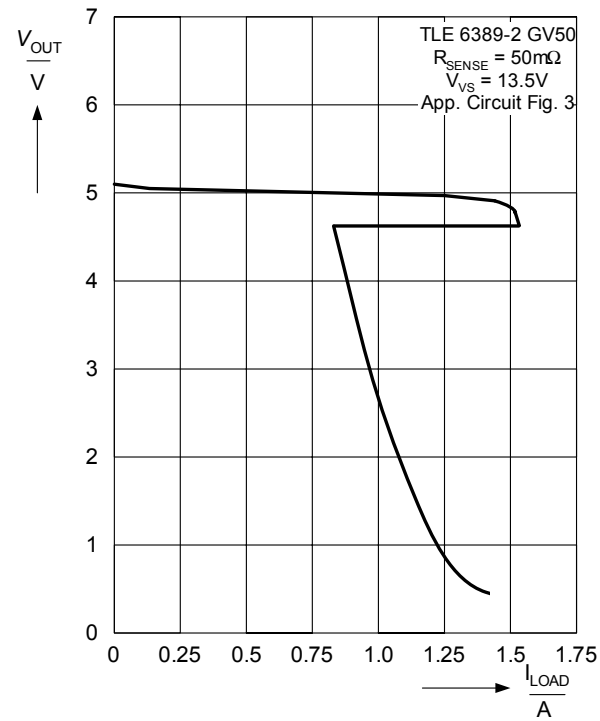
Internal pull up resistors R_{RO} and R_{SO} vs. temperature T_j (-3GV50)



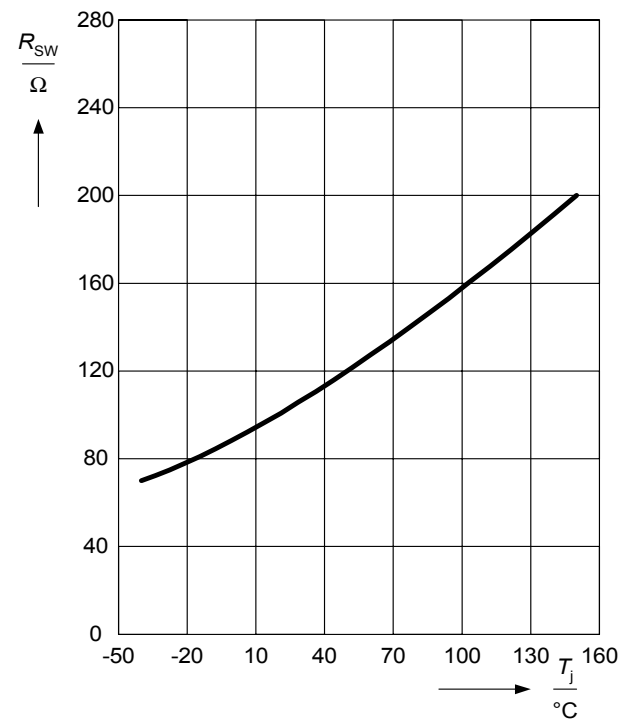
Lower Sense threshold $V_{SI,\ low}$ vs. temperature T_j



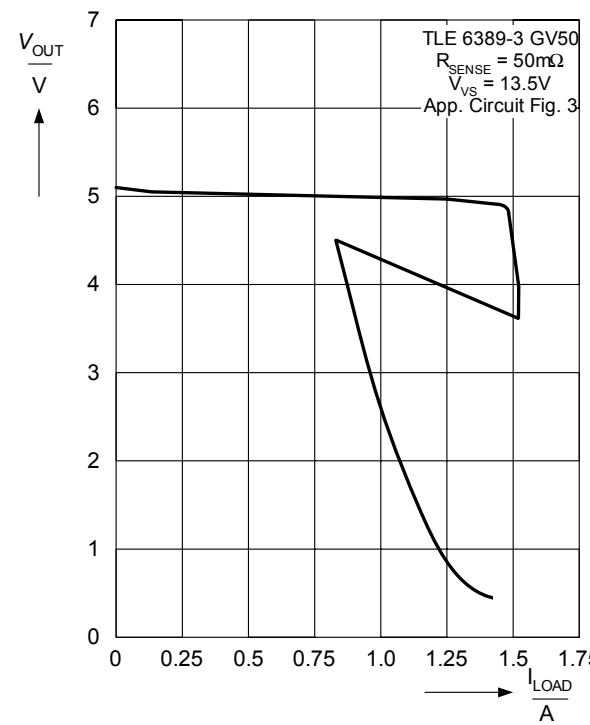
Output Voltage vs. Load Current, TLE6389-2 GV50



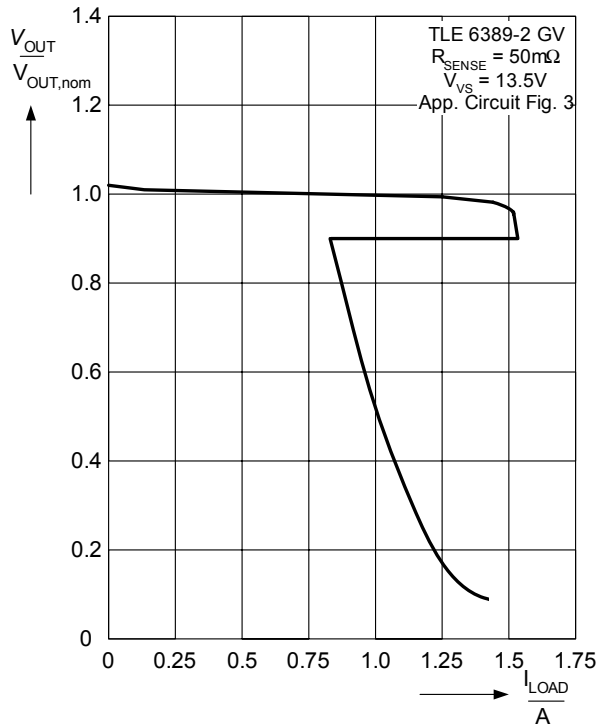
On resistance of SI_GND switch R_{SW} vs. temperature T_j



Output Current vs. Load Current, TLE6389-3 GV50



Output Voltage vs Load Current



6 Detailed circuit description

In the following, some internal blocks of the TLE6389 are described in more detail. For the right choice of the external components please refer to the section application information.

6.1 PFM/PWM Step-down regulator

To meet the strict requirements in terms of current consumption demanded by all Body- and 42V PowerNet applications a special PFM (Pulse Frequency Modulation) - PWM (Pulse Width Modulation) control scheme for highest efficiency is implemented in the TLE 6389 regulators. Under light load conditions the output voltage is able to increase slightly and at a certain threshold the controller jumps into PFM mode. In this PFM operation the PMOS is triggered with a certain on time (depending on input voltage, output voltage, inductance- and sense resistor value) whenever the buck output voltage decreases to the so called WAKE-threshold. The switching frequency of the step down regulator is determined in the PFM mode by the load current. It increases with increasing load current and turns finally to the fixed PWM frequency at a certain load current depending on the input voltage, current sense resistor and inductance. The diagram below shows the buck regulation circuit of the TLE 6389 .

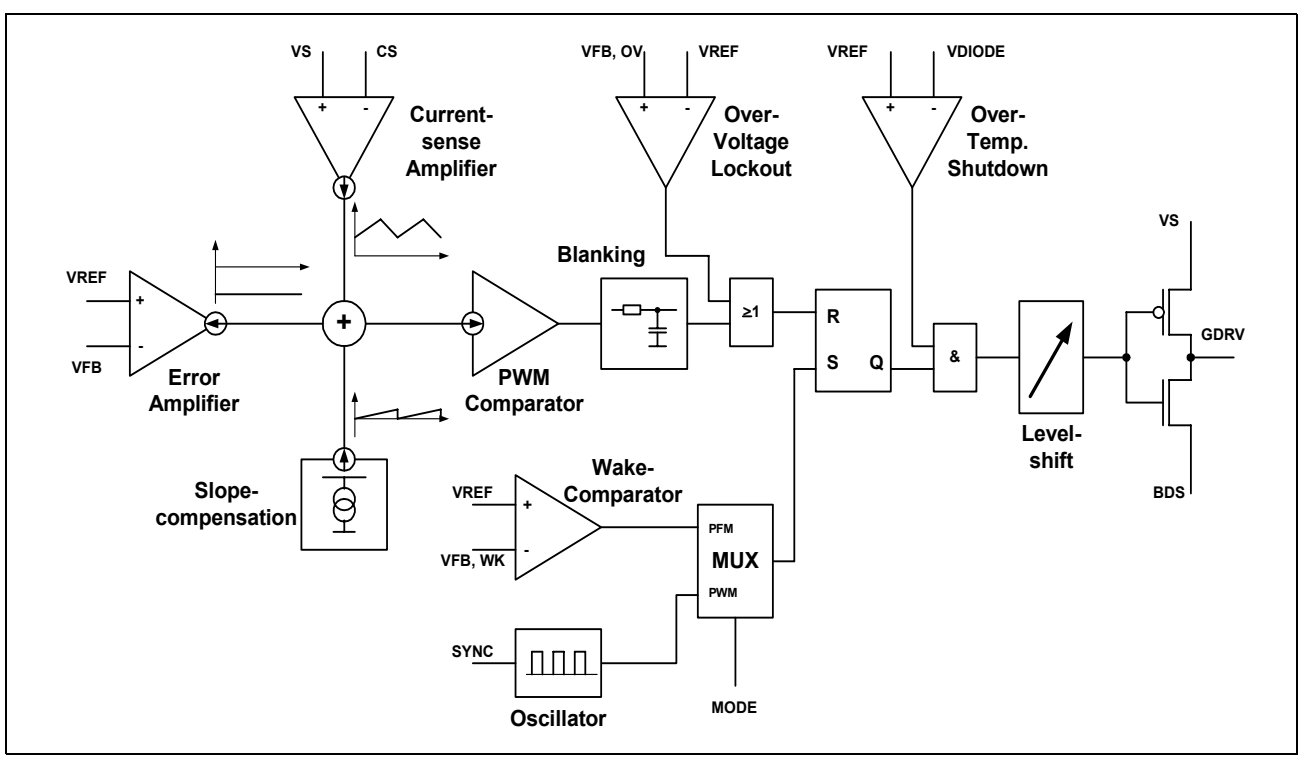


Figure 1 Buck control scheme

The TLE 6389 uses a slope-compensated peak current mode PWM control scheme in which the feedback or output voltage of the step down circuit and the peak current of the current through the PMOS are compared to form the OFF signal for the external PMOS.