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2 x 1W differential input stereo audio amplifier with programmable 3D effects

Features

- Operating range from $V_{CC} = 2.7V$ to $5.5V$
- 1W output power per channel @ $V_{CC} = 5V$, $THD+N = 1\%$, $R_L = 8\Omega$
- Ultra low standby consumption: $10nA$ typ.
- 80dB PSRR @ 217Hz with grounded inputs
- High SNR: 106dB(A) typ.
- Fast startup time: 45ms typ.
- Pop&click-free circuit
- Dedicated standby pin per channel
- Lead-free QFN16 4x4mm package

Applications

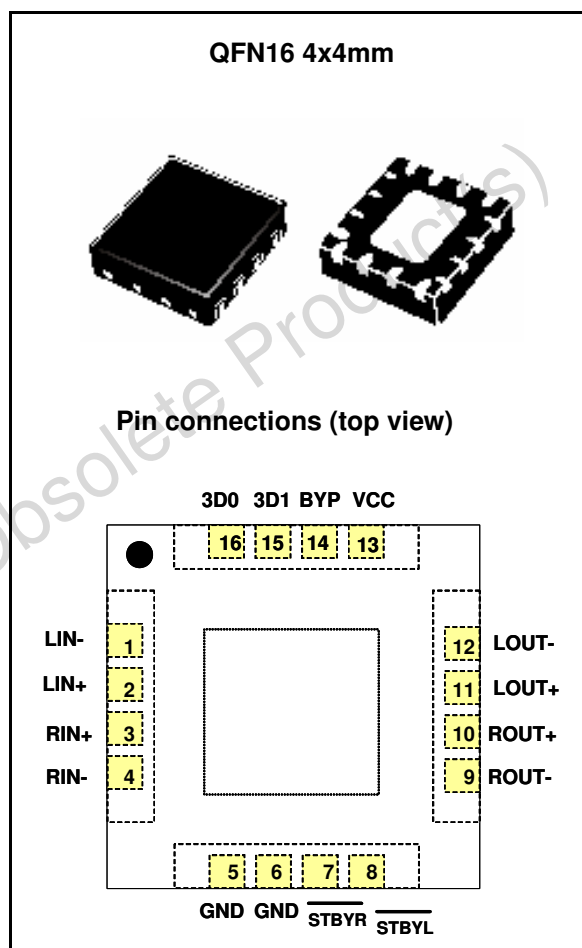
- Cellular mobile phones
- Notebook and PDA computers
- LCD monitors and TVs
- Portable audio devices

Description

The TS4997 is designed for top-class stereo audio applications. Thanks to its compact and power-dissipation efficient QFN16 package with exposed pad, it suits a variety of applications.

With a BTL configuration, this audio power amplifier is capable of delivering 1W per channel of continuous RMS output power into an 8Ω load @ 5V.

3D effects enhancement is programmed through a two digital input pin interface that allows more flexibility on each output audio sound channel.



Each output channel (left and right), also has its own external controlled standby mode pin to reduce the supply current to less than $10nA$ per channel. The device also features an internal thermal shutdown protection.

The gain of each channel can be configured by external gain setting resistors.

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1 Typical application schematics

Figure 1 shows a typical application for the TS4997 with a gain of +6dB set by the input resistors.

Figure 1. Typical application schematics

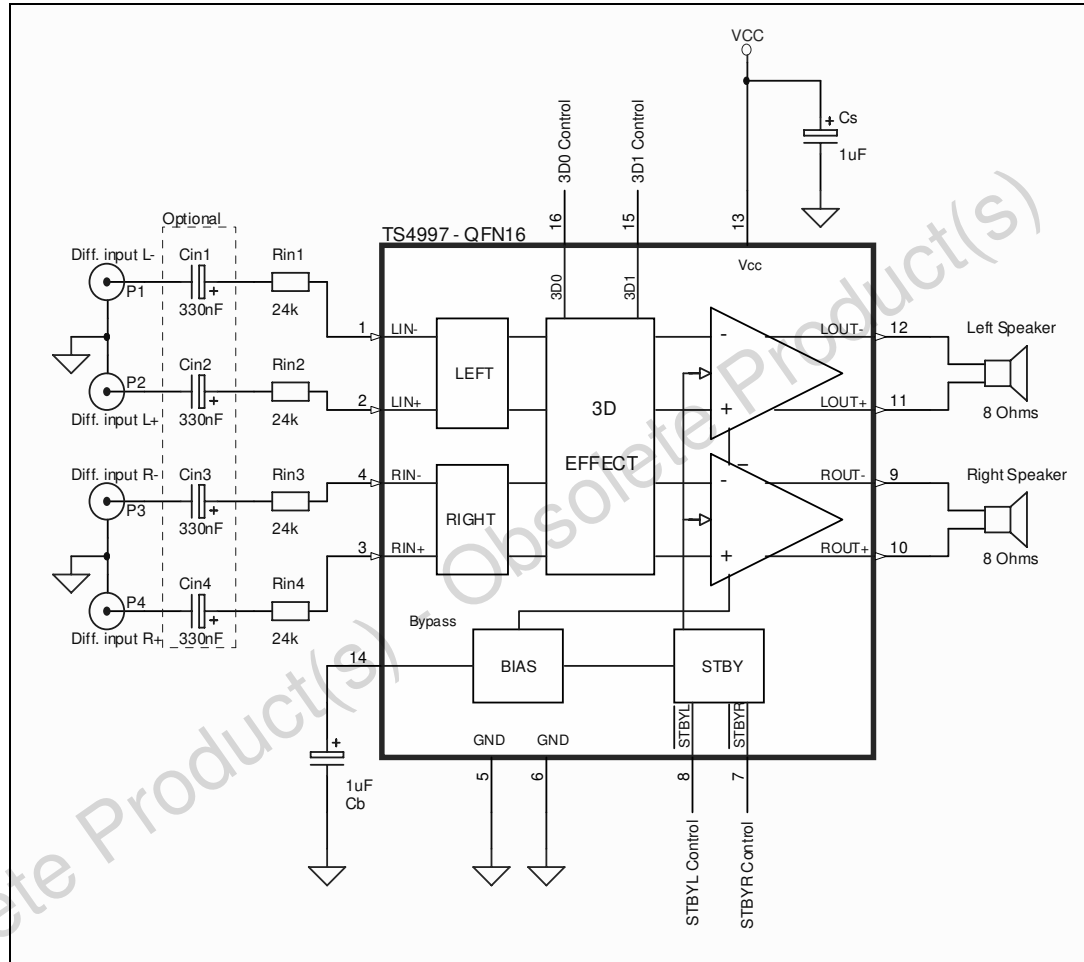


Table 1. External component descriptions

Components	Functional description
R_{IN}	Input resistors that set the closed loop gain in conjunction with a fixed internal feedback resistor ($Gain = R_{feed}/R_{IN}$, where $R_{feed} = 50k\Omega$).
C_{IN}	Input coupling capacitors that block the DC voltage at the amplifier input terminal. Thanks to common mode feedback, these input capacitors are optional. However, if they are added, they form with R_{IN} a 1st order high pass filter with -3dB cut-off frequency ($f_{cut-off} = 1 / (2 \times \pi \times R_{IN} \times C_{IN})$).
C_S	Supply bypass capacitors that provides power supply filtering.
C_B	Bypass pin capacitor that provides half supply filtering.

2 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	6	V
V_i	Input voltage ⁽²⁾	GND to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient	120	°C/W
P_d	Power dissipation	Internally limited	
ESD	Human body model ⁽³⁾ Digital pins STBYL, STBYR, 3D0, 3D1	2	kV
		1.5	
ESD	Machine model	200	V
	Latch-up immunity	200	mA

1. All voltage values are measured with respect to the ground pin.
2. The magnitude of the input signal must never exceed $V_{CC} + 0.3V$ / GND - 0.3V.
3. All voltage values are measured from each pin with respect to supplies.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 5.5	V
V_{ICM}	Common mode input voltage range	GND to $V_{CC} - 1V$	V
V_{IL}	3D0 - 3D1 maximum low input voltage	0.4	V
V_{IH}	3D0 - 3D1 minimum high input voltage	1.3	V
V_{STBY}	Standby voltage input:	$1.3 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$	V
	Device ON		
	Device OFF		
R_L	Load resistor	≥ 4	Ω
R_{OUT}/GND	Output resistor to GND ($V_{STBY} = GND$)	≥ 1	M Ω
TSD	Thermal shutdown temperature	150	°C
R_{thja}	Thermal resistance junction to ambient	QFN16 ⁽¹⁾	°C/W
		QFN16 ⁽²⁾	

1. When mounted on a 4-layer PCB with vias.
2. When mounted on a 2-layer PCB with vias.

3 Electrical characteristics

Table 4. $V_{CC} = +5V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load, left and right channel active		7.4	9.6	mA
I_{STBY}	Standby current ⁽¹⁾ No input signal, $V_{STBYL} = GND$, $V_{STBYR} = GND$, $R_L = 8\Omega$		10	2000	nA
V_{oo}	Output offset voltage No input signal, $R_L = 8\Omega$		1	35	mV
P_o	Output power THD = 1% Max, $F = 1kHz$, $R_L = 8\Omega$	800	1000		mW
THD + N	Total harmonic distortion + noise $P_o = 700mW_{rms}$, $G = 6dB$, $R_L = 8\Omega$, $20Hz \leq F \leq 20kHz$		0.5		%
PSRR	Power supply rejection ratio ⁽²⁾ , inputs grounded $R_L = 8\Omega$, $G = 6dB$, $C_b = 1\mu F$, $V_{ripple} = 200mV_{pp}$, 3D effect off $F = 217Hz$ $F = 1kHz$		80 75		dB
CMRR	Common mode rejection ratio ⁽³⁾ $R_L = 8\Omega$, $G = 6dB$, $C_b = 1\mu F$, $V_{incm} = 200mV_{pp}$, 3D effect off $F = 217Hz$ $F = 1kHz$		57 57		dB
SNR	Signal-to-noise ratio A-weighted, $G = 6dB$, $C_b = 1\mu F$, $R_L = 8\Omega$, 3D effect off (THD + N $\leq 0.5\%$, $20Hz < F < 20kHz$)		108		dB
Crosstalk	Channel separation, $R_L = 8\Omega$, $G = 6dB$, 3D effect off $F = 1kHz$ $F = 20Hz$ to $20kHz$		105 80		dB
V_N	Output voltage noise, $F = 20Hz$ to $20kHz$, $R_L = 8\Omega$, $G=6dB$ $C_b = 1\mu F$, 3D effect off Unweighted A-weighted		15 10		μV_{rms}
Gain	Gain value (R_{IN} in $k\Omega$)	$\frac{40k\Omega}{R_{IN}}$	$\frac{50k\Omega}{R_{IN}}$	$\frac{60k\Omega}{R_{IN}}$	V/V
t_{WU}	Wake-up time ($C_b = 1\mu F$)		46		ms
t_{STBY}	Standby time ($C_b = 1\mu F$)		10		μs
Φ_M	Phase margin at unity gain $R_L = 8\Omega$, $C_L = 500pF$		65		Degrees
GM	Gain margin, $R_L = 8\Omega$, $C_L = 500pF$		15		dB
GBP	Gain bandwidth product, $R_L = 8\Omega$		1.5		MHz

1. Standby mode is active when V_{STBY} is tied to GND.

2. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. V_{ripple} is the sinusoidal signal superimposed upon V_{CC} .

3. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{incm}))$.

Table 5. $V_{CC} = +3.3V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load, left and right channel active		6.6	8.6	mA
I_{STBY}	Standby current ⁽¹⁾ No input signal, $V_{STBYL} = GND$, $V_{STBYR} = GND$, $R_L = 8\Omega$		10	2000	nA
V_{oo}	Output offset voltage No input signal, $R_L = 8\Omega$		1	35	mV
P_o	Output power THD = 1% Max, $F = 1kHz$, $R_L = 8\Omega$	370	460		mW
THD + N	Total harmonic distortion + noise $P_o = 300mW_{rms}$, $G = 6dB$, $R_L = 8\Omega$, $20Hz \leq F \leq 20kHz$		0.5		%
PSRR	Power supply rejection ratio ⁽²⁾ , inputs grounded $R_L = 8\Omega$, $G = 6dB$, $C_b = 1\mu F$, $V_{ripple} = 200mV_{pp}$, 3D effect off $F = 217Hz$ $F = 1kHz$		80 75		dB
CMRR	Common mode rejection ratio ⁽³⁾ $R_L = 8\Omega$, $G = 6dB$, $C_b = 1\mu F$, $V_{incom} = 200mV_{pp}$, 3D effect off $F = 217Hz$ $F = 1kHz$		57 57		dB
SNR	Signal-to-noise ratio A-weighted, $G = 6dB$, $C_b = 1\mu F$, $R_L = 8\Omega$, 3D effect off (THD + N $\leq 0.5\%$, $20Hz < F < 20kHz$)		104		dB
Crosstalk	Channel separation, $R_L = 8\Omega$, $G = 6dB$, 3D effect off $F = 1kHz$ $F = 20Hz$ to $20kHz$		105 80		dB
V_N	Output voltage noise, $F = 20Hz$ to $20kHz$, $R_L = 8\Omega$, $G = 6dB$ $C_b = 1\mu F$, 3D effect off Unweighted A-weighted		15 10		μV_{rms}
Gain	Gain value (R_{IN} in $k\Omega$)	$\frac{40k\Omega}{R_{IN}}$	$\frac{50k\Omega}{R_{IN}}$	$\frac{60k\Omega}{R_{IN}}$	V/V
t_{WU}	Wake-up time ($C_b = 1\mu F$)		47		ms
t_{STBY}	Standby time ($C_b = 1\mu F$)		10		μs
Φ_M	Phase margin at unity gain $R_L = 8\Omega$, $C_L = 500pF$		65		Degrees
GM	Gain margin $R_L = 8\Omega$, $C_L = 500pF$		15		dB
GBP	Gain bandwidth product $R_L = 8\Omega$		1.5		MHz

1. Standby mode is active when V_{STBY} is tied to GND.

2. Dynamic measurements - $20 \cdot \log(\frac{rms(V_{out})}{rms(V_{ripple})})$. V_{ripple} is the sinusoidal signal superimposed upon V_{CC} .

3. Dynamic measurements - $20 \cdot \log(\frac{rms(V_{out})}{rms(V_{incom})})$.

Table 6. $V_{CC} = +2.7V$, $GND = 0V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load, left and right channel active		6.2	8.1	mA
I_{STBY}	Standby current ⁽¹⁾ No input signal, $V_{STBYL} = GND$, $V_{STBYR} = GND$, $R_L = 8\Omega$		10	2000	nA
V_{oo}	Output offset voltage No input signal, $R_L = 8\Omega$		1	35	mV
P_o	Output power THD = 1% Max, $F = 1kHz$, $R_L = 8\Omega$	220	295		mW
THD + N	Total harmonic distortion + noise $P_o = 200mW_{rms}$, $G = 6dB$, $R_L = 8\Omega$, $20Hz \leq F \leq 20kHz$		0.5		%
PSRR	Power supply rejection ratio ⁽²⁾ , inputs grounded $R_L = 8\Omega$, $G = 6dB$, $C_b = 1\mu F$, $V_{ripple} = 200mV_{pp}$, 3D effect off $F = 217Hz$ $F = 1kHz$		76 73		dB
CMRR	Common mode rejection ratio ⁽³⁾ $R_L = 8\Omega$, $G = 6dB$, $C_b = 1\mu F$, $V_{incom} = 200mV_{pp}$, 3D effect off $F = 217Hz$ $F = 1kHz$		57 57		dB
SNR	Signal-to-noise ratio A-weighted, $G = 6dB$, $C_b = 1\mu F$, $R_L = 8\Omega$, 3D effect off (THD + N $\leq 0.5\%$, $20Hz < F < 20kHz$)		102		dB
Crosstalk	Channel separation, $R_L = 8\Omega$, $G = 6dB$, 3D effect off $F = 1kHz$ $F = 20Hz$ to $20kHz$		105 80		dB
V_N	Output voltage noise, $F = 20Hz$ to $20kHz$, $R_L = 8\Omega$, $G = 6dB$ $C_b = 1\mu F$, 3D effect off Unweighted A-weighted		15 10		μV_{rms}
Gain	Gain value (R_{IN} in $k\Omega$)	$\frac{40k\Omega}{R_{IN}}$	$\frac{50k\Omega}{R_{IN}}$	$\frac{60k\Omega}{R_{IN}}$	V/V
t_{WU}	Wake-up time ($C_b = 1\mu F$)		46		ms
t_{STBY}	Standby time ($C_b = 1\mu F$)		10		μs
Φ_M	Phase margin at unity gain $R_L = 8\Omega$, $C_L = 500pF$		65		Degrees
GM	Gain margin $R_L = 8\Omega$, $C_L = 500pF$		15		dB
GBP	Gain bandwidth product $R_L = 8\Omega$		1.5		MHz

1. Standby mode is active when V_{STBY} is tied to GND.

2. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. V_{ripple} is the sinusoidal signal superimposed upon V_{CC} .

3. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{incom}))$.

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Figure 2. THD+N vs. output power

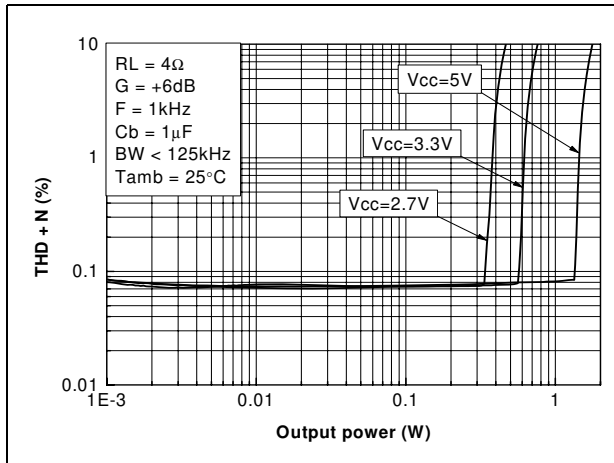


Figure 3. THD+N vs. output power

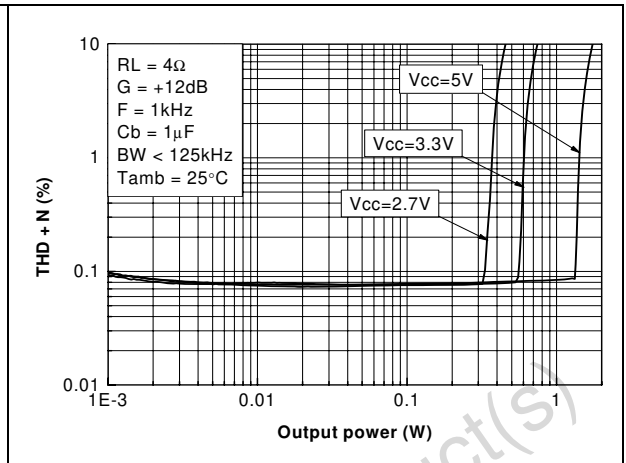


Figure 4. THD+N vs. output power

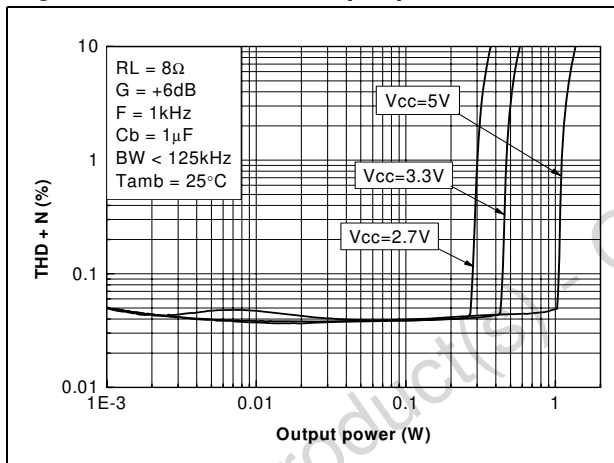


Figure 5. THD+N vs. output power

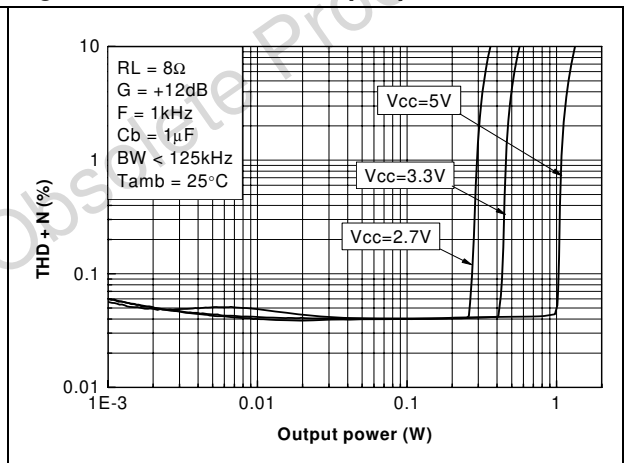


Figure 6. THD+N vs. output power

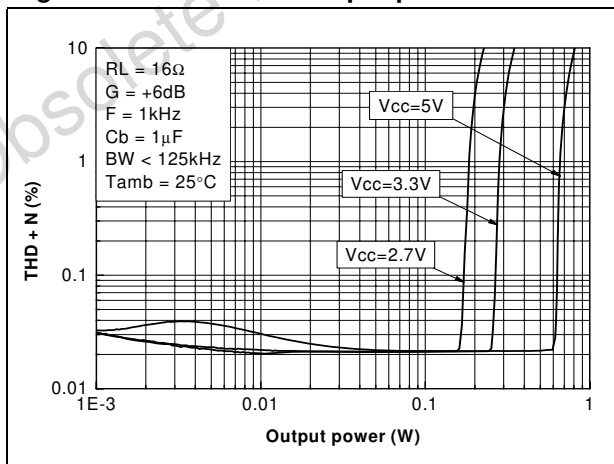


Figure 7. THD+N vs. output power

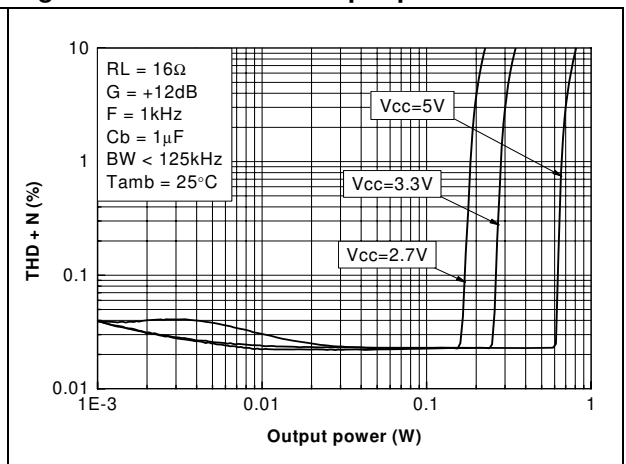


Figure 8. THD+N vs. output power

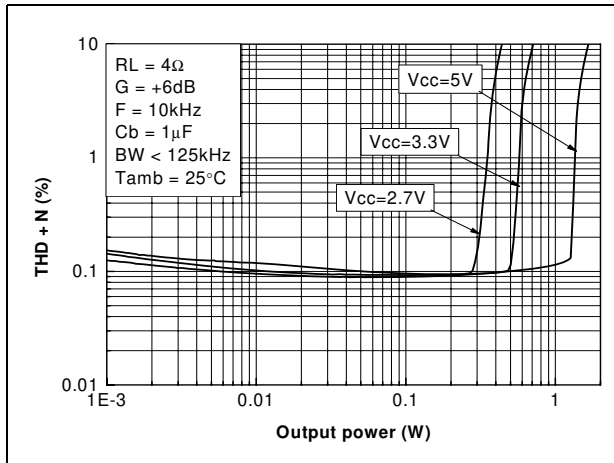


Figure 9. THD+N vs. output power

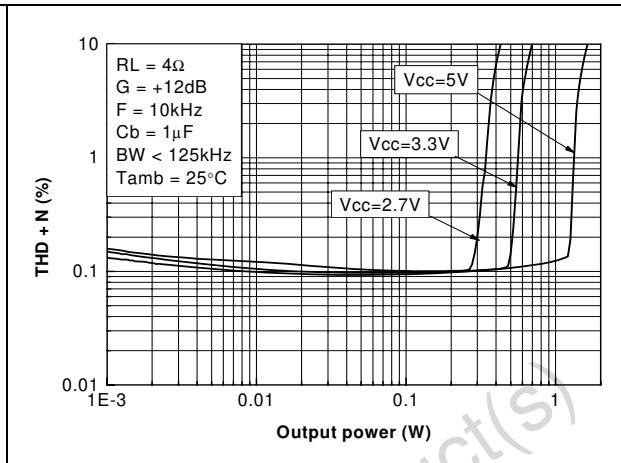


Figure 10. THD+N vs. output power

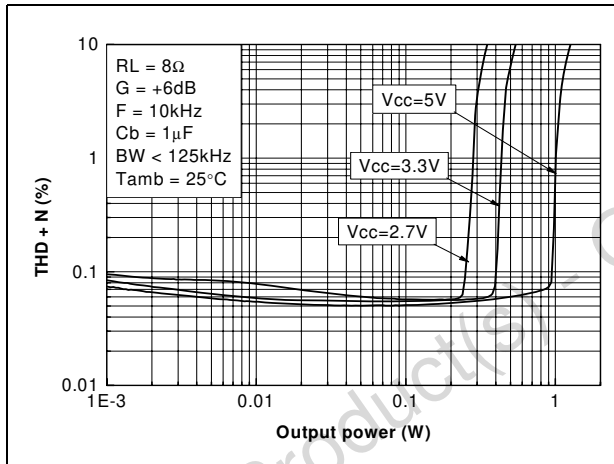


Figure 11. THD+N vs. output power

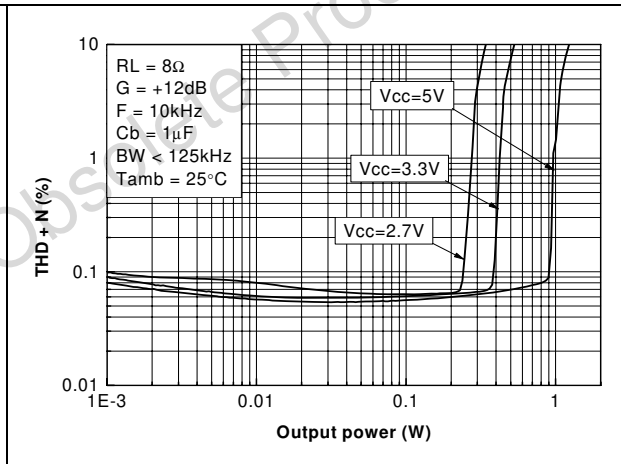


Figure 12. THD+N vs. output power

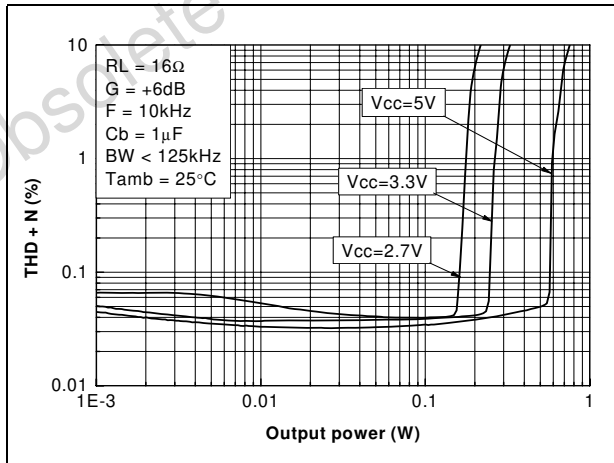


Figure 13. THD+N vs. output power

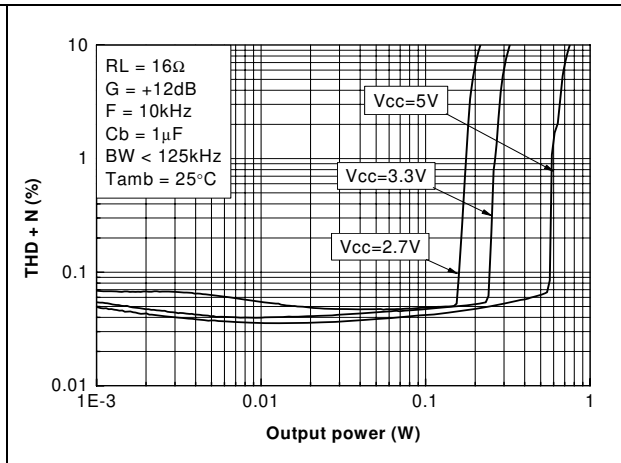


Figure 14. THD+N vs. frequency

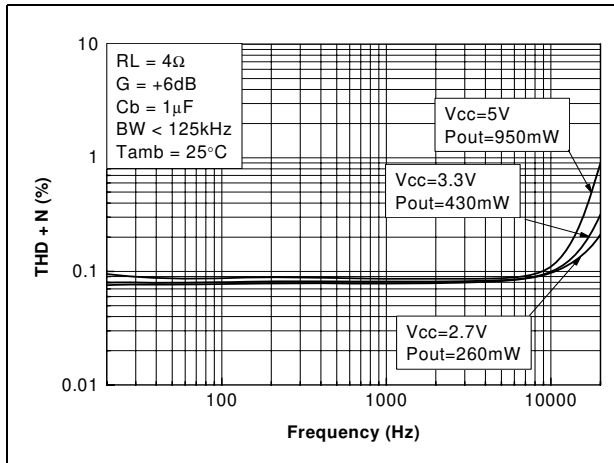


Figure 15. THD+N vs. frequency

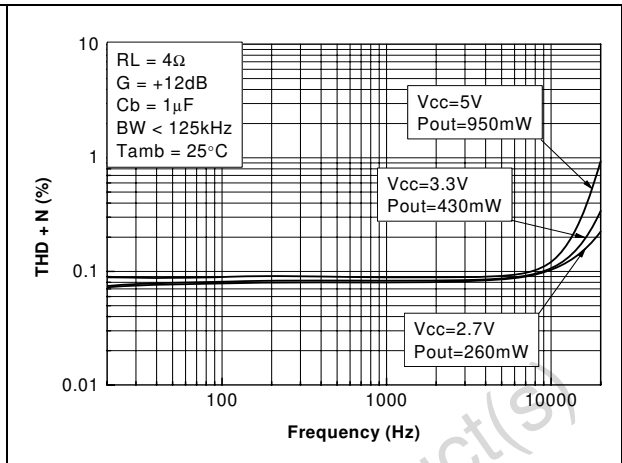


Figure 16. THD+N vs. frequency

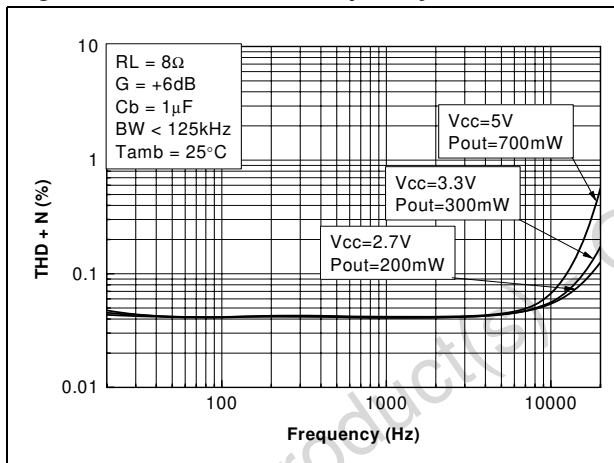


Figure 17. THD+N vs. frequency

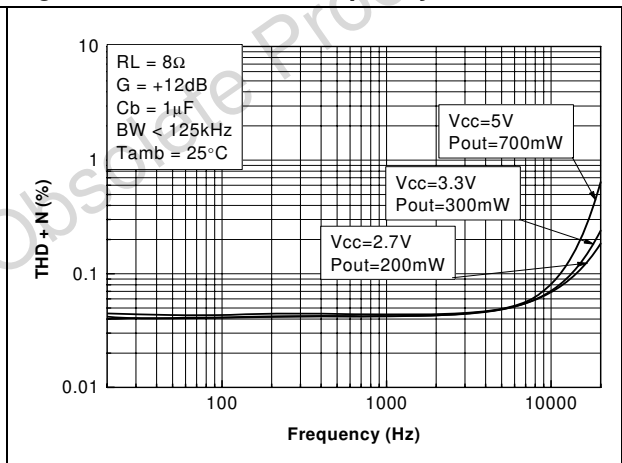


Figure 18. THD+N vs. frequency

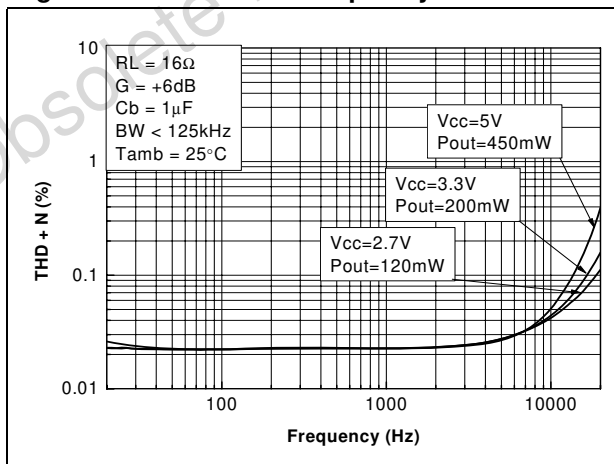


Figure 19. THD+N vs. frequency

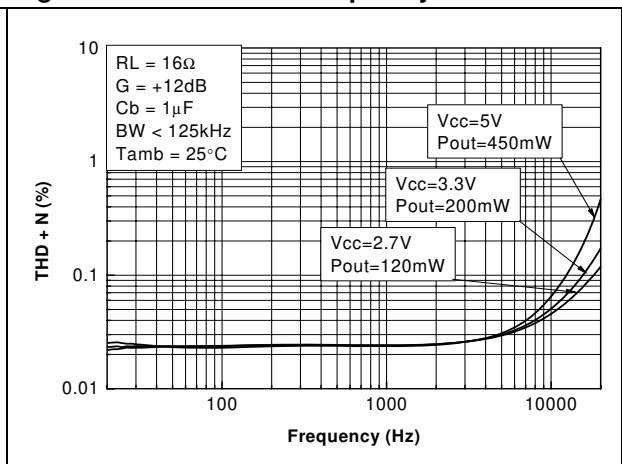


Figure 20. PSRR vs. frequency

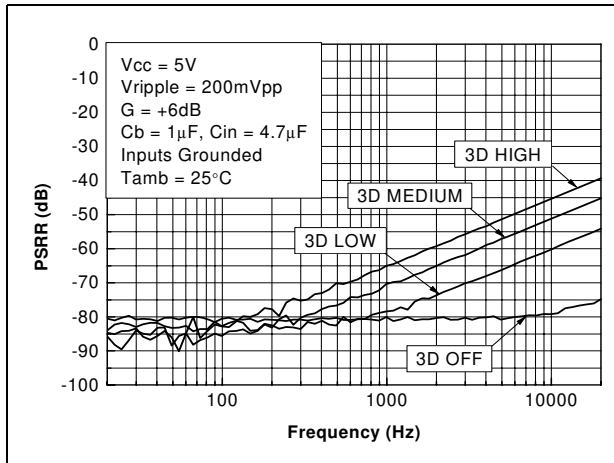


Figure 21. PSRR vs. frequency

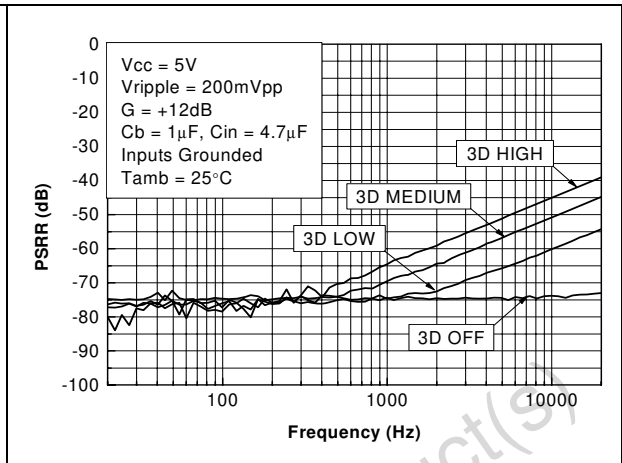


Figure 22. PSRR vs. frequency

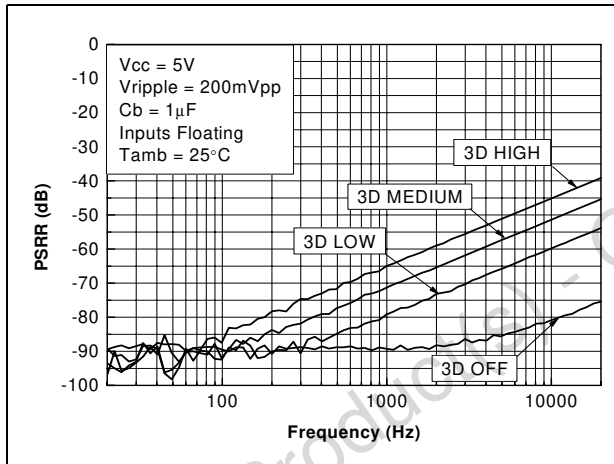


Figure 23. PSRR vs. frequency

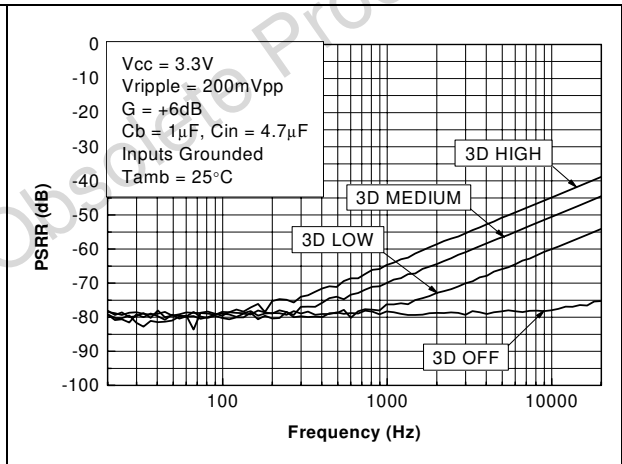


Figure 24. PSRR vs. frequency

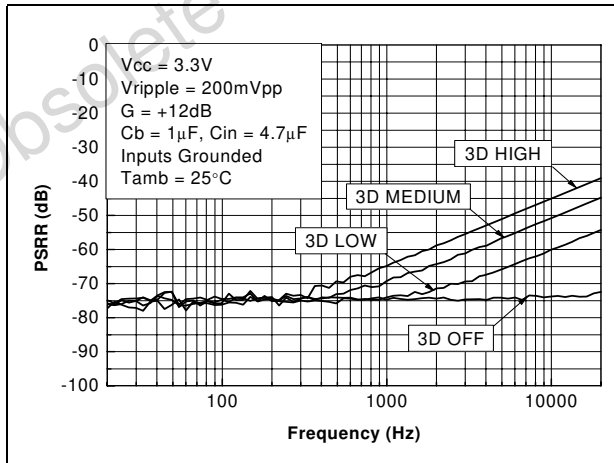


Figure 25. PSRR vs. frequency

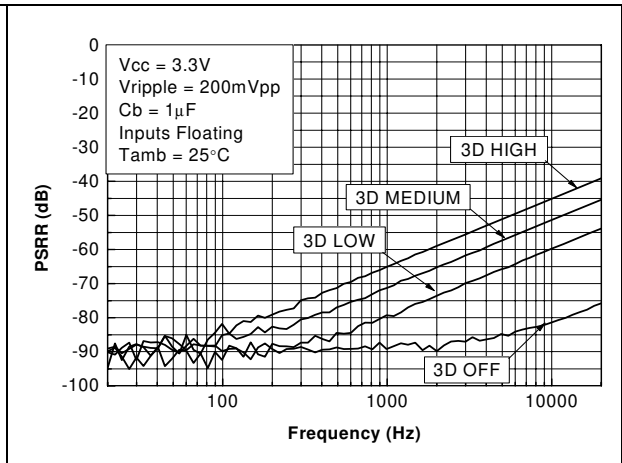


Figure 26. PSRR vs. frequency

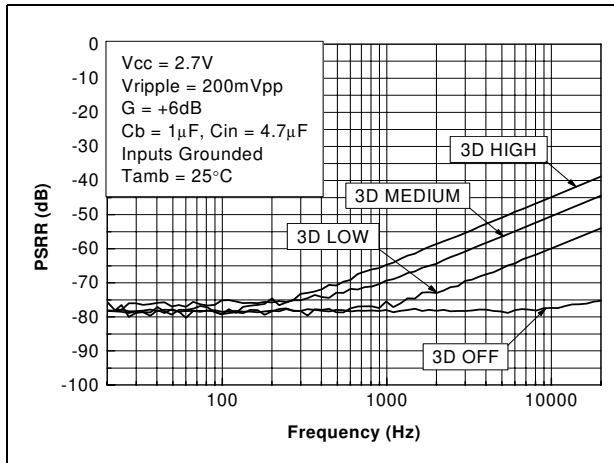


Figure 27. PSRR vs. frequency

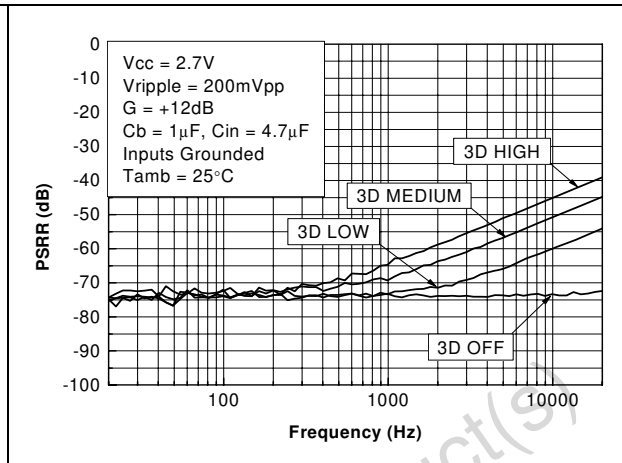


Figure 28. PSRR vs. frequency

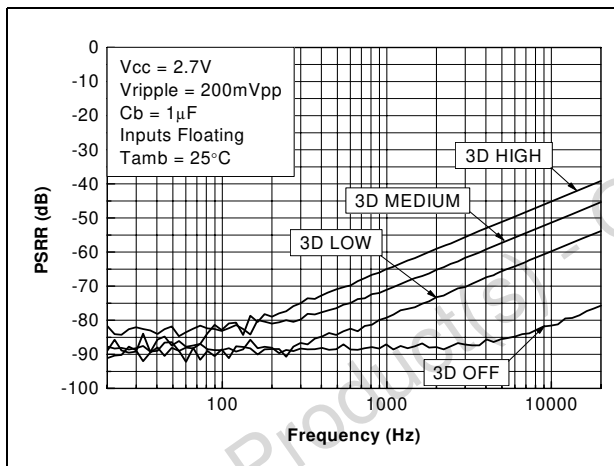


Figure 29. PSRR vs. common mode input voltage

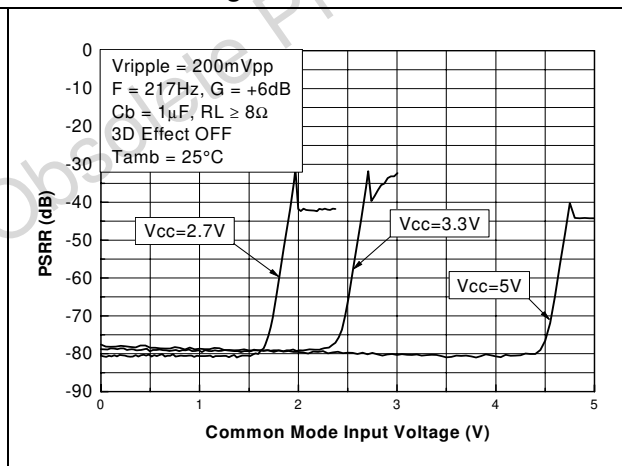


Figure 30. CMRR vs. frequency

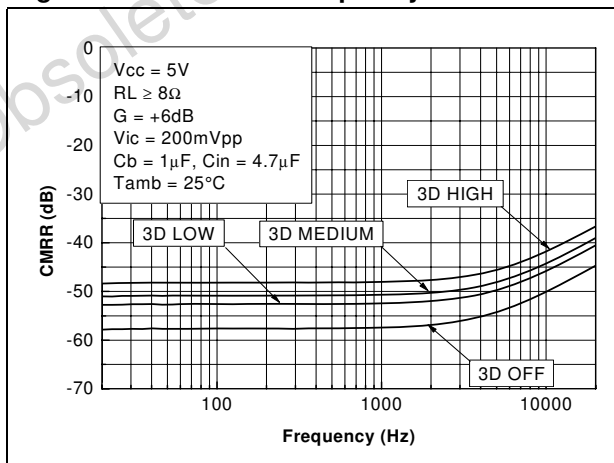


Figure 31. CMRR vs. frequency

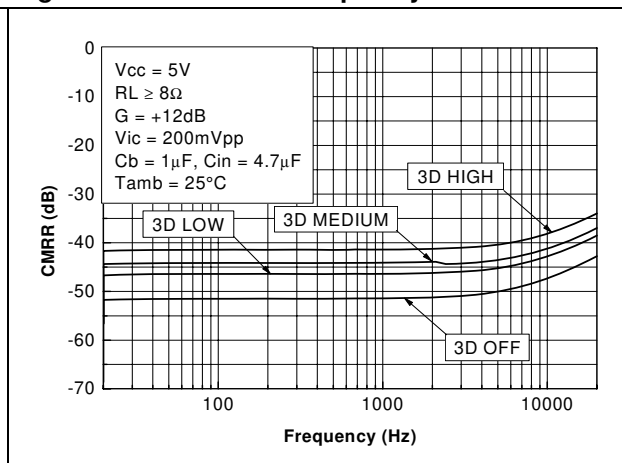


Figure 32. CMRR vs. frequency

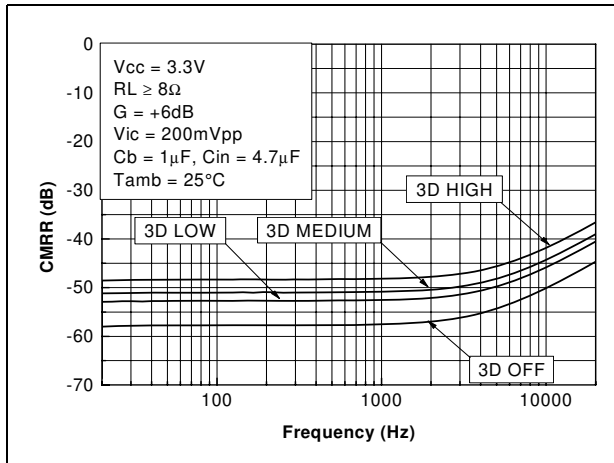


Figure 33. CMRR vs. frequency

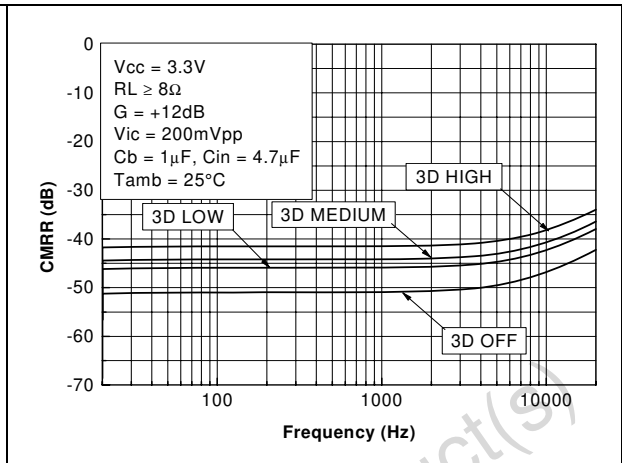


Figure 34. CMRR vs. frequency

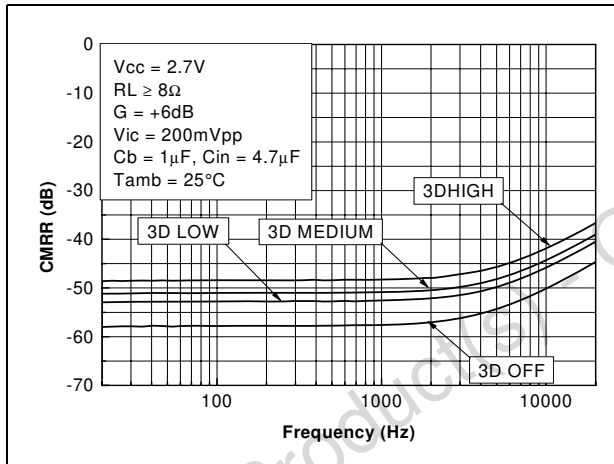


Figure 35. CMRR vs. frequency

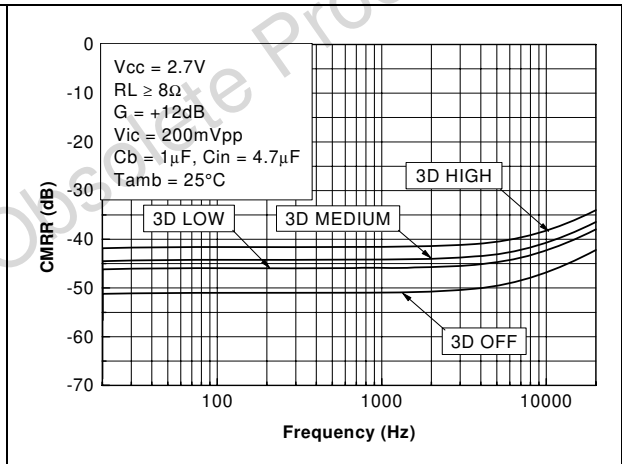


Figure 36. CMRR vs. common mode input voltage

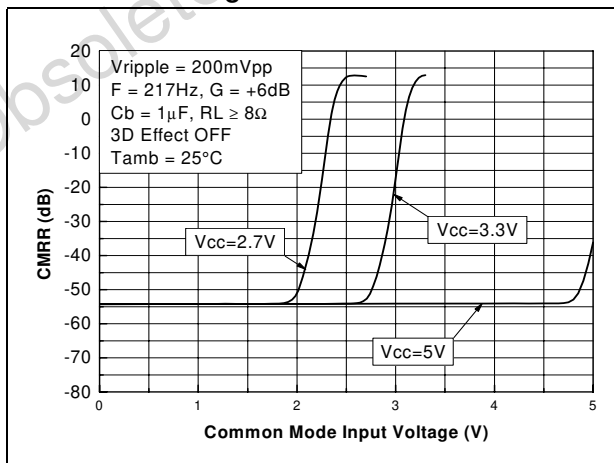


Figure 37. Crosstalk vs. frequency

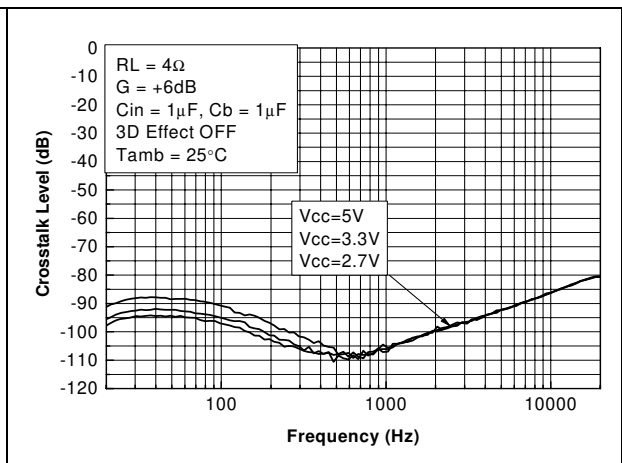


Figure 38. Crosstalk vs. frequency

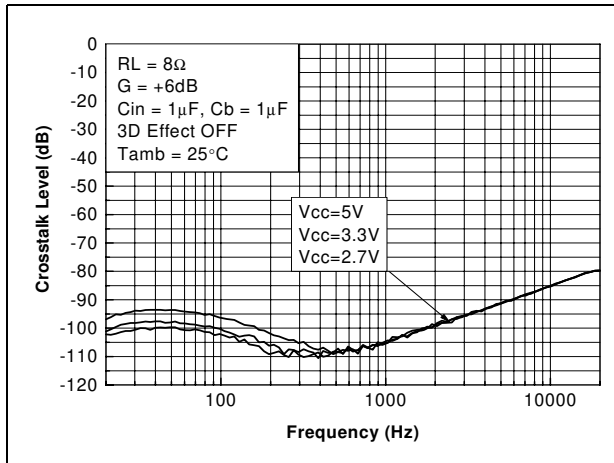


Figure 39. Crosstalk vs. frequency

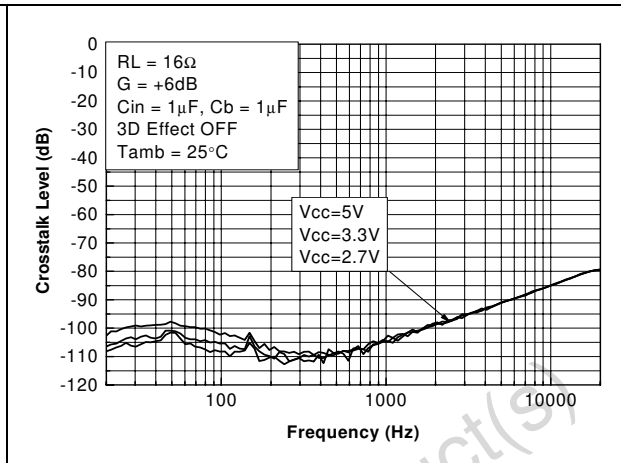


Figure 40. SNR vs. power supply voltage

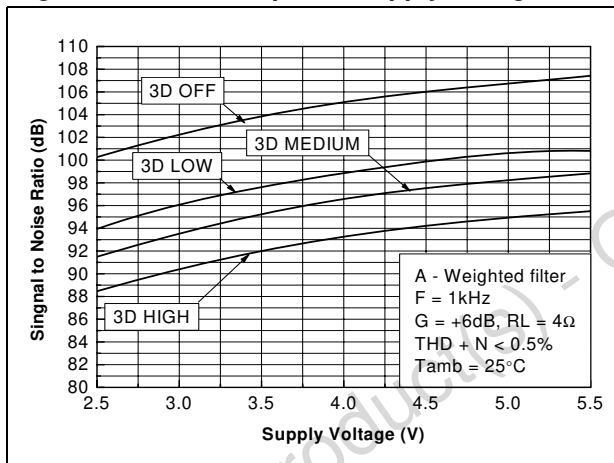


Figure 41. SNR vs. power supply voltage

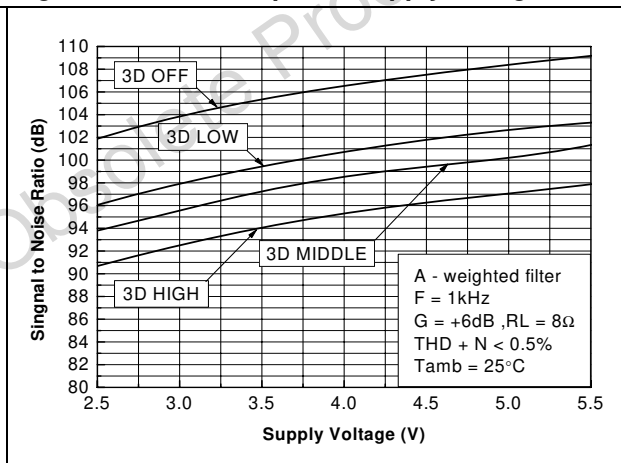


Figure 42. SNR vs. power supply voltage

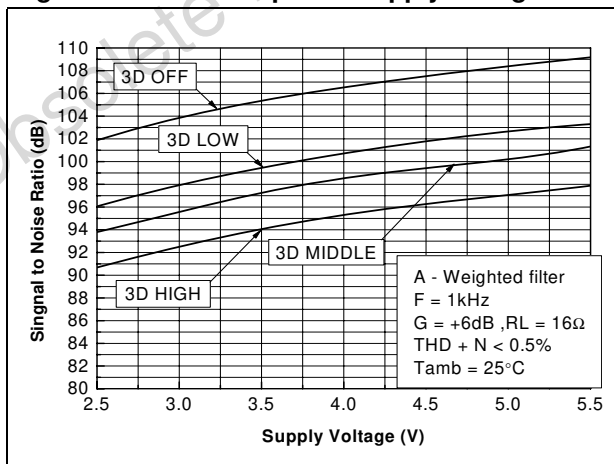


Figure 43. SNR vs. power supply voltage

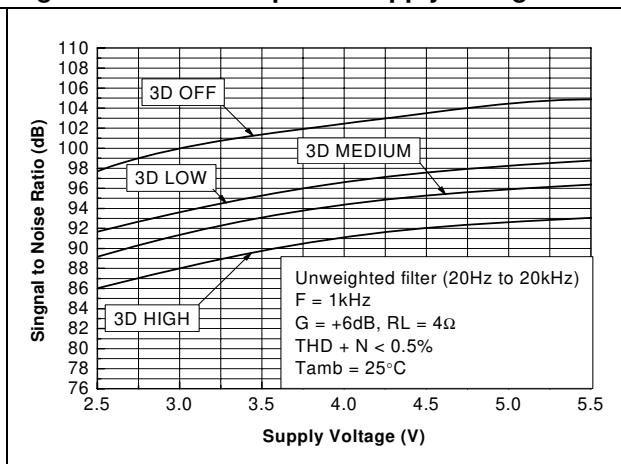


Figure 44. SNR vs. power supply voltage

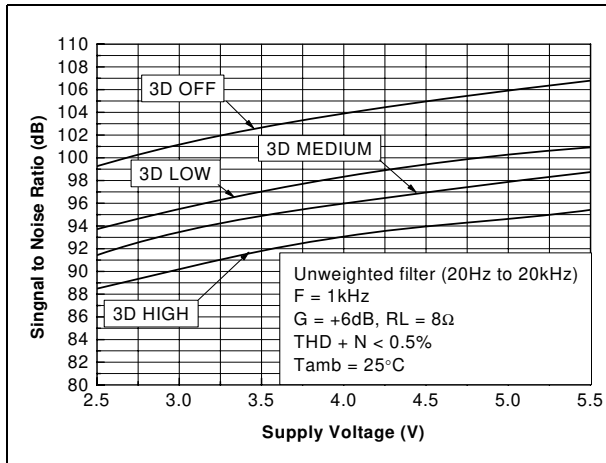


Figure 45. SNR vs. power supply voltage

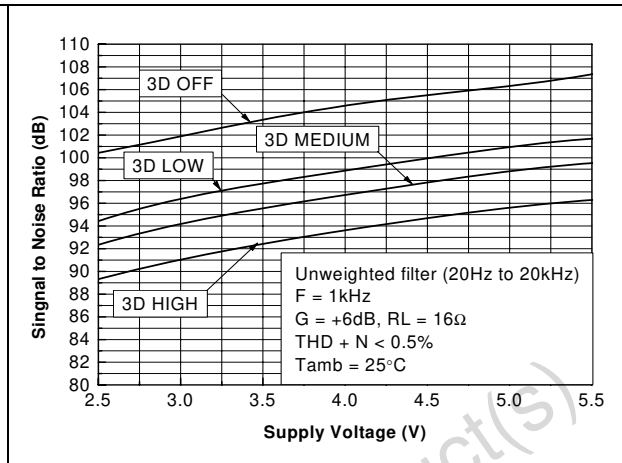


Figure 46. Differential DC output voltage vs. common mode input voltage

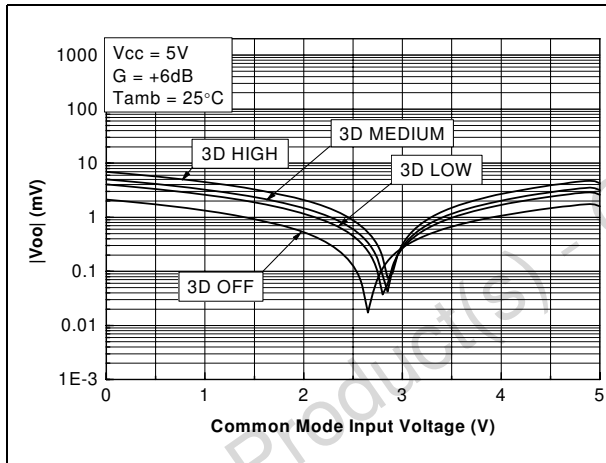


Figure 47. Differential DC output voltage vs. common mode input voltage

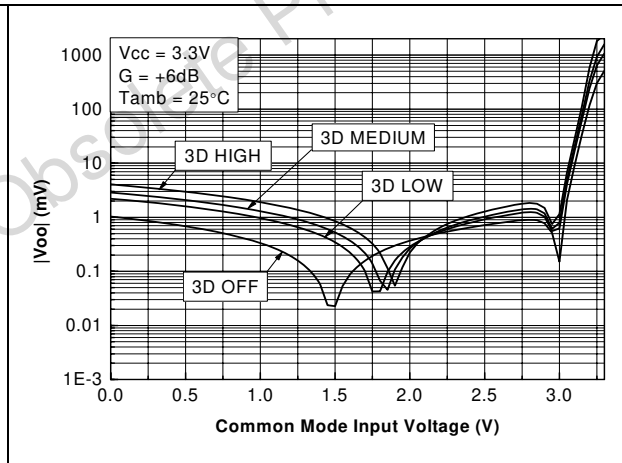


Figure 48. Differential DC output voltage vs. common mode input voltage

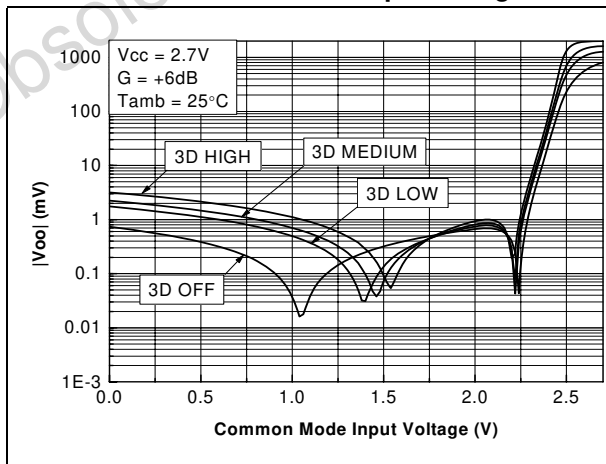


Figure 49. Current consumption vs. power supply voltage

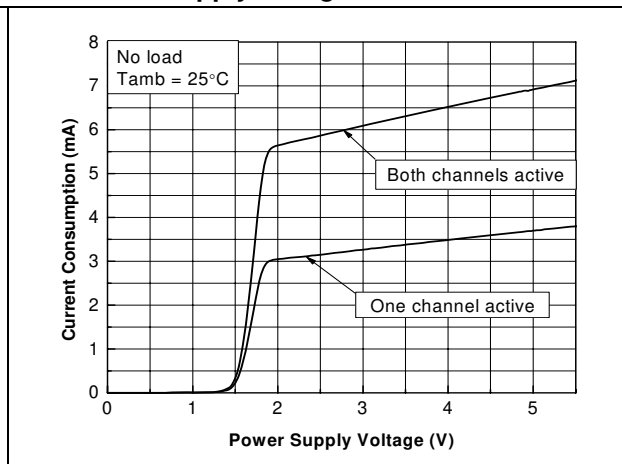


Figure 50. Current consumption vs. standby voltage

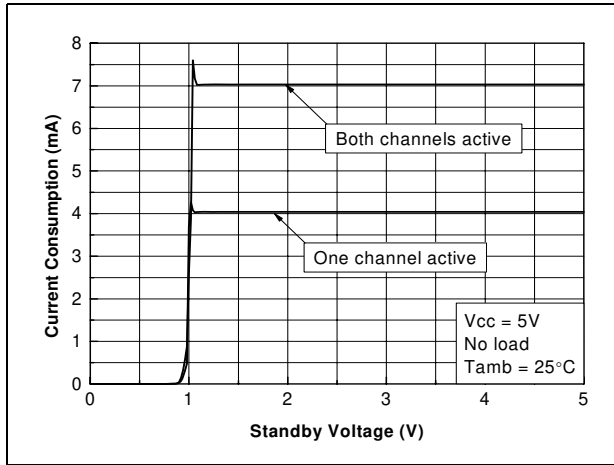


Figure 51. Current consumption vs. standby voltage

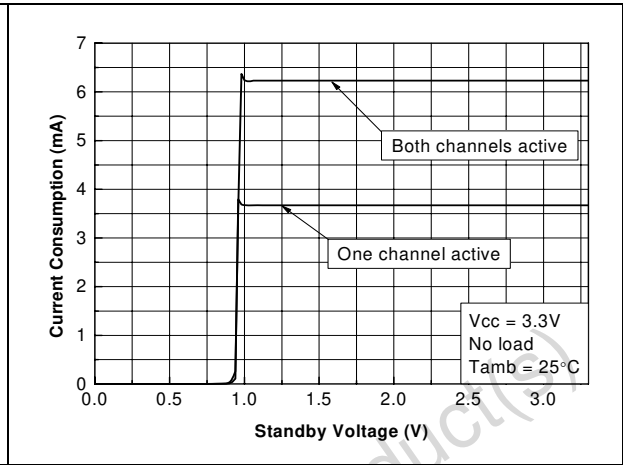


Figure 52. Current consumption vs. standby voltage

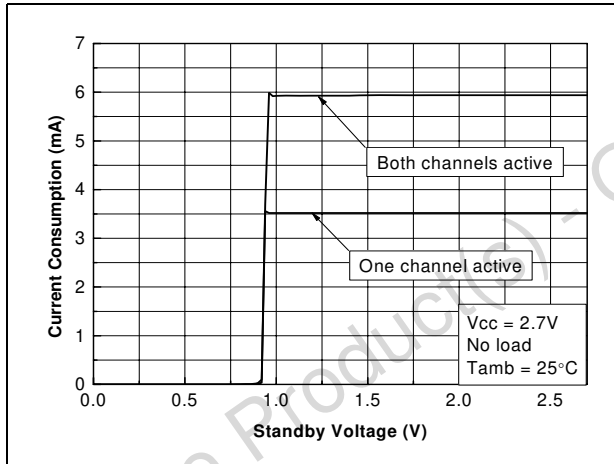


Figure 53. Standby current vs. power supply voltage

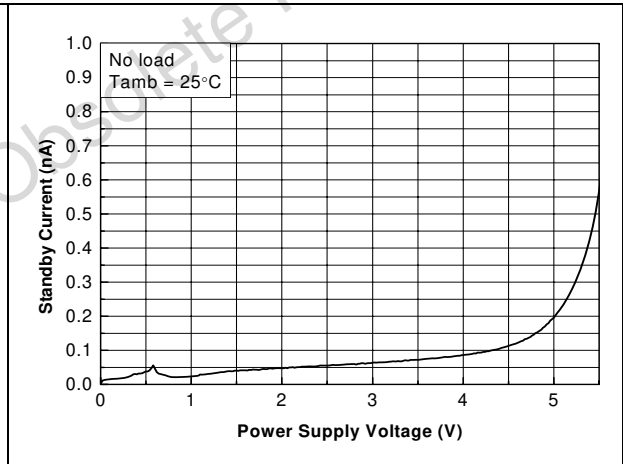


Figure 54. Frequency response

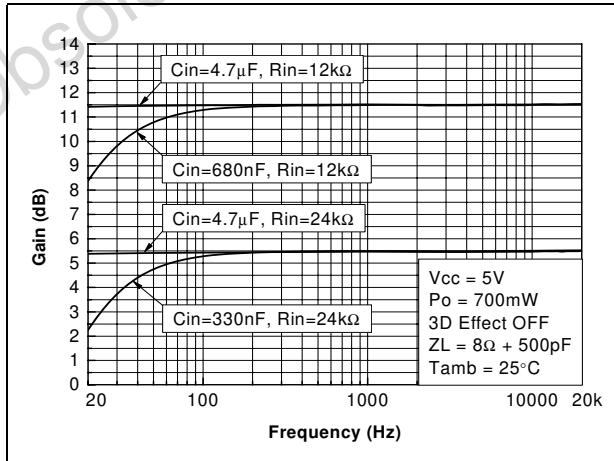


Figure 55. Frequency response

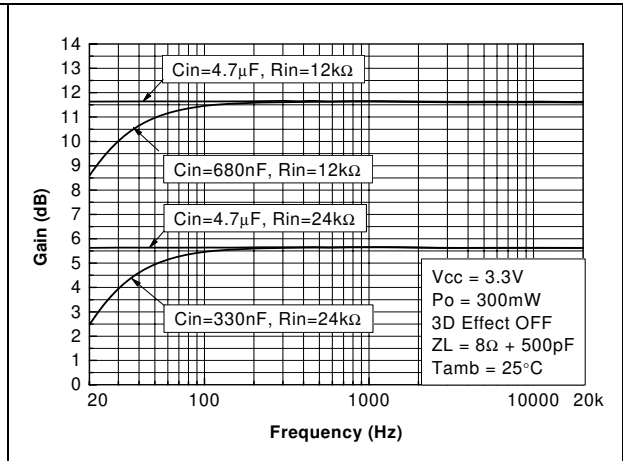


Figure 56. Frequency response

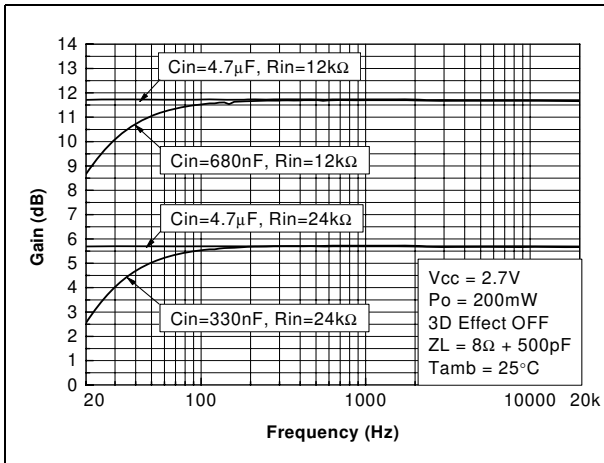


Figure 57. Output power vs. load resistance

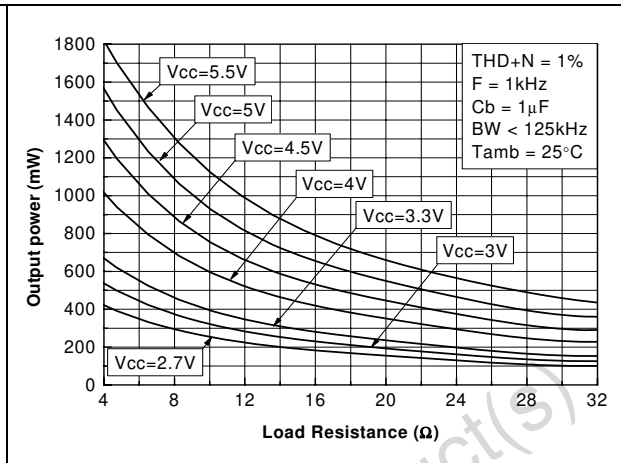


Figure 58. Output power vs. power supply voltage

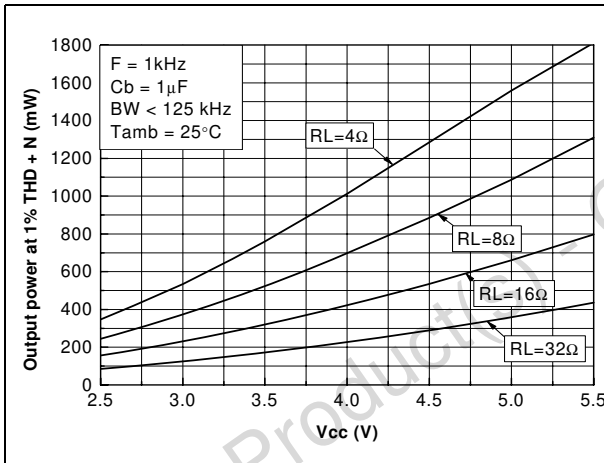


Figure 59. Output power vs. power supply voltage

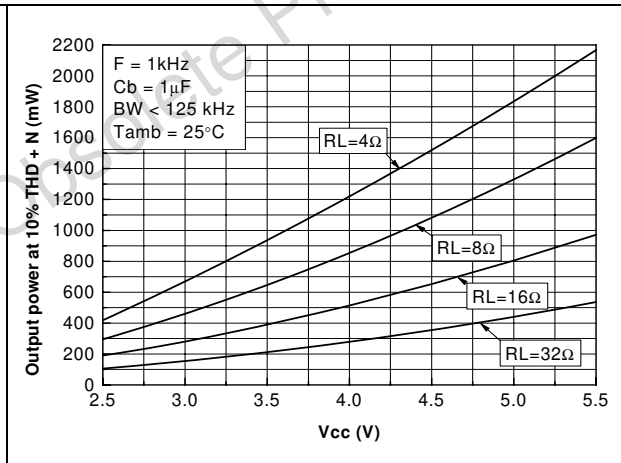


Figure 60. Power dissipation vs. output power

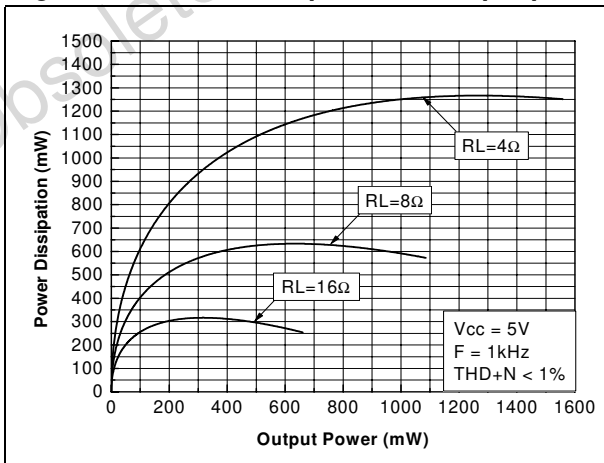


Figure 61. Power dissipation vs. output power

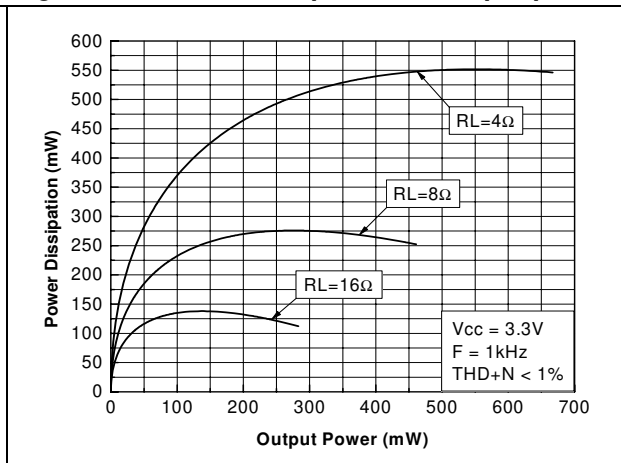


Figure 62. Power dissipation vs. output power Figure 63. Power derating curves

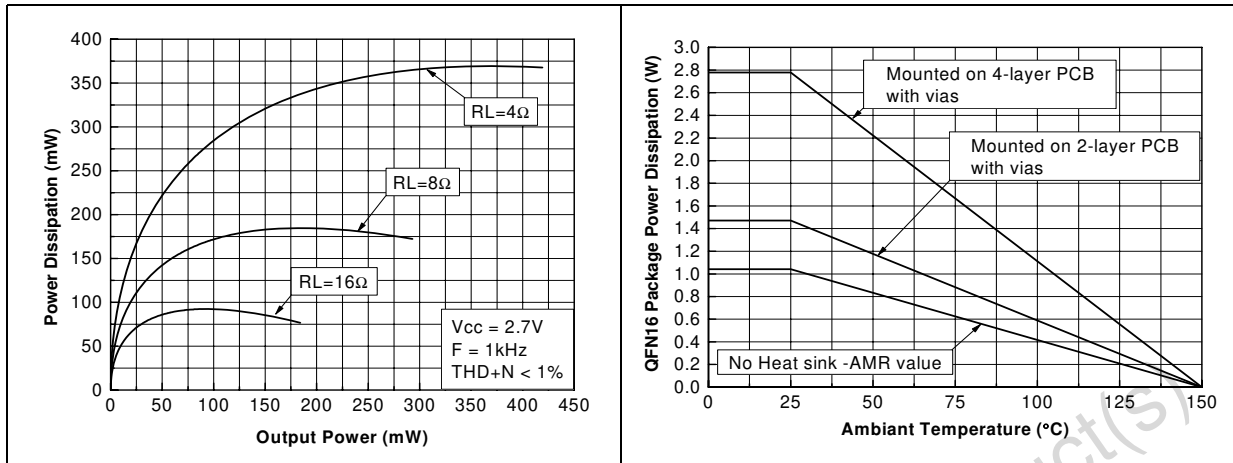


Table 8. Output noise, T_{amb} = 25°C

Conditions	3D effect level	Unweighted filter (20Hz to 20kHz) V _{CC} = 2.7V to 5.5V	A-weighted filter V _{CC} = 2.7V to 5.5V
Inputs floating	OFF	10μVrms	6μVrms
Inputs floating	LOW	18μVrms	12μVrms
Inputs floating	MEDIUM	24μVrms	15μVrms
Inputs floating	HIGH	34μVrms	22μVrms
Inputs grounded, G=6dB	OFF	15μVrms	10μVrms
Inputs grounded, G=6dB	LOW	28μVrms	19μVrms
Inputs grounded, G=6dB	MEDIUM	36μVrms	24μVrms
Inputs grounded, G=6dB	HIGH	52μVrms	35μVrms
Inputs grounded, G=12dB	OFF	20μVrms	14μVrms
Inputs grounded, G=12dB	LOW	39μVrms	26μVrms
Inputs grounded, G=12dB	MEDIUM	50μVrms	33μVrms
Inputs grounded, G=12dB	HIGH	71μVrms	48μVrms

4 Application information

4.1 General description

The TS4997 integrates two monolithic full-differential input/output power amplifiers with two selectable standby pins dedicated for each channel. The gain of each channel is set by external input resistors.

The TS4997 also features 3D effect enhancements that can be programmed through a two digital input pin interface that allows changing 3D effect levels in three steps.

4.2 Differential configuration principle

The TS4997 also includes a common mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ for any DC common mode input voltage. This allows maximum output voltage swing, and therefore, to maximize the output power. Moreover, as the load is connected differentially instead of single-ended, output power is four times higher for the same power supply voltage.

The **advantages** of a full-differential amplifier are:

- High PSRR (power supply rejection ratio),
- High common mode noise rejection,
- Virtually no pops&clicks without additional circuitry, giving a faster startup time compared to conventional single-ended input amplifiers,
- Easier interfacing with differential output audio DAC,
- No input coupling capacitors required due to common mode feedback loop.

In theory, the filtering of the internal bias by an external bypass capacitor is not necessary. However, to reach maximum performance in all tolerance situations, it is recommended to keep this option.

The only constraint is that the differential function is directly linked to external resistor mismatching, therefore you must pay particular attention to this mismatching in order to obtain the best performance from the amplifier.

4.3 Gain in typical application schematic

A typical differential application is shown in [Figure 1 on page 3](#).

The value of the differential gain of each amplifier is dependent on the values of external input resistors R_{IN1} to R_{IN4} and of integrated feedback resistors with fixed value. In the flat region of the frequency-response curve (no C_{IN} effect), the differential gain of each channel is expressed by the relation given in [Equation 1](#).

Equation 1

$$A_{V_{diff}} = \frac{V_{O+} - V_{O-}}{Diff_{input+} - Diff_{input-}} = \frac{R_{feed}}{R_{IN}} = \frac{50k\Omega}{R_{IN}}$$

where $R_{IN} = R_{IN1} = R_{IN2} = R_{IN3} = R_{IN4}$ expressed in $k\Omega$ and $R_{feed} = 50k\Omega$ (value of internal feedback resistors).

Due to the tolerance on the internal 50kΩ feedback resistors, the differential gain will be in the range (no tolerance on R_{IN}):

$$\frac{40\text{k}\Omega}{R_{IN}} \leq A_{V_{diff}} \leq \frac{60\text{k}\Omega}{R_{IN}}$$

The difference of resistance between input resistors of each channel have direct influence on the PSRR, CMRR and other amplifier parameters. In order to reach maximum performance, we recommend matching the input resistors R_{IN1} , R_{IN2} , R_{IN3} , and R_{IN4} with a maximum tolerance of 1%.

Note: For the rest of this section, $A_{V_{diff}}$ will be called A_V to simplify the mathematical expressions.

4.4 Common mode feedback loop limitations

As explained previously, the common mode feedback loop allows the output DC bias voltage to be averaged at $V_{CC}/2$ for any DC common mode bias input voltage.

Due to the V_{ICM} limitation of the input stage (see [Table 3 on page 4](#)), the common mode feedback loop can fulfil its role only within the defined range. This range depends upon the values of V_{CC} , R_{IN} and R_{feed} (A_V). To have a good estimation of the V_{ICM} value, use the following formula:

Equation 2

$$V_{ICM} = \frac{V_{CC} \times R_{IN} + 2 \times V_{ic} \times R_{feed}}{2 \times (R_{IN} + R_{feed})} = \frac{V_{CC} \times R_{IN} + 2 \times V_{ic} \times 50\text{k}\Omega}{2 \times (R_{IN} + 50\text{k}\Omega)} \text{ (V)}$$

with V_{CC} in volts, R_{IN} in kΩ and

$$V_{ic} = \frac{\text{Diff}_{input+} + \text{Diff}_{input-}}{2} \text{ (V)}$$

The result of the calculation must be in the range:

$$\text{GND} \leq V_{ICM} \leq V_{CC} - 1\text{V}$$

Due to the +/-20% tolerance on the 50kΩ feedback resistors R_{feed} (no tolerance on R_{IN}), it is also important to check that the V_{ICM} remains in this range at the tolerance limits:

$$\frac{V_{CC} \times R_{IN} + 2 \times V_{ic} \times 40\text{k}\Omega}{2 \times (R_{IN} + 40\text{k}\Omega)} \leq V_{ICM} \leq \frac{V_{CC} \times R_{IN} + 2 \times V_{ic} \times 60\text{k}\Omega}{2 \times (R_{IN} + 60\text{k}\Omega)} \text{ (V)}$$

If the result of the V_{ICM} calculation is not in this range, an input coupling capacitor must be used.

Example: $V_{CC} = 2.7\text{V}$, $A_V = 2$, and $V_{ic} = 2.2\text{V}$.

With internal resistors $R_{feed} = 50\text{k}\Omega$, calculated external resistors are $R_{IN} = R_{feed}/A_V = 25\text{k}\Omega$, $V_{CC} = 2.7\text{V}$ and $V_{ic} = 2.2\text{V}$, which gives $V_{ICM} = 1.92\text{V}$. Taking into account the tolerance on the feedback resistors, with $R_{feed} = 40\text{k}\Omega$ the common mode input voltage is $V_{ICM} = 1.87\text{V}$ and with $R_{feed} = 60\text{k}\Omega$, it is $V_{ICM} = 1.95\text{V}$.

These values are not in range from GND to $V_{CC} - 1\text{V} = 1.7\text{V}$, therefore input coupling capacitors are required. Alternatively, you can change the V_{ic} value.

4.5 Low frequency response

The input coupling capacitors block the DC part of the input signal at the amplifier inputs. In the low frequency region, C_{IN} starts to have an effect. C_{IN} and R_{IN} form a first-order high pass filter with a -3dB cut-off frequency.

$$F_{CL} = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}} \text{ (Hz)}$$

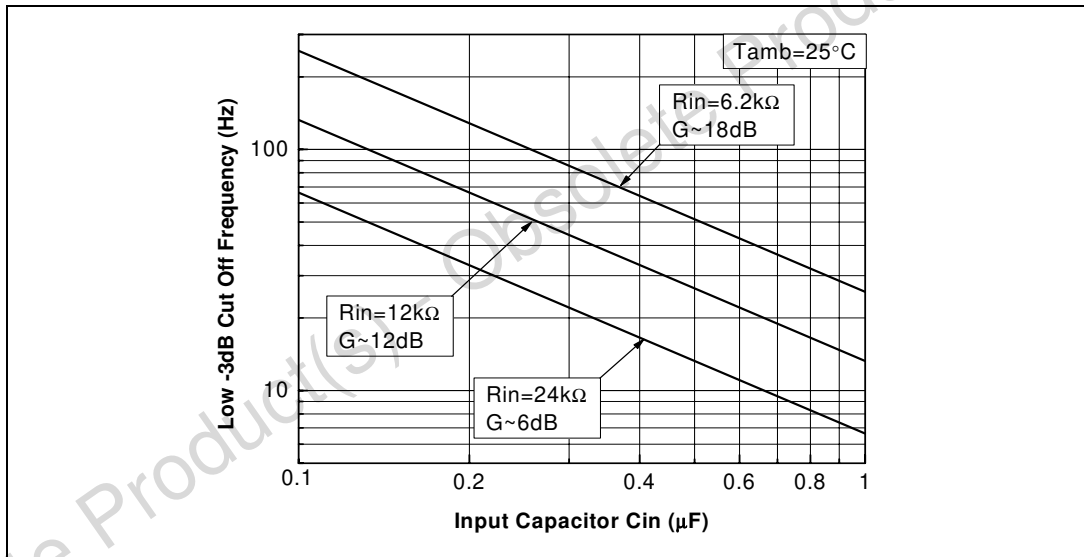
with R_{IN} expressed in Ω and C_{IN} expressed in F.

So, for a desired -3dB cut-off frequency we can calculate C_{IN} :

$$C_{IN} = \frac{1}{2 \times \pi \times R_{IN} \times F_{CL}} \text{ (F)}$$

From [Figure 64](#), you can easily establish the C_{IN} value required for a -3 dB cut-off frequency for some typical cases.

Figure 64. -3dB lower cut-off frequency vs. input capacitance



4.6 3D effect enhancement

The TS4997 features 3D audio effect which can be programmed at three discrete levels (LOW, MEDIUM, HIGH) through input pins 3D1 and 3D0 which provide a digital interface. The correspondence between the logic levels of this interface and 3D effect levels are shown in [Table 9](#).

The 3D audio effect applied to stereo audio signals evokes perception of spatial hearing and improves this effect in cases where the stereo speakers are too close to each other, such as in small handheld devices, or mobile equipment.

The perceived amount of 3D effect is also dependent on many factors such as speaker position, distance between speakers and listener, frequency spectrum of audio signal, or difference of signal between left and right channel. In some cases, the volume can increase when switching on the 3D effect. This factor is dependent on the composition of the stereo audio signal and its frequency spectrum.

Table 9. 3D effect settings

3D effect level	3D0	3D1
OFF	0	0
LOW	0	1
MEDIUM	1	0
HIGH	1	1

4.7 Power dissipation and efficiency

Assumptions:

- Load voltage and current are sinusoidal (V_{out} and I_{out})
- Supply voltage is a pure DC source (V_{CC})

The output voltage is:

$$V_{out} = V_{peak} \sin \omega t \text{ (V)}$$

and

$$I_{out} = \frac{V_{out}}{R_L} \text{ (A)}$$

and

$$P_{out} = \frac{V_{peak}^2}{2R_L} \text{ (W)}$$

Therefore, the average current delivered by the supply voltage is:

Equation 3

$$I_{ccAVG} = 2 \frac{V_{peak}}{\pi R_L} \text{ (A)}$$

The power delivered by the supply voltage is:

Equation 4

$$P_{supply} = V_{CC} I_{ccAVG} \text{ (W)}$$

Therefore, the **power dissipated by each amplifier** is:

$$P_{diss} = P_{supply} - P_{out} \text{ (W)}$$

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}} \sqrt{P_{out}} - P_{out} \text{ (W)}$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{out}} = 0$$

and its value is:

Equation 5

$$P_{dissmax} = \frac{2V_{CC}^2}{\pi^2 R_L} \text{ (W)}$$

Note: This maximum value is only dependent on the power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

Equation 6

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{peak}}{4V_{CC}}$$

The maximum theoretical value is reached when $V_{peak} = V_{CC}$, so:

$$\eta = \frac{\pi}{4} = 78.5\%$$

The TS4997 is stereo amplifier so it has two power amplifiers. Each amplifier produces heat due to its power dissipation. Therefore, the maximum die temperature is the sum of each amplifier's maximum power dissipation. It is calculated as follows:

- P_{diss1} = Power dissipation of left channel power amplifier
- P_{diss2} = Power dissipation of right channel power amplifier
- Total $P_{diss} = P_{diss1} + P_{diss2}$ (W)

In most cases, $P_{diss1} = P_{diss2}$, giving:

$$\text{Total } P_{diss} = 2 \times P_{diss1} = \frac{4\sqrt{2}V_{CC}}{\pi\sqrt{R_L}} \sqrt{P_{out}} - 2P_{out} \text{ (W)}$$

The maximum die temperature allowable for the TS4997 is 150°C. In case of overheating, a thermal shutdown protection set to 150°C, puts the TS4997 in standby until the temperature of the die is reduced by about 5°C.

To calculate the maximum ambient temperature T_{amb} allowable, you need to know:

- the power supply voltage value, V_{CC}
- the load resistor value, R_L
- the package type, R_{THJA}

Example: $V_{CC}=5V$, $R_L=8\Omega$, $R_{THJAQFN16}=85^\circ\text{C/W}$ (with 2-layer PCB with vias).

Using the power dissipation formula given in [Equation 5](#), the maximum dissipated power per channel is:

$$P_{dissmax} = 633\text{mW}$$

And the power dissipated by both channels is:

$$\text{Total } P_{dissmax} = 2 \times P_{dissmax} = 1266\text{mW}$$

T_{amb} is calculated as follows:

Equation 7

$$T_{amb} = 150^{\circ}\text{C} - R_{THJA} \times \text{Total } P_{dissmax}$$

Therefore, the maximum allowable value for T_{amb} is:

$$T_{amb} = 150 - 85 \times 2 \times 1.266 = 42.4^{\circ}\text{C}$$

If a 4-layer PCB with vias is used, $R_{THJA, QFN16} = 45^{\circ}\text{C/W}$ and the maximum allowable value for T_{amb} in this case is:

$$T_{amb} = 150 - 45 \times 2 \times 1.266 = 93^{\circ}\text{C}$$

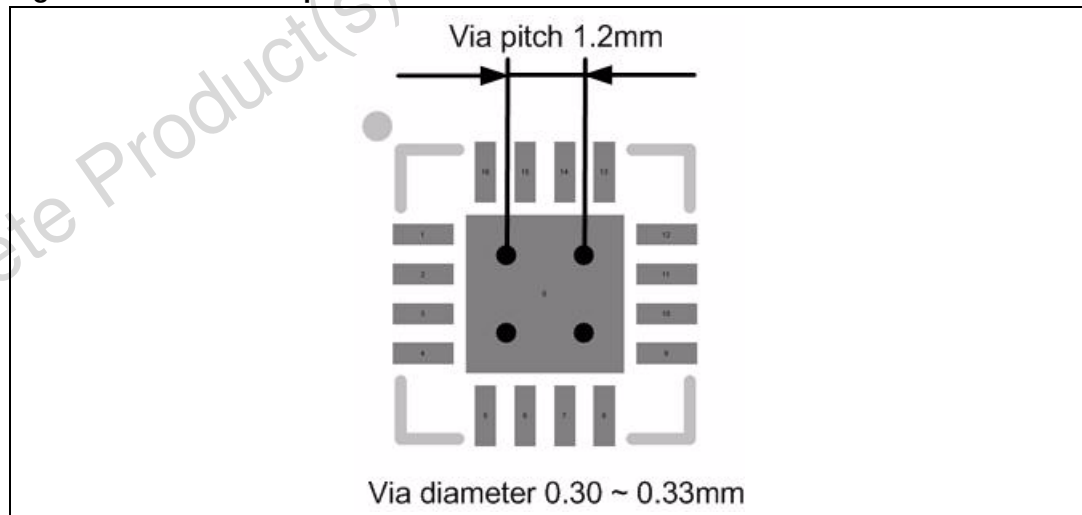
4.8 Footprint recommendation

Footprint soldering pad dimensions are given in [Figure 72 on page 31](#). As discussed in the previous section, the maximum allowable value for ambient temperature is dependent on the thermal resistance junction to ambient R_{THJA} . Decreasing the R_{THJA} value causes better power dissipation.

Based on best thermal performance, it is recommended to use 4-layer PCBs with vias to effectively remove heat from the device. It is also recommended to use vias for 2-layer PCBs to connect the package exposed pad to heatsink copper areas placed on another layer.

For proper thermal conductivity, the vias must be plated through and solder-filled. Typical thermal vias have the following dimensions: 1.2mm pitch, 0.3mm diameter.

Figure 65. QFN16 footprint recommendation



4.9 Decoupling of the circuit

Two capacitors are needed to correctly bypass the TS4997: a power supply bypass capacitor C_S and a bias voltage bypass capacitor C_b .