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The revision list summarizes the locations of revisions and additions. Details should always be checked by referring to the relevant text.

H8S/2329 Group

Hardware Manual

Renesas 16-Bit Single-Chip Microcomputer

H8S Family/H8S/2300 Series

H8S/2329	HD64F2329B	H8S/2324S	HD6412324S
	HD64F2329E	H8S/2323	HD6432323
H8S/2328	HD6432328	H8S/2322R	HD6412322R
	HD64F2328B	H8S/2321	HD6412321
H8S/2327	HD6432327	H8S/2320	HD6412320
H8S/2326	HD64F2326		

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

— The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions may occur due to the false recognition of the pin state as an input signal. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

— The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

— The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

— When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

— The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

Preface

This LSI is a single-chip microcomputer made up of the H8S/2000 CPU with an internal 32-bit architecture as its core, and the peripheral functions required to configure a system.

This LSI is equipped with ROM, RAM, a bus controller, data transfer controller (DTC), a 16-bit timer pulse unit (TPU), a watchdog timer (WDT), a serial communication interface (SCI), DMA controller (DMAC), a D/A converter, an A/D converter, and I/O ports as on-chip supporting modules. This LSI is suitable for use as an embedded processor for high-level control systems. Its on-chip ROM are flash memory (F-ZTAT^{TM*}) and mask ROM that provides flexibility as it can be reprogrammed in no time to cope with all situations from the early stages of mass production to full-scale mass production. This is particularly applicable to application devices with specifications that will most probably change.

Note: * F-ZTAT is a trademark of Renesas Technology Corp.

Target Users: This manual was written for users who will be using the H8S/2329 Group, H8S/2328 Group in the design of application systems. Members of this audience are expected to understand the fundamentals of electrical circuits, logical circuits, and microcomputers.

Objective: This manual was written to explain the hardware functions and electrical characteristics of the H8S/2329 Group, H8S/2328 Group to the above audience. Refer to the H8S/2600 Series, H8S/2000 Series Software Manual for a detailed description of the instruction set.

Notes on reading this manual:

- In order to understand the overall functions of the chip
Read the manual according to the contents. This manual can be roughly categorized into parts on the CPU, system control functions, peripheral functions and electrical characteristics.
- In order to understand the details of the CPU's functions
Read the H8S/2600 Series, H8S/2000 Series Software Manual.
- In order to understand the details of a register when its name is known
The addresses, bits, and initial values of the registers are summarized in appendix B, Internal I/O Registers.

Example: Bit order: The MSB is on the left and the LSB is on the right.

Related Manuals: The latest versions of all related manuals are available from our web site. Please ensure you have the latest versions of all documents you require.
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H8S/2329 Group, H8S/2328 Group Manuals:

Document Title	Document No.
H8S/2329 Group, H8S/2328 Group Hardware Manual	This manual
H8S/2600 Series, H8S/2000 Series Software Manual	REJ09B0139


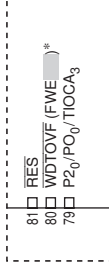
User's Manuals for Development Tools:

Document Title	Document No.
H8S, H8S/300 Series C/C++ Compiler, Assembler, Optimized Linkage Editor Compiler Package Ver.6.01 User's Manual	REJ10B0161
H8S, H8S/300 Series Simulator/Debugger (for Windows) User's Manual	ADE-702-037
High-performance Embedded Workshop (for Windows 95/98 and Windows NT 4.0) User's Manual	ADE-702-201

Application Notes:

Document Title	Document No.
H8S Series Technical Q & A Application Note	REJ05B0397

Main Revisions for This Edition

Item	Page	Revision (See Manual for Details)
1.3.1 Pin Arrangement Figure 1.3 Mask ROM Versions, F-ZTAT Versions, H8S/2324S, H8S/2322R, H8S/2320 Pin Arrangement (TFP-120: Top View)	10	Figure amended
		
		Note amended
		Note: * The FWE pin applies to the H8S/2328B F-ZTAT and H8S/2326 F-ZTAT only.
		The WDT0VF pin function is not available in the F-ZTAT versions.
Figure 1.4 Mask ROM Versions, F-ZTAT Versions, H8S/2324S, H8S/2322R, H8S/2320 Pin Arrangement (FP-128B: Top View)	11	Figure amended
		
		Note amended
		Note: * The FWE pin applies to the H8S/2328B F-ZTAT and H8S/2326 F-ZTAT only.
		The WDT0VF pin function is not available in the F-ZTAT versions.
Figure 1.7 HD64F2329B Pin Arrangement (TFP-120: Top View)	14	Figure added

1.3.1 Pin Arrangement 15 Figure added

Figure 1.8
HD64F2329B Pin
Arrangement (FP-
128B: Top View)

1.3.3 Pin Functions 26 Table amended

Table 1.3 Pin Functions

MD_2	MD_1	MD_0	Operating Mode
0	0	1	—
	1	0	Mode 2 ^{*1}
		1	Mode 3 ^{*1}
1	0	0	Mode 4 ^{*2}
		1	Mode 5 ^{*2}
	1	0	Mode 6
		1	Mode 7

6.3.5 Chip Select Signals 169

Description amended

Enabling or disabling of the \overline{CS}_n signal is performed by setting the data direction register (DDR) for the port corresponding to the particular \overline{CS}_n pin and either the CS167 enable bit (CS167E) or the CS25 enable bit (CS25E).

In ROM-disabled expansion mode, the \overline{CS}_0 pin is placed in the output state after a power-on reset. Pins \overline{CS}_1 to \overline{CS}_7 are placed in the input state after a power-on reset, so the corresponding DDR bits, and CS167E or CS25E, should be set to 1 when outputting signals \overline{CS}_1 to \overline{CS}_7 .

In ROM-enabled expansion mode, pins \overline{CS}_0 to \overline{CS}_7 are all placed in the input state after a power-on reset, so the corresponding DDR bits, and CS167E or CS25E, should be set to 1 when outputting signals \overline{CS}_0 to \overline{CS}_7 .

Item	Page	Revision (See Manual for Details)																																																
14.2.8 Bit Rate Register (BRR)	618	Table amended																																																
Table 14.3 BRR Settings for Various Bit Rates (Asynchronous Mode)		<div style="text-align: right;">$\phi = 25 \text{ MHz}$</div> <table border="1"> <thead> <tr> <th>Bit Rate (bits/s)</th> <th>n</th> <th>N</th> <th>Error (%)</th> </tr> </thead> <tbody> <tr><td>110</td><td>3</td><td>110</td><td>-0.02</td></tr> <tr><td>150</td><td>3</td><td>80</td><td>0.47</td></tr> <tr><td>300</td><td>2</td><td>162</td><td>-0.15</td></tr> <tr><td>600</td><td>2</td><td>80</td><td>0.47</td></tr> <tr><td>1200</td><td>1</td><td>162</td><td>-0.15</td></tr> <tr><td>2400</td><td>1</td><td>80</td><td>0.47</td></tr> <tr><td>4800</td><td>0</td><td>162</td><td>-0.15</td></tr> <tr><td>9600</td><td>0</td><td>80</td><td>0.47</td></tr> <tr><td>19200</td><td>0</td><td>40</td><td>-0.76</td></tr> <tr><td>31250</td><td>0</td><td>24</td><td>1.00</td></tr> <tr><td>38400</td><td>0</td><td>19</td><td>1.73</td></tr> </tbody> </table>	Bit Rate (bits/s)	n	N	Error (%)	110	3	110	-0.02	150	3	80	0.47	300	2	162	-0.15	600	2	80	0.47	1200	1	162	-0.15	2400	1	80	0.47	4800	0	162	-0.15	9600	0	80	0.47	19200	0	40	-0.76	31250	0	24	1.00	38400	0	19	1.73
Bit Rate (bits/s)	n	N	Error (%)																																															
110	3	110	-0.02																																															
150	3	80	0.47																																															
300	2	162	-0.15																																															
600	2	80	0.47																																															
1200	1	162	-0.15																																															
2400	1	80	0.47																																															
4800	0	162	-0.15																																															
9600	0	80	0.47																																															
19200	0	40	-0.76																																															
31250	0	24	1.00																																															
38400	0	19	1.73																																															

19.4.1 Features 740 Description amended
The flash memory can be reprogrammed **minimum** 100 times.

19.13.1 Features 791 Description amended
The flash memory can be reprogrammed **minimum** 100 times.

19.22.1 Features 849 Description amended
The flash memory can be reprogrammed **minimum** 100 times.

22.2.6 Flash Memory Characteristics 977 Table amended

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Programming time ^{*1 *2 *4}	t_p	—	10	200	ms/128 bytes	
Erase time ^{*1 *3 *6}	t_E	—	50	1000	ms/block	
Rewrite times	N_{WEC}	100 ^{*7}	10000 ^{*8}	—	Times	
Data hold time	t_{DRP} ^{*9}	10	—	—	year	
Programming Wait time after SWE bit setting ^{*1}	x	1	—	—	s	
Wait time after PSU bit setting ^{*1}	y	50	—	—	s	

Item	Page	Revision (See Manual for Details)
22.2.6 Flash Memory Characteristics	978	Notes added
Table 22.22 Flash Memory Characteristics		<p>7. The minimum number of rewrites after which all characteristics are guaranteed. (The guaranteed range is one to min. rewrites.)</p> <p>8. Reference value at 25°C. (This is a general indication of the number of rewrites possible under normal conditions.)</p> <p>9. The data retention characteristics within the specified range, including min. rewrites.</p>
Appendix F Package Dimensions	1267	Figure replaced
Figure F.1 TFP-120 Package Dimensions		
Figure F.2 FP-128B Package Dimensions	1268	Figure replaced

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