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User's Manual

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The revision list can be viewed directly by clicking the title page.

The revision list summarizes the locations of revisions and additions. Details should always be checked by referring to the relevant text.

H8/38086R Group

Hardware Manual

Renesas 16-Bit Single-Chip Microcomputer H8 Family/H8/300H Super Low Power Series

H8/38086RF
H8/38086R
H8/38085R
H8/38084R
H8/38083R

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Rev.3.00 2006.08

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General Precautions on Handling of Product

1. Treatment of NC Pins

Note: Do not connect anything to the NC pins.
The NC (not connected) pins are either not connected to any of the internal circuitry or are used as test pins or to reduce noise. If something is connected to the NC pins, the operation of the LSI is not guaranteed.

2. Treatment of Unused Input Pins

Note: Fix all unused input pins to high or low level.
Generally, the input pins of CMOS products are high-impedance input pins. If unused pins are in their open states, intermediate levels are induced by noise in the vicinity, a pass-through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.
The states of internal circuits are undefined until full power is supplied throughout the chip and a low level is input on the reset pin. During the period where the states are undefined, the register settings and the output state of each pin are also undefined. Design your system so that it does not malfunction because of processing while it is in this undefined state. For those products which have a reset function, reset the LSI immediately after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.
The undefined or reserved addresses may be used to expand functions, or test registers may have been be allocated to these addresses. Do not access these registers; the system's operation is not guaranteed if they are accessed.

Configuration of This Manual

This manual comprises the following items:

1. General Precautions on Handling of Product
2. Configuration of This Manual
3. Preface
4. Main Revisions for This Edition

   The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.
5. Contents
6. Overview
7. Description of Functional Modules
   - CPU and System-Control Modules
   - On-Chip Peripheral Modules

   The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

   i) Feature
   ii) Input/Output Pin
   iii) Register Description
   iv) Operation
   v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

8. List of Registers
9. Electrical Characteristics
10. Appendix
11. Index

Preface

H8/38086R Group is single-chip microcomputers made up of the high-speed H8/300H CPU employing Renesas Technology original architecture as their cores, and the peripheral functions required to configure a system. The H8/300H CPU has an instruction set that is compatible with the H8/300 CPU.

Target Users: This manual was written for users who will be using the H8/38086R Group in the design of application systems. Target users are expected to understand the fundamentals of electrical circuits, logical circuits, and microcomputers.

Objective: This manual was written to explain the hardware functions and electrical characteristics of the H8/38086R Group to the target users.
Refer to the H8/300H Series Software Manual for a detailed description of the instruction set.

Notes on reading this manual:

- In order to understand the overall functions of the chip
  Read the manual according to the contents. This manual can be roughly categorized into parts on the CPU, system control functions, peripheral functions, and electrical characteristics.
- In order to understand the details of the CPU's functions
  Read the H8/300H Series Software Manual.
- In order to understand the details of a register when its name is known
  Read the index that is the final part of the manual to find the page number of the entry on the register. The addresses, bits, and initial values of the registers are summarized in section 24, List of Registers.

Example:	Register name:	The following notation is used for cases when the same or a similar function, e.g. serial communication interface, is implemented on more than one channel: XXX_N (XXX is the register name and N is the channel number)
	Bit order:	The MSB is on the left and the LSB is on the right.

Notes:

When using an on-chip debugger (such as the E7 or E8) for H8/38086R program development and debugging, the following restrictions must be noted.

1. The $\overline{\text{NMI}}$ pin is reserved for the on-chip debugger, and cannot be used.
2. Pins P16, P36, and P37 cannot be used. In order to use these pins, additional hardware must be provided on the user board.
3. Area H'C000 to H'CFFF is used by the on-chip debugger, and is not available to the user.
4. Area H′F380 to H′F77F must on no account be accessed.
5. When the on-chip debugger is used, address breaks can be set as either available to the user or for use by the on-chip debugger. If address breaks are set as being used by the on-chip debugger, the address break control registers must not be accessed.
6. When the on-chip debugger is used, $\overline{\text{NMI}}$ is an input pin, P16 and P36 are input pins, and P37 is an output pin.
7. When on-board programming/erasing is performed in boot mode, the SCI3 (P41/RXD and P42/TXD) is used.
8. When using the on-chip debugger, set the FROMCKSTP bit in clock halt register 1 to 1.

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H8/38086R Group manuals:

Document Title	Document No.
H8/38086R Group Hardware Manual	This manual
H8/300H Series Software Manual	REJ09B0213

User's manuals for development tools:

Document Title	Document No.
H8S, H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual	REJ10B0058
H8S, H8/300 Series Simulator/Debugger User's Manual	ADE-702-282
H8S, H8/300 Series High-performance Embedded Workshop 3 Tutorial	REJ10B0024
H8S, H8/300 Series High-performance Embedded Workshop 3 User's Manual	REJ10B0026

Application notes:

Document Title	Document No.
F-ZTAT Microcomputer On-Board Programming	REJ05B0523

Main Revisions for This Edition

Item	Page	Revision (See Manual for Details)
All	—	(Before) E7 → (After) on-chip debugger
Preface	vi	When using an on-chip debugger (such as the E7 or E8) for H8/38086R program development and debugging, ...
1.1 Features	2	• Compact package Table amended

Package	Code	Old Code	Body Size	Pin Pitch	Remarks
QFP-80	PRQP0080JB-A	FP-80A	14 × 14 mm	0.65 mm	
TQFP-80	PTQP0080KC-A	TFP-80C	12 × 12 mm	0.5 mm	
P-TFLGA-85	PTLG0085JA-A	TLP-85V	7 × 7 mm	0.65 mm	

1.2 Internal Block Diagram Figure1.1 Internal Block Diagram of H8/38076R Group	3	Note 2 amended 2. The SCK4, SI4, SO4, and $\overline{\text{NMI}}$ pins are not available when the E7 or on-chip debugger is used.
1.4 Pin Functions Table 1.4 Pin Functions	19	Table amended

Type	Symbol	Pin No. FP-80A, TFP-80C	Pin No. TLP-85V	Pad No.*1	Pad No.*2	I/O	Functions
16-bit timer pulse unit (TPU)	TIOCA1	80	A3	81	80	I/O	Pins for the TGR1A input capture input or output compare output, or PWM output.
	TIOCB1	1	B1	1	1	Input	Pins for the TGR1B input capture input.
	TIOCA2	2	C1	2	2	I/O	Pins for the TGR2A input capture input or output compare output, or PWM output.
	TIOCB2	3	B2	3	3	Input	Pins for the TGR2B input capture input.

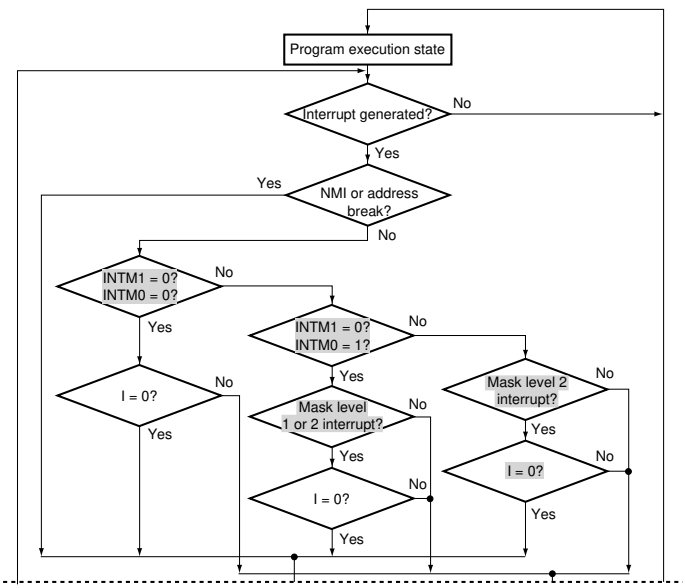
2.1 Address Space and Memory Map Figure 2.1 Memory Map	26	Note amended Note: The areas from H'C000 to H'CFFF and from H'F380 to H'F77F are used by the on-chip debugger. They are not available to the user when the on-chip debugger is being used.

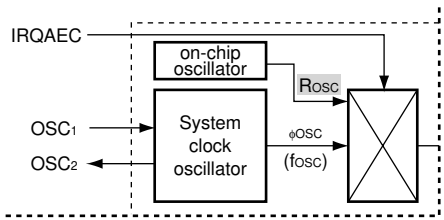
Item	Page	Revision (See Manual for Details)
2.8.3 Bit-Manipulation Instruction	57	• Prior to executing BSET instruction MOV.B #H'80, R0L
	59	• Prior to executing BCLR instruction MOV.B #H'3F, R0L
3.1 Exception Sources and Vector Address Table 3.1 Exception Sources and Vector Address	62	Table amended

Source Origin	Exception Sources	Vector Number	Vector Address	Priority
Address break	Break conditions satisfied	5	H'000A to H'000B	
Internal interrupts*	—	19 to 43	H'0026 to H'0057	Low

3.2 Reset	63, 64	Replaced
3.3 Interrupts	65	Description amended .. The interrupt controller can set interrupts other than NMI to one of three mask levels in order to control multiple interrupts. The interrupt priority registers A to E (IPRA to IPRE) of the interrupt controller set the interrupt mask level.
3.5.1 Notes on Stack Area Use	68	Description amended To save register values, use PUSH.W Rn (MOV.W Rn, @–SP) or PUSH.L ERn (MOV.L ERn, @–SP). To restore register values, use POP.W Rn (MOV.W @SP+, Rn) or POP.L ERn (MOV.L @SP+, ERn). During interrupt exception handling or when an RTE instruction is executed, CCR contents are saved and restored in word size.
Section 4 Interrupt Controller 4.1 Features	73	Description amended • Mask levels settable with IPR An interrupt priority register (IPR) is provided for setting interrupt mask levels. Three mask levels can be set for each module for all interrupts except NMI and address break.

Item	Page	Revision (See Manual for Details)
4.3.8 Interrupt Priority Registers A to E (IPRA to IPRE)	84	Description amended IPR sets mask levels (levels 2 to 0) for interrupts other than NMI and address break. ... Setting a value in the range from H'0 to H'3 in the 2-bit groups of bits 7 and 6, 5 and 4, 3 and 2, and 1 and 0 sets the mask level of the corresponding interrupt. ... Table amended (Before) Priority level → (After) Mask level
4.3.9 Interrupt Mask Register (INTM)	85	Table amended (Before) Priority level → (After) Mask level
4.4.1 External Interrupts	86	(2) WKP7 to WKP0 Interrupts ... The interrupt mask level can be set by IPR. (3) IRQ4, IRQ3, IRQ1, and IRQ0 Interrupts ... The interrupt mask level can be set by IPR. (4) IRQAEC Interrupts ... The interrupt mask level can be set by IPR.
4.4.2 Internal Interrupts	87	• The interrupt mask level can be set by IPR.
4.5 Interrupt Exception Handling Vector Table	87	Description amended ... The lower the vector number, the higher the priority. The priority within a module is fixed. Mask levels for Interrupts other than NMI and address break can be modified by IPR.

Item	Page	Revision (See Manual for Details)
4.6 Operation Table 4.3 Interrupt Control States	90	Table amended (Before) priority level → (After) mask level
	90, 91	Description amended 2. The following control operations are performed by referencing the INTM1 and INTM0 bits in INTM and the I bit in CCR. • When the I bit is set to 1, the interrupt request is held pending. • When the I bit is cleared to 0 and the INTM1 bit is set to 1, interrupts with mask level 1 or below are held pending. • When the I bit is cleared to 0, the INTM1 bit is cleared to 0, and the INTM0 bit is set to 1, interrupt requests with mask level 0 are held pending. • When the I bit, INTM1 bit, and INTM0 bit are all cleared to 0, all interrupt requests are accepted. 3. If contention occurs between interrupts that are not held pending by the INTM1 and INTM0 bits in the INTM register and the I bit in CCR, the interrupt with the highest priority as shown in table 4.2 is selected, regardless of the IPR setting.
Figure 4.2 Flowchart of Procedure Up to Interrupt Acceptance	92	Figure amended 

Item	Page	Revision (See Manual for Details)
4.6.1 Interrupt Exception Handling Sequence Figure 4.3 Interrupt Exception Handling Sequence	93	Figure amended (Before) Address bus → (After) Internal address bus (Before) $\overline{RD}$ → (After) Internal read signal (Before) $\overline{HWR}$, $\overline{LWR}$ → (After) Internal write signal (Before) D_{15} to D_0 → (After) Internal data bus
4.6.2 Interrupt Response Times Table 4.4 Interrupt Response Times (States)	94	Table amended No. / Execution Status / Number of States 1 / Interrupt mask level determination / 1 or 2*1 Note 1 amended 1. One state for internal interrupts and two states for external interrupts.
4.7.2 Instructions that Disable Interrupts	96	Description amended When an interrupt request is generated, an interrupt is request is sent to the CPU after the interrupt controller has determined the mask level.
Section 5 Clock Pulse Generators Figure 5.1 Block Diagram of Clock Pulse Generators (Masked ROM Version) (2)	98	Figure amended 
5.2 System Clock Generator Figure 5.2 Typical Connection to Crystal Resonator	101	Figure amended Frequency / Manufacturer / Product Type / C_1, C_2 Recommendation Value 4.19 MHz / Kyocera Kinseki Corporation / HC-491U-S / 22 pF ±20%
5.2.4 On-Chip Oscillator Selection Method (Supported only by the Masked ROM Version)	102	Description amended ... The setting takes effect when the rest is cleared. When the on-chip oscillator is selected, ...

Item	Page	Revision (See Manual for Details)
5.3.1 Connecting 32.768-kHz/38.4-kHz Crystal Resonator	103	Description amended Clock pulses can be supplied to the subclock generator by connecting a 32.768-kHz or 38.4-kHz crystal resonator, ...
Figure 5.5 Typical Connection to 32.768-kHz/38.4-kHz Crystal Resonator		Figure amended

Frequency	Manufacturer	Products Name	C_1, C_2 Recommendation Value	Equivalent Series Resistance
38.4 kHz	Epson Toyocom	C-4-TYPE	7 pF	30 kΩ max
32.768 kHz	Epson Toyocom	C-001R	7 pF	35 kΩ max

Figure 5.6 Equivalent Circuit of 32.768-kHz/38.4-kHz Crystal Resonator	104	Figure amended C_o = 0.9 pF(typ.) R_s = 35 kΩ (max.)
	104	Description added Notes on Use of Subclock Generator Circuit The drive capacity of the subclock generator circuit is limited in order to reduce current consumption when operating in the subclock mode. As a result, there may not be sufficient additional margin to accommodate some resonators. Be sure to select a resonator with an equivalent series resistance (R_S) corresponding to that shown in figure 5.6.
5.3.3 External Clock Input Method	105	Title amended
5.4.1 Prescaler S		Description amended The output from prescaler S is shared by the on-chip peripheral modules. In active (medium-speed) mode and sleep (medium-speed) mode,
5.5.3 Definition of Oscillation Stabilization Wait Time	108, 109	Replaced
5.5.6 Note on Using Power-On Reset Circuit	110	Description amended The LSI's internal power-on reset circuit can be adjusted by connecting an external capacitor to the $\overline{\text{RES}}$ pin. Adjust the capacitance of the external capacitor to ensure sufficient oscillation stabilization time before reset clearing. For details, see section 22, Power-On Reset Circuit.

Item	Page	Revision (See Manual for Details)
6.1.1 System Control Register 1 (SYSCR1)	112	Table amended

Bit	Bit Name	Initial Value	R/W	Description
6	STS2	0	R/W	When an external clock is to be used, the minimum value (STS2 = 1, STS1 = 0, STS0 = 1) is recommended.
5	STS1	0	R/W	
4	STS0	0	R/W	If the internal oscillator is used, the settings CTCS2 = 0, STS = 1, and STS0 = 0 are recommended. If the setting other than the recommended value is made, operation may start before the end of the waiting time.

Item	Page	Revision (See Manual for Details)
6.1.2 System Control Register 2 (SYSCR2)	114	Table amended

Bit	Bit Name	Initial Value	R/W	Description
4	NESEL	1	R/W	Noise Elimination Sampling Frequency Select The subclock pulse generator generates the watch clock signal (ϕ_w) and the system clock pulse generator generates the oscillator clock (ϕ_{osc}). This bit selects the sampling frequency of ϕ_{osc} when ϕ_w is sampled. When ϕ_{osc} = 2 to 10 MHz, clear this bit to 0. Set it to 1 if the internal oscillator is used. 0: Sampling rate is ϕ_{osc}/16. 1: Sampling rate is ϕ_{osc}/4.
1	SA1	0	R/W	Subactive Mode Clock Select 1 and 0
0	SA0	0	R/W	Select the operating clock frequency in subactive and subsleep modes. The values of SA1 and SA0 do not change if they are written to in subactive mode. 00: ϕ_w/8 01: ϕ_w/4 1X: ϕ_w/2

Item	Page	Revision (See Manual for Details)
6.1.3 Clock Halt Registers 1 and 2 (CKSTPR1 and CKSTPR2)	115	Table amended

Bit	Bit Name	Initial Value	R/W	Description
7	S4CKSTP*1*4	1	R/W*1	SCI4 Module Standby SCI4 enters standby mode when this bit is cleared to 0.
1	FROMCKSTP*1*4	1	R/W	Flash Memory Module Standby Flash memory enters standby mode when this bit is cleared to 0.

Item	Page	Revision (See Manual for Details)
6.2 Mode Transitions and States of LSI Figure 6.1 Mode Transition Diagram	118	Note amended A transition between different modes cannot be made to occur simply because an interrupt request is generated. Make sure to enable interrupt requests.
Table 6.2 Transition Mode after SLEEP Instruction Execution and Interrupt Handling	120	Table amended

State Before Transition	LSON	MSON	SSBY	TMA3	DTON	Transition Mode after SLEEP Instruction Execution	Transition Mode due to Interrupt	Symbol in Figure 6.1
Active (medium-speed) mode	0	0	0	*	1	Active (high-speed) mode (direct transition)	—	f
	0	1	0	*	1	Active (medium-speed) mode (direct transition)	—	—

Table 6.3 Internal State in Each Operating Mode	122	Note amended

Function		Watch Mode	Subactive Mode	Subsleep Mode	Standby Mode
Peripheral modules	RTC	Functioning/ retained*8	Functioning/ retained*8	Functioning/ retained*8	Functioning/ retained*8
	Asynchronous event counter	Functioning*5	Functioning	Functioning	Functioning*5
	Timer F	Functioning/ retained*6	Functioning/retained*6	Functioning/ retained*6	Retained
	TPU	Retained	Retained	Retained	Retained
	WDT	Functioning*7/ retained	Functioning*7/ retained	Functioning*7/ retained	Functioning*7/ retained
	SCI3/IrDA	Reset	Functioning/ retained*2	Functioning/ retained*2	Reset

Notes:

5. Only incrementing of the external event timer by ECL/ECH and overflow interrupts operate.

6. Functioning if $\phi w/4$ is selected as an internal clock. Halted and retained otherwise.

7. Functioning if the on-chip oscillator is selected.

8. Functioning if the internal time keeping time-base function is selected and retained if the interval timer is selected.

Item	Page	Revision (See Manual for Details)
6.2.5 Subactive Mode	125	Description amended In subactive mode, the system clock oscillator stops but on-chip peripheral modules other than TPU, IIC2, the ΔΣ A/D converter, the A/D converter, and PWM function. The operating frequency of subactive mode is selected from $\phi_w/2$, $\phi_w/4$, and $\phi_w/8$ by the SA1 and SA0 bits in SYSCR2.
6.3 Direct Transition	126	Description amended ... operating frequency modification in active mode. ... If the direct transition interrupt is disabled by IENR2, no direct transition takes place and a transition is made instead to sleep or watch mode. Note: If a direct transition is attempted while the I bit in CCR is set to 1, the device remains in sleep or watch mode, and recovery is not possible.
6.3.1 Direct Transition from Active (High-Speed) Mode to Active (Medium-Speed) Mode	127	Description amended Example: When $\phi_{osc}/8$ is selected as the CPU operating clock following transition Direct transition time = (2 + 1) × 1tosc + 14 × 8tosc = 115tosc
6.3.2 Direct Transition from Active (High-Speed) Mode to Subactive Mode	128	Description amended Example: When ϕosc/8 is selected as the CPU operating clock following transition Direct transition time = (2 + 1) × 1tosc + 14 × 1tsubcyc = 3tosc + 14tsubcyc
6.3.3 Direct Transition from Active (Medium-Speed) Mode to Active (High-Speed) Mode		Description amended Example: When $\phi_{osc}/8$ is selected as the CPU operating clock before transition Direct transition time = (2 + 1) × 8tosc + 14 × 1tosc = 38tosc
6.3.4 Direct Transition from Active (Medium-Speed) Mode to Subactive Mode	129	Description amended Example: When ϕosc/8 is selected as the CPU operating clock before transition Direct transition time = (2 + 1) × 8tosc + 14 × 1tsubcyc = 24tosc + 14tsubcyc
6.3.5 Direct Transition from Subactive Mode to Active (High-Speed) Mode		Description amended Example: When ϕw/8 is selected as the CPU operating clock before transition and wait time = 8192 states Direct transition time = (2 + 1) × 8tw + (8192 + 14) × tosc = 24tw + 8206tosc
6.3.6 Direct Transition from Subactive Mode to Active (Medium-Speed) Mode	130	Description amended Example: When ϕw/8 is selected as the CPU operating clock before transition, $\phi_{osc}/8$ is selected as the CPU operating clock following transition, and the wait time is 8,192 states Direct transition time = (2 + 1) × 8tw + (8192 + 14) × 8tosc = 24tw + 65648tosc

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7.3 On-Board Programming Modes	142	... The boot program transfers the programming control program from the externally-connected host to on-chip RAM via SCI3 (channel 2). ...
7.6 Programmer Mode	153	Description amended ... with the on-chip 64-kbyte flash memory (FZTAT64V3).
7.8 Notes on Setting Module Standby Mode	154	Description amended Even if an interrupt source occurs while the interrupt is enabled in module standby mode, program runaway may occur because the vector cannot be fetched.
9.1.5 Pin Functions	163	Description amended • P15/TIOCB2 pin

TPU Channel 2 Setting	Next table (1)	Next table (2)	Next table (3)		
PCR15	—	0	1	0	1
Pin Function	—	P15 input pin	P15 output pin	P15 input pin	P15 output pin
				TIOCB2 input pin*	

Note: * When the MD1 and MD0 bits are set to B'00 and the IOB3 bit to 1, the pin function becomes the TIOCB2 input pin.
Clear PCR15 to 0 when using TIOCB2 as an input pin.

TPU Channel 2 Setting	(2)	(3)	(1)	
MD1, MD0	B'00			B'10, B'01, B'11
IOB3 to IOB0	B'0000	B'1xxx	B'0001 to B'0111	B'xxxx
CCLR1, CCLR0	B'xx			
Output Function	—		Setting prohibited	

[Legend] x: Don't care.

	164	• P14/TIOCA2/TCLKC pin

Notes: 1. When the MD1 and MD0 bits are set to B'00 and the IOA3 bit to 1, the pin function becomes the TIOCA2 input pin.
Clear PCR14 to 0 when using TIOCA2 as an input pin.
2. When the TPSC2 to TPSC0 bits in TCR_2 are set to B'110, the pin function becomes the TCLKC input pin.
Clear PCR14 to 0 when using TCLKC as an input pin.

TPU Channel 2 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD1, MD0	B'00		B'1x	B'10	B'11	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output Function	—	Output compare output	—	PWM mode 1* output	PWM mode 2 output	—

[Legend] x: Don't care.

Note: * The output of the TIOCB2 pin is disabled.

Item	Page	Revision (See Manual for Details)
9.1.5 Pin Functions	165	Description amended

• P13/TIOCB1/TCLKB pin

TPU Channel 1 Setting	Next table (1)	Next table (2)		Next table (3)	
PCR13	—	0	1	0	1
Pin Function	—	P13 input pin	P13 output pin	P13 input pin	P13 output pin
				TIOCB1 input pin	
		TCLKB input pin*			

Note: * When the TPSC2 to TPSC0 bits in TCR_1 or TCR_2 are set to B'101, the pin function becomes the TCLKB input pin.
Clear PCR13 to 0 when using TCLKB as an input pin.

TPU Channel 1 Setting	(2)	(3)	(1)	
MD1, MD0	B'00			B'10, B'01, B'11
IOB3 to IOB0	B'0000	B'1xxx	B'0001 to B'0111	B'xxxx
CCLR1, CCLR0	B'xx			
Output Function	—		Setting prohibited	

[Legend] x: Don't care.

	166	• P12/TIOCA1/TCLKA pin

Notes: 1. When the MD1 and MD0 bits are set to B'00 and the IOA3 bit to 1, the pin function becomes the TIOCA1 input pin.
Clear PCR12 to 0 when using TIOCA1 as an input pin.
2. When the TPSC2 to TPSC0 bits in TCR_1 or TCR_2 are set to B'100, the pin function becomes the TCLKA input pin.
Clear PCR12 to 0 when using TCLKA as an input pin.

TPU Channel 1 Setting	(2)	(1)	(2)	(1)	(1)	(2)
MD1, MD0	B'00		B'1x	B'10	B'11	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B'xx00	
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output Function	—	Output compare output	—	PWM mode 1* output	PWM mode 2 output	—

[Legend] x: Don't care.

Note: * The output of the TIOCB1 pin is disabled.

Item	Page	Revision (See Manual for Details)
9.2.5 Pin Functions	171	Description amended

• P32/TXD32/SCL pin

The pin function is switched as shown below according to the combination of the PCR32 bit in PCR3, ICE bit in ICRR1, TE bit in SCR32, and SPC32 bit in SPCR.

ICE	0			1
SPC32	0		1	x
TE	x		x	x
PCR32	0	1	x	x
Pin Function	P32 input pin	P32 output pin	TXD32 output pin*	SCL I/O pin

[Legend] x: Don't care.

Note: * If SPC32 is set to 1 and TE is cleared to 0, the mark state is entered and 1 is output from the TXD32 output pin.

• P31/RXD32/SDA pin

The pin function is switched as shown below according to the combination of the PCR31 bit in PCR3, ICE bit in ICCR1, and RE bit in SCR32.

ICE	0			1
RE	0		1	x
PCR31	0	1	x	x
Pin Function	P31 input pin	P31 output pin	RXD32 output pin	SDA I/O pin

[Legend] x: Don't care.

	172	• P30/SCK32/TMOW pin

The pin function is switched as shown below according to the combination of the TMOW bit in PMR3, PCR30 bit in PCR3, CKE1 and CKE0 bits in SCR32, and COM bit in SMR32.

TMOW	0				1
CKE1	0			1	x
CKE0	0		1	x	x
COM	0	1	x	x	x
PCR30	0	1	x	x	x
Pin Function	P30 input pin	P30 output pin	SCK32 output pin	SCK32 input pin	TMOW output pin

[Legend] x: Don't care.

9.3.3 Port Mode Register 4 (PMR4)	175	Description amended

Bit	Bit Name	Initial Value	R/W	Description
0	TMIF	0	R/W	P40/SCK31/TMIF Pin Function Switch Selects whether pin P40/SCK31/TMIF is used as P40/SCK31 or as TMIF. 0: P40/SCK31 I/O pin 1: TMIF input pin

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9.3.4 Pin Functions	176	Description amended

• P42/TXD31/IrTXD/TMOFH pin

TMOFH	0				1
SPC31	0		1		x
TE	x		x		x
IrE	x		0	1	x
PCR42	0	1	x	x	x
Pin Function	P42 input pin	P42 output pin	TXD31 output pin*	IrTXD output pin*	TMOFH output pin

[Legend] x: Don't care.

Note: * If SPC31 is set to 1 and TE is cleared to 0, the mark state is entered, 1 is output from the TXD32 output pin, and 0 is output from the IrTXD pin.

177 • P40/SCK31/TMIF pin

TMIF	0					1
CKE1	0			1		x
CKE0	0		1	0	1	x
COM	0		1	x	x	x
PCR40	0	1	x	x	x	x
Pin Function	P40 input pin	P40 output pin	SCK31 output pin	SCK31 input pin	Setting prohibited	TMIF input pin

[Legend] x: Don't care.

9.8.4 Pin Functions	192	Description amended

• P92/$\overline{\text{IRQ4}}$ pin

IRQ4	0		1	
PCR92	0	1	0	1
Pin Function	P92 input pin	P92 output pin	$\overline{\text{IRQ4}}$ input pin	Setting prohibited

9.9.3 Pin Functions	194, 195	Replaced
9.10.3 Pin Functions	198	Description amended

• PB2/AN2/$\overline{\text{IRQ3}}$ pin

IRQ3	0		1
CH3 to CH0	Other than B'0110	B'0110	x
Pin Function	PB2 input pin	AN2 input pin	$\overline{\text{IRQ3}}$ input pin

[Legend] x: Don't care.

199 • PB1/AN1/$\overline{\text{IRQ1}}$ pin

IRQ1	0		1
CH3 to CH0	Other than B'0101	B'0101	x
Pin Function	PB1 input pin	AN1 input pin	$\overline{\text{IRQ1}}$ input pin

[Legend] x: Don't care.

Item	Page	Revision (See Manual for Details)
9.10.3 Pin Functions	199	Description amended • PB0/AN0/$\overline{\text{IRQ0}}$ pin

IRQ0	0		1
CH3 to CH0	Other than B'0100	B'0100	x
Pin Function	PB0 input pin	AN0 input pin	$\overline{\text{IRQ0}}$ input pin

[Legend] x: Don't care.

9.11.1 Serial Port Control Register (SPCR)	201	Table amended (Before) output data → (After) the output data polarity (Before) input data → (After) the input data polarity
9.12.1 How to Handle Unused Pin	202	Description amended • If an unused pin is an output pin, it is recommended to handle it in one of the following ways: — Set the output of the unused pin to high and pull it up to Vcc with an external resistor of approximately 100 kΩ. — Set the output of the unused pin to low and pull it down to GND with an external resistor of approximately 100 kΩ.
10.3.5 RTC Control Register 1 (RTCCR1)	208	Table amended

Bit	Bit Name	Initial Value	R/W	Description
3	—	0	R/W	Reserved Only 0 can be written to this bit.
2 to 0	—	All 0	—	Reserved These bits are always read as 0.

10.3.7 Clock Source Select Register (RTCCSR)	210	Description amended ... A free running counter controls start/stop of counter operation by the RUN bit in RTCCR1. When a clock other than φw/4 is selected, ...

Bit	Bit Name	Initial Value	R/W	Description
3	RCS3	1	R/W	Clock Source Selection
2	RCS2	0	R/W	0000: φ/8 ····· Free running counter operation
1	RCS1	0	R/W	0001: φ/32 ····· Free running counter operation
0	RCS0	0	R/W	0010: φ/128 ····· Free running counter operation
				0011: φ/256 ····· Free running counter operation
				0100: φ/512 ····· Free running counter operation
				0101: φ/2048 ····· Free running counter operation
				0110: φ/4096 ····· Free running counter operation
				0111: φ/8192 ····· Free running counter operation
				1000: φw/4 ····· RTC operation Settings other than the above are prohibited.

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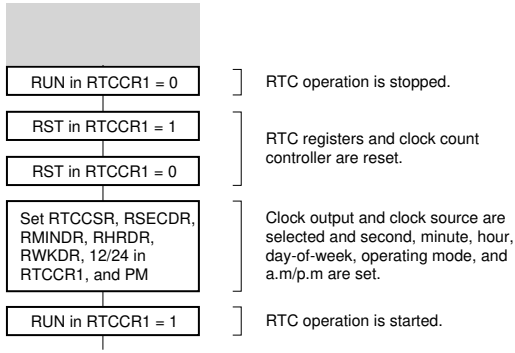
10.4.2 Initial Setting Procedure Figure 10.3 Initial Setting Procedure	212	Figure amended 
10.6.2 Notes on Using Interrupts	215	Added
11.6.1 16-Bit Timer Mode	228	Description amended If an OCRFL write and compare match signal generation occur simultaneously, the compare match signal is invalid. However, a compare match signal may or may not be generated when the written data and the counter value match. ...
11.6.2 8-Bit Timer Mode	228	Description amended (1) TCFH, OCRFH If an OCRFH write and compare match signal generation occur simultaneously, the compare match signal is invalid. However, a compare match signal may or may not be generated when the written data and the counter value match. ...
	229	Description amended (2) TCFL, OCRFL If an OCRFL write and compare match signal generation occur simultaneously, the compare match signal is invalid. However, a compare match signal may or may not be generated when the written data and the counter value match. ...
11.6.3 Flag Clearing	229	Description amended For ST of (1) formula, please substitute the longest number of execution states in used instruction.