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ConnectCore™ 9P 9215, Wi-9P 9215, and 3G 9P 9215

Hardware Reference

90000879_R

Updated on: 5/22/14

Using this Guide

This guide provides information about the Digi ConnectCore 9P 9215 Family of embedded core modules.

Conventions used in this guide

This table describes the typographic conventions used in this guide:

This convention	Is used for
italic type	Emphasis, new terms, variables, and document titles.
monospaced type	Filenames, pathnames, and code examples.

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About the Module

CHAPTER 1

The ConnectCore 9P 9215 Family of modules delivers powerful network-enabled core processor solutions with up to 16 MB of NOR flash, up to 32 MB SDRAM, a rich set of integrated peripherals, and superior design flexibility.

At the heart of the modules is a Digi 32-bit ARM9-based Digi NS9215 processor running at 150 MHz. Key features include 10/100 Mbit Ethernet, two on-chip Flexible Interface Modules (FIMs), 256-bit AES accelerator, power management modes with dynamic clock scaling, and a rich set of on-chip peripherals. Based on Digi 802.11 baseband technology, the ConnectCore Wi-9P 9215 also provides an additional 802.11a/b/g interface with enterprise-grade WPA2/802.11i support.

The ConnectCore 3G 9P 9215 module allows you to instantly add intelligent cellular communication to your products.

Built on leading Qualcomm Gobi 3000 technology, the module delivers a pre-certified embedded cellular connectivity solution without the traditional carrier/network limitations. Selecting cellular network technology and carriers is now a matter of software configuration and service provisioning, any time.

The unique FIMs on the Digi NS9215 processor are two independent 300 MHz DRPIC165X processor cores that allow customers to dynamically select application-specific interfaces in software. The growing list of supported interfaces includes UART, SD/SDIO, CAN bus, USB-device low-speed, 1-Wire®, USB device low-speed, parallel bus interface, and others.

Utilizing the Digi NET+™ ARM processor and secure 802.11a/b/g WLAN technology, the family of ConnectCore 9P 9215 modules offers the industry's only network-enabled core module with true long-term product availability to meet the extended life cycle requirements of embedded product designs.

For further information about the Digi NS9215, see the Digi NS9215 Hardware Reference Manual.

About the Software

The ConnectCore 9P 9215 Family of modules comes in distinct flavors of software: Embedded Development Firmware; or the Digi Plug-and-Play Firmware (ConnectCore Wi-9P 9215 only.)

The Embedded Development Firmware is used for the NET+OS® or Digi Embedded Linux Development systems. These modules require a developer to load system software, compile and debug their applications using the Digi ESP™ Development Environment. In this environment, applications are developed in ANSI C and use the various libraries and services to create custom applications, with resolution down to the device driver.

In the Digi Plug-and-Play Firmware, the firmware is fixed. These modules require either some minor configuration or the loading and launching of Python applications that alter the general behavior of the system. In this environment, fast turn around and minimal development should be expected, however, the level of customization is limited to the Python API and/or the configuration methods.

The information within this chapter is broken down into two sections based on software type. For embedded NET+OS or Digi Embedded Linux users see page 14; for Digi Plug-and-Play Firmware users see page 41.

Digi Embedded Linux and NET+OS

This section describes the features and functionality of modules utilizing embedded NET+OS or Digi Embedded Linux Development Environments only. If you are using a module that utilizes Digi Plug-and-Play Firmware see page 41.

Once you have read through all of the embedded NET+OS / Digi Embedded Linux related sections, proceed to Chapter 2.

Module pinout

The module has two 80 pin connectors, X1 and X2. The following tables describe each pin, its properties, and its use on the Development Board.

Pinout legend: Type

I	Input
O	Output
I/O	Input or output
P	Power

X1 pinout

X1 pin number	Type	Module Functionality	Comments
1	P	GND	
2	P	GND	
3	I	RSTIN#	10k pull-up on module
4	O	SRESET#	Output of the reset controller push pull with 470R current limiting resistor
5	O	RSTOUT#	Output of logical AND function between NS9215 RESET_DONE and NS9215 RESET_OUT#
6	I	TCK	JTAG - 10k pull-up on module
7	I	TMS	JTAG - 10k pull-up on module
8	I	TDI	JTAG - 10k pull-up on module
9	O	TDO	JTAG - 10k pull-up on module
10	I	TRST#	JTAG - 2k2 pull-down on module
11	O	RTCK	JTAG - Optional
12	I	OCD_EN#	10k pull-up on module
13	I	LITTLE# / BIG ENDIAN	2k2 series resistor on module

X1 pin number	Type	Module Functionality	Comments
14	I	WLAN_DISABLE#	Normally connected to X2-15
15	I	SW_CONF0	2k2 series resistor on module
16	I	SW_CONF1	2k2 series resistor on module
17	I	SW_CONF2	2k2 series resistor on module
18	I	SW_CONF3	2k2 series resistor on module
19	O	LED_WWAN#	Reserved
20	P	GND	
21	I/O	BD0	Buffered Data - only active when either CS0# or CS2# is active NS9215 D[31:16]
22	I/O	BD1	
23	I/O	BD2	
24	I/O	BD3	
25	I/O	BD4	
26	I/O	BD5	
27	I/O	BD6	
28	I/O	BD7	
29	I/O	BD8	
30	I/O	BD9	
31	I/O	BD10	
32	I/O	BD11	
33	I/O	BD12	
34	I/O	BD13	
35	I/O	BD14	
36	I/O	BD15	
37	P	GND	
38	O	BAO	Buffered Address always active
39	O	BA1	
40	O	BA2	
41	O	BA3	
42	O	BA4	
43	O	BA5	
44	O	BA6	
45	O	BA7	

X1 pin number	Type	Module Functionality	Comments
46	O	BA8	
47	O	BA9	
48	O	BA10	
49	O	BA11	
50	O	BA12	
51	O	BA13	
52	O	BA14	
53	O	BA15	
54	O	BA16	
55	O	GND	
56	O	EXT_OE#	
57	O	EXT_WE#	
58	O	EXT_CSO#	
59	O	EXT_CS2#	
60	O	BE2#	NS9215 BE2#
61	O	BE3#	NS9215 BE3#
62	I	EXT_WAIT#	10k pull-up on module
63	O	EXT_CLK#	Connected over a 22R resistor to NS9215 CLK_OUT1 pin
64	P	GND	
65	I	ETH_TPIN	
66	O	ETH_ACTIVITY#	Low active signal with 330R resistor on module
67	I	ETH_TPIP	
68	O	ETH_LINK#	Low active signal with 330R resistor on module
69	O	ETH_TPON	
70	O	ETH_TPOP	
71	P	GND	
72	P	USB_VBUS	Power / See Note 1
73	I	USB_OC#	See Note 1
74	I/O	USB_P	See Note 1
75	I/O	USB_N	See Note 1
76	O	USB_PWR#	See Note 1
77	I	Reserved	

X1 pin number	Type	Module Functionality	Comments
78	P	VRTC	Backup Battery for RTC, for 3V cell. Can be left floating, if RTC backup not needed.
79	P	VLIO	Mobile: Power from Li-Ion Battery (2.5V-5.5V) Non-Mobile: connected to 3.3V
80	P	GND	

Note 1: ConnectCore 3G 9P 9215 USB circuit only.

X2 pinout

The following table shows the GPIO multiplexing capabilities for the Embedded Development Firmware module.

X2 pin number	Type	Module Functionality	I/O Multiplexing	Comments
1	P	GND		
2	P	GND		
3	I/O	DCDA# SPI_EN# GPIO0 XBEE_ON_SLEEP#	DCDA# DMA0_DONE PIC_0_GEN_IO[0] GPIO0 SPI_EN	
4	I/O	CTSA# GPIO1	CTSA# EIRQ0 PIC_0_GEN_IO[1] GPIO1	EIRQ0 - Reserved on wireless variant
5	I/O	DSRA# GPIO2 XBEE_RESET#	DSRA# EIRQ1 PIC_0_GEN_IO[2] GPIO2	
6	I/O	RXDA SPI_RXD GPIO3	RXDA DMA0_PDEN PIC_0_GEN_IO[3] GPIO3 SPI_RX	
7	I/O	RIA# ERIQ2 GPIO4	RIA# EIRQ2 Timer6_in GPIO4 SPI_CLK	**Note:** This pin is used to force execution of a backup image for NET+OS, and should not be pulled down at start-up if used with NET+OS.

X2 pin number	Type	Module Functionality	I/O Multiplexing	Comments
8	I/O	RTSA# SPI_CLK GPIO5	RTSA# RS485CTLA EIRQ3 Timer6_Out GPIO5 SPI_CLK	
9	I/O	DTRA# GPIO6 SLEEP_RQ	DTRA# TXCLKA DMA0_REQ Timer7_In GPIO6 PIC_DBG_DATA_OUT	
10	I/O	TXDA SPI_TXD GPIO7	TXDA Timer8_In Timer7_Out GPIO7 SPI_TX	
11	I/O	DCDC# TXCLKC GPIO8	DCDC# DMA1_DONE Timer8_Out GPIO8 SPIB_EN	
12	I/O	CTSC# GPIO9	CTSC# I2C_SCK EIRQ0 GPIO9 PIC_DBG_DATA_IN	EIRQ0 - Reserved on wireless variant
13	I/O	DSRC# GPIO10	DSRC# QDCI EIRQ1 GPIO10 PIC_DBG_CLK	
14	I/O	RXDC GPIO11	RXDC DMA1_DP EIRQ2 GPIO11 SPI_RXboot	

X2 pin number	Type	Module Functionality	I/O Multiplexing	Comments
15	I/O	RIC# RXCLKC GPIO12	RIC# RXCLKC I2C_SDA RST_DONE GPIO12 SPI_CLK	When booting, NS9215 RIC# signal is default configured as Output, RST_DONE. To avoid input/output conflicts, put a series resistor on this signal if necessary.
16	I/O	RTSC# RXCLKC GPIO13	RTSC# QDCQ Ext Timer Event Out Ch 9 GPIO13 SPI_CLKboot	
17	I/O	DTRC# TXCLKC GPIO14	DTRC# TXCLKC DMA1_REQ PIC_0_CAN_RXD GPIO14 SPI_TXDboot	
18	I/O	TXDC GPIO15	TXDC Timer9_In PIC_0_CAN_TXD GPIO15 SPI_ENboot	
19	I/O	DCDB# GPIO51	DCDB# PIC_0_BUS_1[8] PIC_1_BUS_1[8] GPIO51	
20	I/O	CTSB# GPIO52	CTSB# PIC_0_BUS_1[9] PIC_1_BUS_1[9] GPIO52	
21	I/O	DSRB# GPIO53	DSRB# PIC_0_BUS_1[10] PIC_1_BUS_1[10] GPIO53	
22	I/O	RXDB GPIO54	RXDB PIC_0_BUS_1[11] PIC_1_BUS_1[11] GPIO54	

X2 pin number	Type	Module Functionality	I/O Multiplexing	Comments
23	I/O	RIB# GPIO55	RIB# PIC_0_BUS_1[12] PIC_1_BUS_1[12] GPIO55	
24	I/O	RTSB# GPIO56	RTSB# RS485CTLB PIC_0_BUS_1[13] PIC_1_BUS_1[13] GPIO56	
25	I/O	DTRB# GPIO57	TXCLKB DTRB# PIC_0_BUS_1[14] PIC_1_BUS_1[14] GPIO57	
26	I/O	TXDB GPIO58	TXDB PIC_0_BUS_1[15] PIC_1_BUS_1[15] GPIO58	
27	I/O	DCDD# GPIO59	DCDD# PIC_0_BUS_1[16] PIC_1_BUS_1[16] GPIO59	
28	I/O	CTSD# GPIO60	CTSD# PIC_0_BUS_1[17] PIC_1_BUS_1[17] GPIO60	
29	I/O	DSRD# GPIO61	DSRD# PIC_0_BUS_1[18] PIC_1_BUS_1[18] GPIO61	
30	I/O	RXDDD GPIO62	RXDD PIC_0_BUS_1[19] PIC_1_BUS_1[19] GPIO62	
31	I/O	RID# GPIO63	RID# PIC_0_BUS_1[20] PIC_1_BUS_1[20] GPIO63	

X2 pin number	Type	Module Functionality	I/O Multiplexing	Comments
32	I/O	RTSD# GPIO64	RTSD# RS485CTLD PIC_0_BUS_1[21] PIC_1_BUS_1[21] GPIO64	
33	I/O	DTRD# GPIO65	TXCLKD DTRD# PIC_0_BUS_1[22] PIC_1_BUS_1[22] GPIO65	
34	I/O	TXDD GPIO66	TXDD PIC_0_BUS_1[23] PIC_1_BUS_1[23] GPIO66	
35	I/O	GPIO67	PIC_0_CLK[I] PIC_0_CLK[0] EIRQ3 GPIO67	
36	I/O	GPIO68	PIC_0_GEN_IO[0] PIC_1_GEN_IO[0] PIC_1_CAN_RXD GPIO68	
37	I/O	GPIO69	PIC_0_GEN_IO[1] PIC_1_GEN_IO[1] PIC_1_CAN_TXD GPIO69	
38	I/O	GPIO70	PIC_0_GEN_IO[2] PIC_1_GEN_IO[2] PWM0 GPIO70	
39	I/O	GPIO71	PIC_0_GEN_IO[3] PIC_1_GEN_IO[3] PWM1 GPIO71	
40	I/O	GPIO72	PIC_0_GEN_IO[4] PIC_1_GEN_IO[4] PWM2 GPIO72	

X2 pin number	Type	Module Functionality	I/O Multiplexing	Comments
41	I/O	GPIO73	PIC_0_GEN_IO[5] PIC_1_GEN_IO[5] PWM3 GPIO73	
42	I/O	GPIO74	PIC_0_GEN_IO[6] PIC_1_GEN_IO[6] Timer0_In GPIO74	
43	I/O	GPIO75	PIC_0_GEN_IO[7] PIC_1_GEN_IO[7] Timer1_In GPIO75	
44	I/O	GPIO76	PIC_0_CTL_IO[0] PIC_1_CTL_IO[0] Timer2_In GPIO76	
45	I/O	GPIO77	PIC_0_CTL_IO[1] PIC_1_CTL_IO[1] Timer3_In GPIO77	
46	I/O	GPIO78	PIC_0_CTL_IO[2] PIC_1_CTL_IO[2] Timer4_In GPIO78	
47	I/O	GPIO79	PIC_0_CTL_IO[3] PIC_1_CTL_IO[3] Timer5_In GPIO79	
48	I/O	GPIO80	PIC_0_BUS_0[0] PIC_1_BUS_0[0] Timer6_In GPIO80	
49	I/O	USER_BUTTON1# GPIO81	PIC_0_BUS_0[1] PIC_1_BUS_0[1] Timer7_In GPIO81	
50	I/O	USER_LED1# GPIO82	PIC_0_BUS_0[2] PIC_1_BUS_0[2] Timer8_In GPIO82	

X2 pin number	Type	Module Functionality	I/O Multiplexing	Comments
51	I/O	GPIO83	PIC_0_BUS_0[3] PIC_1_BUS_0[3] Timer9_In GPIO83	
52	I/O	USER_BUTTON2# GPIO84	PIC_0_BUS_0[4] PIC_1_BUS_0[4] Timer0_Out GPIO84	
53	I/O	USER_LED2# GPIO85	PIC_0_BUS_0[5] PIC_1_BUS_0[5] Timer1_Out GPIO85	
54	I/O	GPIO86	PIC_0_BUS_0[6] PIC_1_BUS_0[6] Timer2_Out GPIO86	
55	I/O	GPIO87	PIC_0_BUS_0[7] PIC_1_BUS_0[7] Timer3_Out GPIO87	
56	I/O	GPIO93	PIC_0_BUS_0[13] PIC_1_BUS_0[13] Timer9_Out GPIO93	
57	I/O	GPIO94	PIC_0_BUS_0[14] PIC_1_BUS_0[14] QDCI GPIO94	
58	I/O	GPIO95	PIC_0_BUS_0[15] PIC_1_BUS_0[15] QDCQ GPIO95	
59	I/O	CAN0_RXD GPIO96	PIC_0_BUS_1[0] PIC_1_BUS_1[0] PIC_0_CAN_RXD GPIO96	
60	I/O	CAN0_TXD GPIO97	PIC_0_BUS_1[1] PIC_1_BUS_1[1] PIC_0_CAN_TXD GPIO97	

X2 pin number	Type	Module Functionality	I/O Multiplexing	Comments
61	I/O	CAN1_RXD GPIO98	PIC_0_BUS_1[2] PIC_1_BUS_1[2] PIC_1_CAN_RXD GPIO98	
62	I/O	CAN1_TXD GPIO99	PIC_0_BUS_1[3] PIC_1_BUS_1[3] PIC_1_CAN_TXD GPIO99	
63	I/O	GPIO100	PIC_0_BUS_1[4] PIC_1_BUS_1[4] PWM4 GPIO100	
64	I/O	EIRQ3# GPIO101	PIC_0_BUS_1[5] PIC_1_BUS_1[5] EIRQ3 GPIO101	
65	I/O	I2C_SCL GPIO102	PIC_0_BUS_1[6] PIC_1_BUS_1[6] I2C_SCL GPIO102	4k7 pull-up on module
66	I/O	I2C_SDA GPIO103	PIC_0_BUS_1[7] PIC_1_BUS_1[7] I2C_SDA GPIO103	4k7 pull-up on module
67	I	ADC_IN0	VIN0_ADC	
68	I	ADC_IN1	VIN1_ADC	
69	I	ADC_IN2	VIN2_ADC	
70	I	ADC_IN3	VIN3_ADC	
71	I	ADC_IN4	VIN4_ADC	
72	I	ADC_IN5	VIN5_ADC	
73	I	ADC_IN6	VIN6_ADC	
74	I	ADC_IN7	VIN7_ADC	
75	P	VSS_ADC		Connected on module to AGND through 0Ù resistor
76	P	VREF_ADC		100nF decoupling capacitor between VREF_ADC and VSS_ADC
77	P	V_{DD} +3.3V		

X2 pin number	Type	Module Functionality	I/O Multiplexing	Comments
78	P	V_{DD} +3.3V		
79	P	GND		
80	P	GND		

Configuration pins — CPU

None of the 64 GPIO pins on connector X2 disturb CPU boot strap functions. The boot strap functions are controlled by address signals. A user can not disturb boot strap functions from the outside if the module configuration signals, described below, are correctly configured.

Default module CPU configuration

The user has access to six configuration signals:

- LITTLE#/ BIG_ ENDIAN which allows the user to select the endianess of the module
- OCD_EN# which allows the user to activate on-chip debugging
- SW_CONF [3:0] which are reserved for the user; the user software can read out these signals through the GEN ID register (@ 0xA090_0210).

Configuration pins — Module

The ConnectCore 9P 9215 Family of modules support the following JTAG signals: TCK, TMS, TDI, TDO, TRST#, and RTCK. Selection can be made between ARM debug mode and boundary scan mode with the signal OCD_EN#.

Identification of the module

In order to make it easier for software to recognize a module and especially a hardware variant of the module, a specific bit field made of 4 bits has been reserved on the module. This bit field can be read out through GEN ID register and corresponds to A[12:9]. These configuration signals use the internal CPU pull-up resistor and can be pulled down through external population option 2k2 resistors.

In the same way, 3 bits are available on the module to identify the SDRAM configuration scheme. These bits correspond to A[19:17]. It is impossible for the user to disturb either the variant specific or SDRAM configuration specific bits from outside.

In addition, the ConnectCore 9P 9215 Family of modules have reserved 4 bits for special platform identification. This bit field can be read out through GEN ID register and corresponds to A[16:13]. Configuration of these signals is done through the SW_CONF pins. SW_CONF0 is connected to A13 through a 2k2 series resistor, and so on for the further SW_CONF pins. Therefore, this bit can be set high by leaving the