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## High-Speed Quad SPST CMOS Analog Switch

### DESCRIPTION

The DG201HS is an improved monolithic device containing four independent analog switches. It is designed to provide high speed, low error switching of analog signals. Combining low on-resistance (25 Ω) with high speed ( $t_{ON}$ : 38 ns), the DG201HS is ideally suited for high speed data acquisition requirements.

To achieve high voltage ratings and superior switching performance, the DG201HS is built on a proprietary high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages to the supply values, when off.

### FEATURES

- Fast Switching- $t_{ON}$ : 38 ns
- Low On-Resistance: 25 Ω
- Low Leakage: 100 pA
- Low Charge Injection
- TTL/CMOS Logic Compatible
- Single Supply Compatibility
- High Current Rating: - 30 mA

### BENEFITS

- Faster Throughput
- Higher Accuracy
- Reduced Pedestal Error
- Upgrades Existing Designs
- Simple Interfacing
- Replaces HI201HS, ADG201HS
- Space Savings (TSSOP)

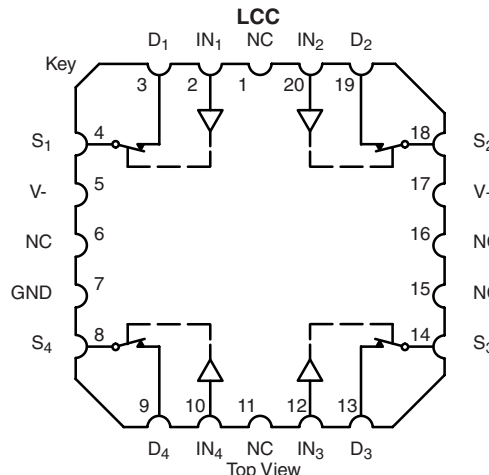
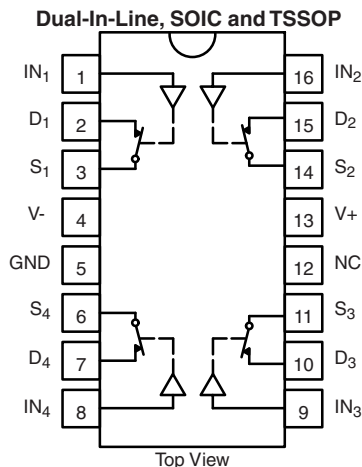
### APPLICATIONS

- Data Acquisition
- Hi-Rel Systems
- Sample-and-Hold Circuits
- Communication Systems
- Automatic Test Equipment
- Integrator Reset Circuits
- Choppers
- Gain Switching
- Avionics



**RoHS\***  
COMPLIANT

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE	
Logic	Switch
0	ON
1	OFF

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V

\* Pb containing terminations are not RoHS compliant, exemptions may apply

## ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 to 85 °C	16-Pin Plastic DIP	DG201HSDJ DG201HSDJ-E3
	16-Pin Narrow SOIC	DG201HSDY DG201HSDY-E3 DG201HSDY-T1 DG201HSDY-T1-E3
	16-Pin TSSOP	DG201HSDQ DG201HSDQ-E3 DG201HSDQ-T1 DG201HSDQ-T1-E3

## ABSOLUTE MAXIMUM RATINGS

Parameter	Limit	Unit	
V+ to V-	44	V	
GND to V-	25		
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>	(V-) - 4 to (V+) + 4 or 30 mA, whichever occurs first		
Continuous Current (Any Terminal)	30	mA	
Current, S or D (Pulsed at 1 ms, 10 % duty cycle)	100		
Storage Temperature	(A Suffix)	- 65 to 150	°C
	(D Suffix)	- 65 to 125	
Power Dissipation (Package) <sup>b</sup>	16-Pin Plastic DIP <sup>c</sup>	470	mW
	16-Pin CerDIP <sup>d</sup>	900	
	16-Pin Narrow Body SOIC and TSSOP <sup>e</sup>	600	
	LCC-20 <sup>d</sup>	900	

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC board.
- Derate 6 mW/°C above 75 °C.
- Derate 12 mW/°C above 75 °C.
- Derate 7.6 mW/°C above 75 °C.

## SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

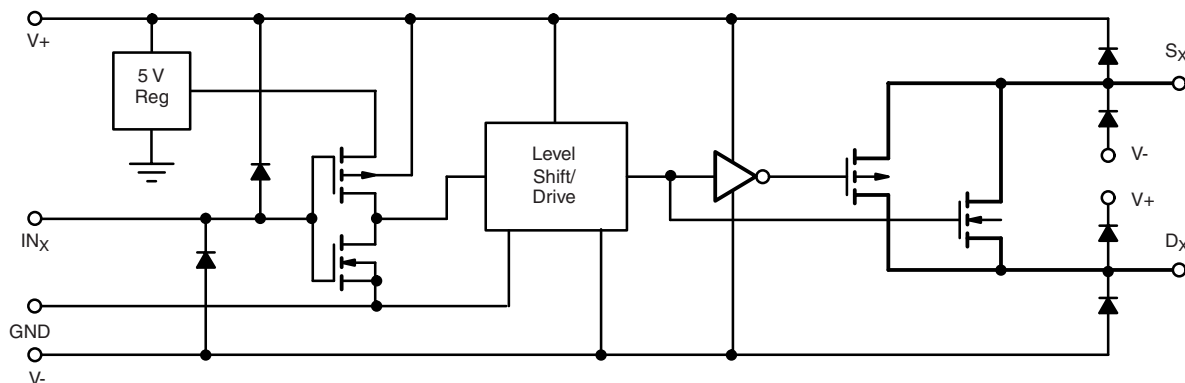


Figure 1.



<b>SPECIFICATIONS<sup>a</sup></b>									
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_{IN} = 3\text{ V}$ , $0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix - 55 to 125 °C		D Suffix - 40 to 85 °C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		V-	V+	V-	V+	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}$ , $V_D = \pm 8.5\text{ V}$ $V_+ = 13.5\text{ V}$ , $V_- = -13.5\text{ V}$	Room Full	25		50 75		50 75	$\Omega$
$r_{DS(on)}$ Match			Room	3					%
Switch Off Leakage Current	$I_{S(off)}$	$V_+ = 16.5\text{ V}$ , $V_- = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}$ $V_S = \pm 15.5\text{ V}$	Room Full	0.1	-1 -60	1 60	-1 -20	1 20	nA
	$I_{D(off)}$		Room Full	0.1	-1 -60	1 60	-1 -20	1 20	
Channel On Leakage Current	$I_{D(on)}$	$V_+ = 16.5\text{ V}$ , $V_- = -16.5\text{ V}$ $V_S = V_D = \pm 15.5\text{ V}$	Room Full	0.1	-1 -60	1 60	-1 -20	1 20	
<b>Digital Control</b>									
Input, High Voltage	$V_{INH}$		Full		2.4		2.4		V
Input, Low Voltage	$V_{INL}$		Full			0.8		0.8	
Input Capacitance	$C_{IN}$		Full	5					pF
Input Current	$I_{INH}$ or $I_{INL}$	$V_{IN}$ under test = 0.8 V, 3 V	Full		-1	1	-1	1	$\mu\text{A}$
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	$R_L = 1\text{ k}\Omega$ , $C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}$ , $V_{INH} = 3\text{ V}$ See Figure 2	Room Full	48		60 75		60 75	ns
Turn-Off Time	$t_{OFF1}$		Room Full	30		50 70		50 70	
	$t_{OFF2}$		Room	150					
Output Settling Time to 0.1 %	$t_s$		Room	180					
Charge Injection	Q	$C_L = 1\text{ nF}$ , $V_S = 0\text{ V}$ $V_{gen} = 0\text{ V}$ , $R_{gen} = 0\text{ }\Omega$	Room	-5					pC
Off Isolation	OIRR	$R_L = 1\text{ k}\Omega$ , $C_L = 10\text{ pF}$ $f = 100\text{ kHz}$	Room	85					dB
Crosstalk (Channel-to-Channel)	$X_{TALK}$	Any Other Channel Switches $R_L = 1\text{ k}\Omega$ , $C_L = 10\text{ pF}$ $f = 100\text{ kHz}$	Room	100					
Source Off Capacitance	$C_{S(off)}$	$V_S$ , $V_D = 0\text{ V}$ , $f = 1\text{ MHz}$	Room	8					pF
Drain Off Capacitance	$C_{D(off)}$		Room	8					
Channel On Capacitance	$C_{D(on)}$		Room	30					
Drain-to-Source Capacitance	$C_{DS(off)}$		Room	0.5					
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_{IN} = 0$ or $5\text{ V}$	Room Full	4.5		10		10	mA
Negative Supply Current	$I_-$		Room Full	3.5	-6		-6		
Power Consumption <sup>c</sup>	$P_C$		Full			240		240	mW

Notes:

- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.

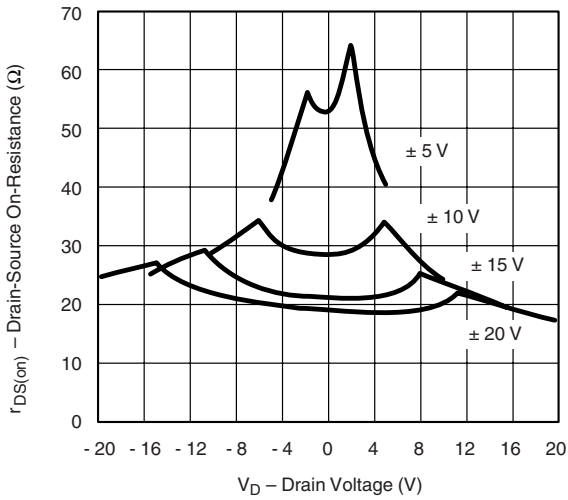
SPECIFICATIONS <sup>a</sup> FOR SINGLE SUPPLY									
Parameter	Symbol	Test Conditions Unless Specified V <sub>+</sub> = 10.8 V to 16.5 V, V <sub>-</sub> = GND = 0 V, V <sub>IN</sub> = 3 V, 0.8 V <sup>f</sup>	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix - 55 to 125 °C		D Suffix - 40 to 85 °C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full		0	V <sub>+</sub>	0	V <sub>+</sub>	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	I <sub>S</sub> = - 10 mA, V <sub>D</sub> = 8.5 V V <sub>+</sub> = 10.8 V	Room Full	65		90 120		90 120	Ω
Switch Off Leakage Current	I <sub>S(off)</sub>	V <sub>+</sub> = 16.5 V V <sub>S</sub> = 0.5 V, 10 V	Room Full	0.1	- 1 - 60	1 60	- 1 - 20	1 20	nA
	I <sub>D(off)</sub>	V <sub>D</sub> = 10 V, 0.5 V	Room Full	0.1	- 1 - 60	1 60	- 1 - 20	1 20	
Channel On Leakage Current	I <sub>D(on)</sub> + I <sub>S(on)</sub>	V <sub>+</sub> = 16.5 V V <sub>D</sub> = 0.5 V, 10 V	Room Full	0.1	- 1 - 60	1 60	- 1 - 20	1 20	
<b>Digital Control</b>									
Input, High Voltage	V <sub>INH</sub>		Full		2.4		2.4		V
Input, Low Voltage	V <sub>INL</sub>		Full			0.8		0.8	
Input Capacitance	C <sub>IN</sub>		Full	5					pF
Input Current	I <sub>INH</sub> or I <sub>INL</sub>	V <sub>+</sub> = 16.5 V V <sub>IN</sub> under test = 0.8 V, 3 V	Full		- 1	1	- 1	1	μA
<b>Dynamic Characteristics</b>									
Turn-On Time	t <sub>ON</sub>	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF V <sub>S</sub> = 2 V, V = 10.8 V See Figure 2	Room Full			50 70		50 70	ns
Turn-Off Time	t <sub>OFF1</sub>		Room Full			50 70		50 70	
	t <sub>OFF2</sub>		Room	150					
Output Settling Time to 0.1 %	t <sub>s</sub>		Room	180					
Charge Injection	Q	C <sub>L</sub> = 1 nF, V <sub>S</sub> = 0 V V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω	Room	10					pC
Off Isolation	OIRR	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 10 pF f = 100 kHz	Room	85					
Crosstalk (Channel-to-Channel)	X <sub>TALK</sub>	Any Other Channel Switches R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 10 pF f = 100 kHz	Room	100					dB
Source Off Capacitance	C <sub>S(off)</sub>	f = 1 MHz	Room	10					pF
Drain Off Capacitance	C <sub>D(off)</sub>		Room	10					
Channel On Capacitance	C <sub>D(on)</sub>		V <sub>ANALOG</sub> = 0 V	Room	30				
<b>Power Supply</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 15 V, V <sub>IN</sub> = 0 or 5 V	Full			10		10	mA
Power Consumption <sup>c</sup>	P <sub>C</sub>		Full			150		150	mW

Notes:

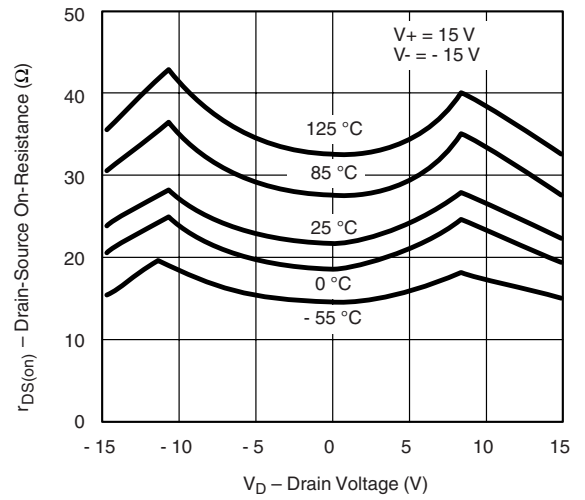
- Refer to PROCESS OPTION FLOWCHART.
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- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V<sub>IN</sub> = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

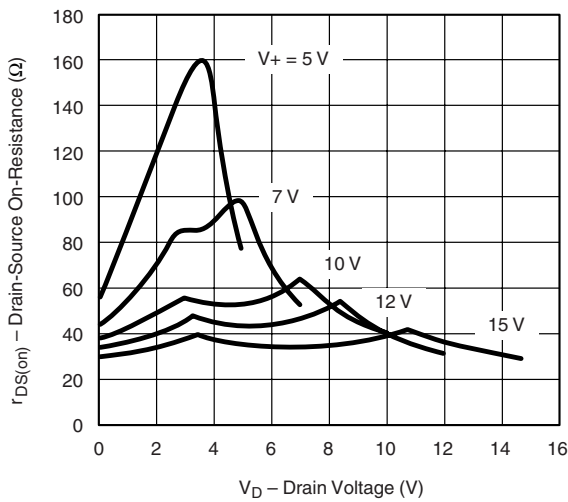
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



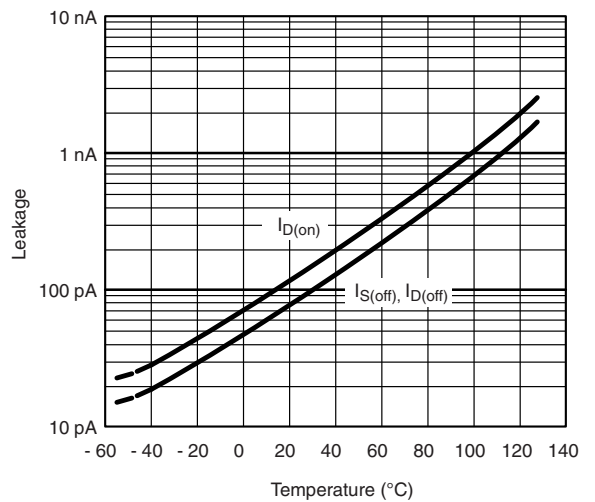
$r_{DS(on)}$  vs.  $V_D$  and Power Supply Voltages



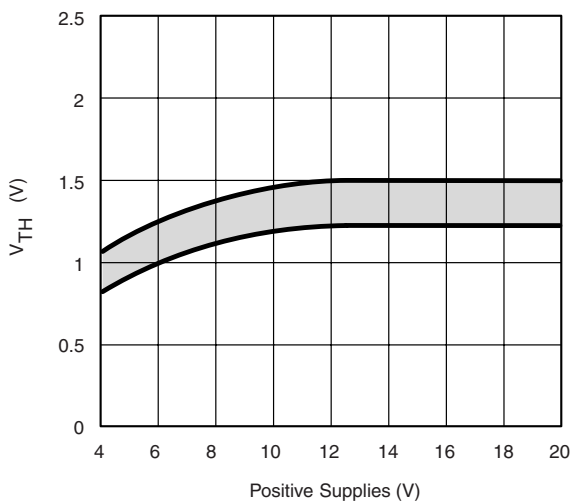
$r_{DS(on)}$  vs.  $V_D$  and Temperature



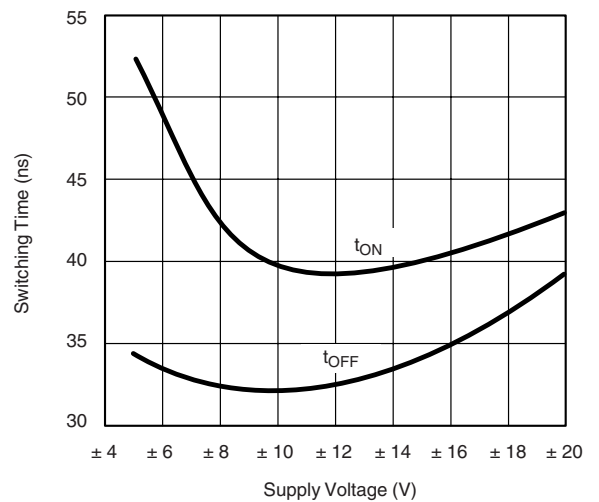
$r_{DS(on)}$  vs.  $V_D$  and Single Power Supply Voltages



Leakage Currents vs. Temperature

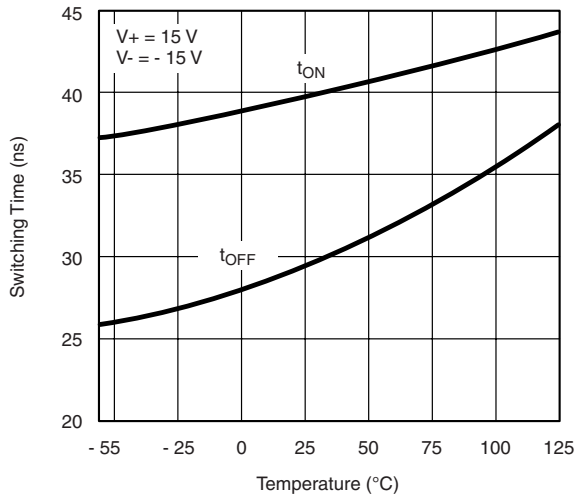


Input Switching Threshold vs. Supply Voltage

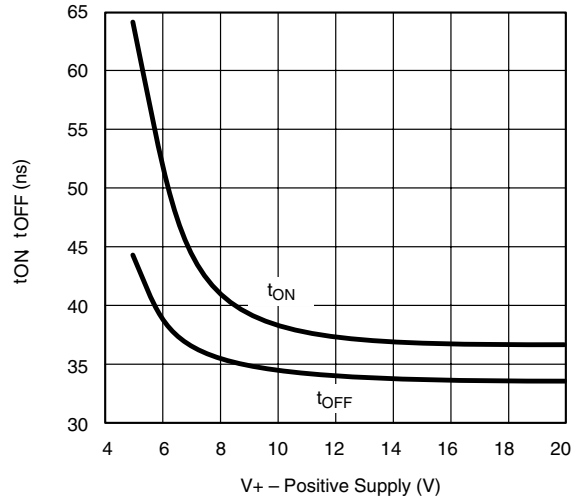


Switching Time vs. Power Supply Voltage

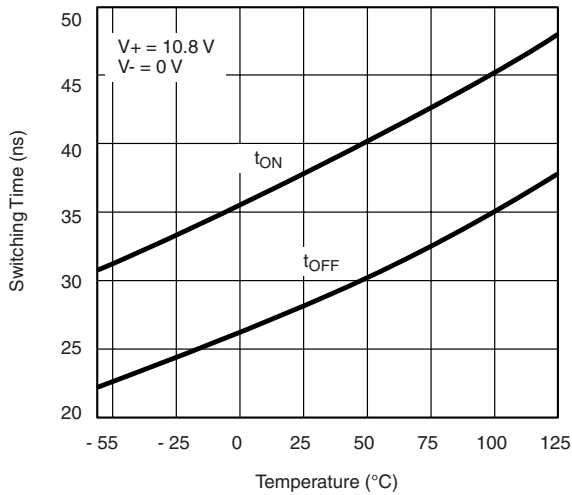
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



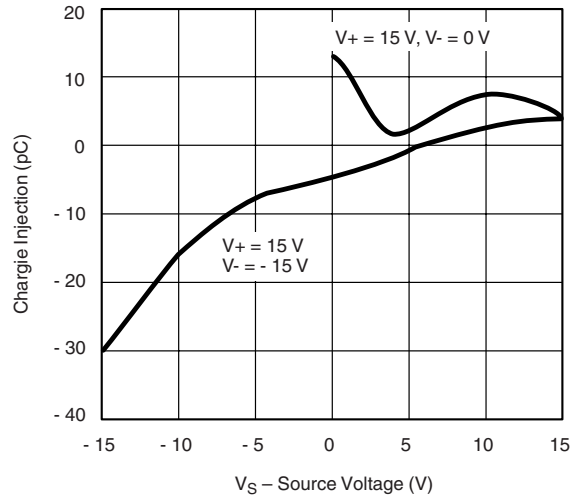
**Switching Times vs. Temperature**



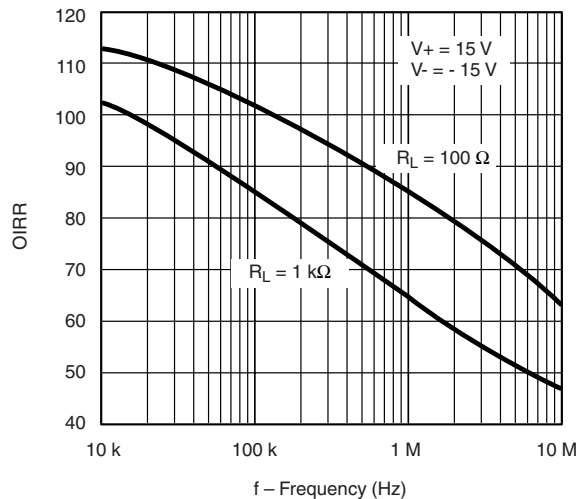
**Switching Times vs. Power Supply Voltage**



**Switching Times vs. Temperature**

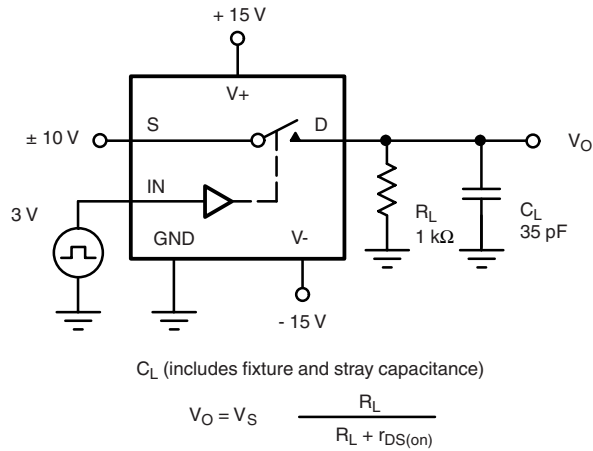


**Charge Injection vs. Source Voltage**

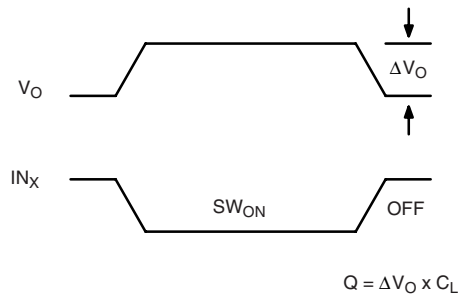
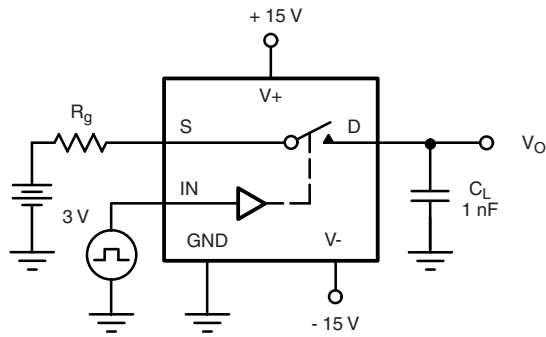
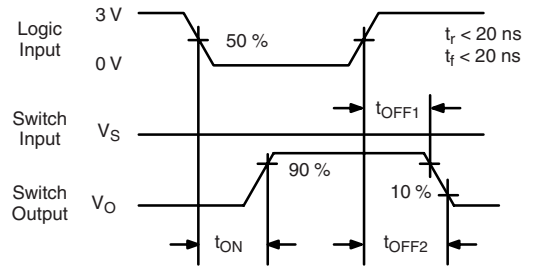


**Off Isolation vs. Frequency**

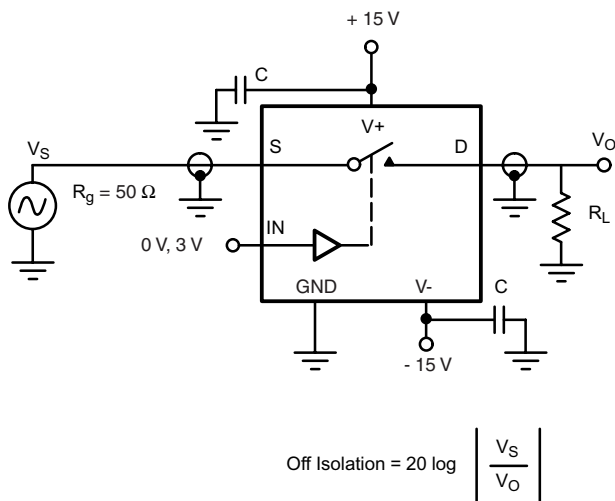
**TEST CIRCUITS**



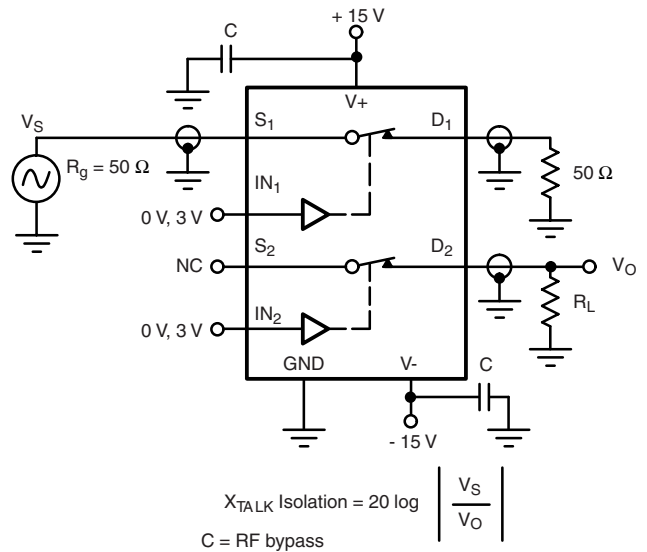
**Figure 2. Switching Time**



**Figure 3. Charge Injection**



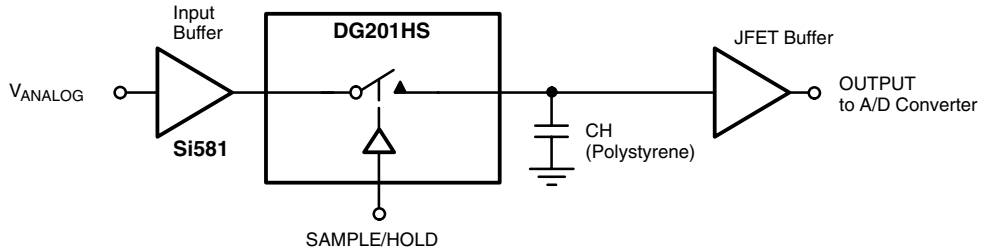
**Figure 4. Off Isolation**



**Figure 5. Crosstalk**

### APPLICATIONS

A high-speed, low-glitch analog switch such as Vishay Siliconix's DG201HS improves the accuracy and shortens the acquisition and settling times of a sample-and-hold circuit.



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?70038>.



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