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High-Speed, Low-Glitch D/CMOS Analog Switches

DESCRIPTION

The DG611, DG612, DG613 feature high-speed low-capacitance lateral DMOS switches. Charge injection has been minimized to optimize performance in fast sample-and-hold applications.

Each switch conducts equally well in both directions when on and blocks up to 16 V_{p-p} when off. Capacitances have been minimized to ensure fast switching and low-glitch energy. To achieve such fast and clean switching performance, the DG611, DG612, DG613 are built on the Vishay Siliconix proprietary D/CMOS process. This process combines n-channel DMOS switching FETs with low-power CMOS control logic and drivers. An epitaxial layer prevents latchup.

The DG611 and DG612 differ only in that they respond to opposite logic levels. The versatile DG613 has two normally open and two normally closed switches. It can be given various configurations, including four SPST, two SPDT, one DPDT.

For additional information see Applications Note AN207.

FEATURES

- Fast switching - t_{ON}: 12 ns
- Low charge injection: ± 2 pC
- Wide bandwidth: 500 MHz
- 5 V CMOS logic compatible
- Low R_{DS(on)}: 18 Ω
- Low quiescent power : 1.2 nW
- Single supply operation

BENEFITS

- Improved data throughput
- Minimal switching transients
- Improved system performance
- Easily interfaced
- Low insertion loss
- Minimal power consumption

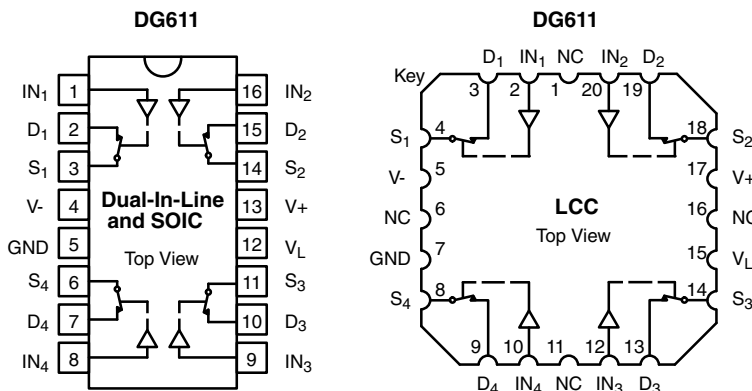
APPLICATIONS

- Fast sample-and-holds
- Synchronous demodulators
- Pixel-rate video switching
- Disk/tape drives
- DAC deglitching
- Switched capacitor filters
- GaAs FET drivers
- Satellite receivers



Available
RoHS*
COMPLIANT

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



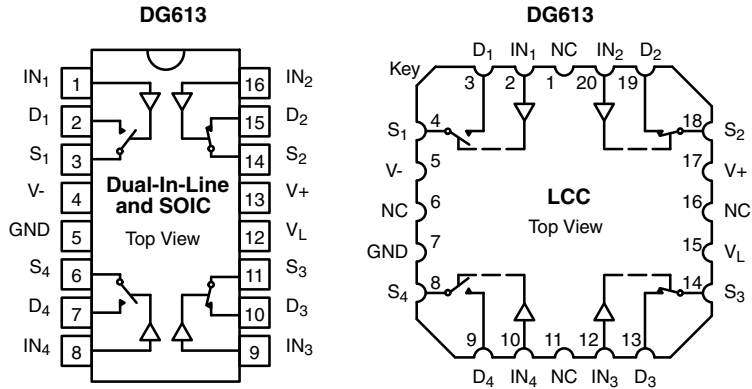
Four SPST Switches per Package

| TRUTH TABLE | | |
|-------------|-------|-------|
| Logic | DG611 | DG612 |
| 0 | ON | OFF |
| 1 | OFF | ON |

Logic "0" ≤ 1 V
Logic "1" ≥ 4 V

* Pb containing terminations are not RoHS compliant, exemptions may apply

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Four SPST Switches per Package

| TRUTH TABLE | | |
|-------------|-----------------------------------|-----------------------------------|
| Logic | SW ₁ , SW ₄ | SW ₂ , SW ₃ |
| 0 | OFF | ON |
| 1 | ON | OFF |

Logic "0" ≤ 1 V
Logic "1" ≥ 4 V

| ORDERING INFORMATION | | |
|----------------------|--------------------|--|
| Temp. Range | Package | Part Number |
| DG611, DG612 | | |
| - 40 °C to 85 °C | 16-Pin Plastic DIP | DG611DJ DG611DJ-E3 |
| | | DG612DJ DG612DJ-E3 |
| | 16-Pin Narrow SOIC | DG611DY DG611DY-E3 DG611DY-T1 DG611DY-T1-E3 |
| | | DG612DY DG612DY-E3 DG612DY-T1 DG612DY-T1-E3 |
| DG613 | | |
| - 40 °C to 85 °C | 16-Pin Plastic DIP | DG613DJ DG613DJ-E3 |
| | 16-Pin Narrow SOIC | DG613DY DG613DY-E3 DG613DY-T1 DG613DY-T1-E3 |



| ABSOLUTE MAXIMUM RATINGS | | | |
|---|---|-------------|-------------|
| Parameter | Limit | Unit | |
| V+ to V- | - 0.3 to 21 | V | |
| V+ to GND | - 0.3 to 21 | | |
| V- to GND | - 19 to 0.3 | | |
| V _L to GND | - 1 to (V+) + 1 or 20 mA, whichever occurs first | | |
| V _{IN} ^a | (V-) - 1 to (V+) + 1 or 20 mA, whichever occurs first | | |
| V _S , V _D ^a | (V-) - 0.3 to (V+) + 16 or 20 mA, whichever occurs first | mA | |
| Continuous Current (Any Terminal) | ± 30 | | |
| Current, S or D (Pulsed at 1 μs, 10 % Duty Cycle) | ± 100 | °C | |
| Storage Temperature | CerDIP | | - 65 to 150 |
| | Plastic | - 65 to 125 | |
| Power Dissipation (Package) ^b | 16-Pin Plastic DIP ^c | 470 | mW |
| | 16-Pin Narrow SOIC ^d | 600 | |
| | 16-Pin CerDIP ^e | 900 | |
| | 20-Pin LCC ^e | 900 | |

Notes:

- a. Signals on S_x, D_x, or IN_x exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 6 mW/°C above 75 °C.
- d. Derate 7.6 mW/°C above 75 °C.
- e. Derate 12 mW/°C above 75 °C.

| RECOMMENDED OPERATING RANGE | | |
|-----------------------------|---------------------|------|
| Parameter | Limit | Unit |
| V+ | 5 to 21 | V |
| V- | - 10 to 0 | |
| V _L | 4 to V+ | |
| V _{IN} | 0 to V _L | |
| V _{ANALOG} | V- to (V+) - 5 | |

| SPECIFICATIONS ^a | | | | | | | | | |
|-------------------------------------|----------------------|--|--------------------|-------------------|------------------------------|-------------------|-----------------------------|-------------------|------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified V ₊ = 15 V, V ₋ = -3 V V _L = 5 V, V _{IN} = 4 V, 1 V ^f | Temp. ^b | Typ. ^c | A Suffix -55 °C to 125 °C | | D Suffix -40 °C to 85 °C | | Unit |
| | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Analog Switch | | | | | | | | | |
| Analog Signal Range ^e | V _{ANALOG} | V ₋ = -5 V, V ₊ = 12 V | Full | | -5 | 7 | -5 | 7 | V |
| Switch On-Resistance | R _{DS(on)} | I _S = -1 mA, V _D = 0 V | Room Full | 18 | | 45 60 | | 45 60 | Ω |
| Resistance Match Bet Ch. | ΔR _{DS(on)} | | Room | 2 | | | | | |
| Source Off Leakage | I _{S(off)} | V _S = 0 V, V _D = 10 V | Room Hot | ± 0.001 | -0.25 -20 | 0.25 20 | -0.25 -20 | 0.25 20 | nA |
| Drain Off Leakage Current | I _{D(off)} | V _S = 10 V, V _D = 0 V | Room Hot | ± 0.001 | -0.25 -20 | 0.25 20 | -0.25 -20 | 0.25 20 | |
| Switch On Leakage Current | I _{D(on)} | V _S = V _D = 0 V | Room Hot | ± 0.001 | -0.4 -40 | 0.4 40 | -0.4 -40 | 0.4 40 | |
| Digital Control | | | | | | | | | |
| Input Voltage High | V _{IH} | | Full | | 4 | | 4 | | V |
| Input Voltage Low | V _{IL} | | Full | | | 1 | | 1 | |
| Input Current | I _{IN} | | Room Hot | 0.005 | -1 -20 | 1 20 | -1 -20 | 1 20 | μA |
| Input Capacitance | C _{IN} | | Room | 5 | | | | | pF |
| Dynamic Characteristics | | | | | | | | | |
| Off State Input Capacitance | C _{S(off)} | V _S = 0 V | Room | 3 | | | | | pF |
| Off State Output Capacitance | C _{D(off)} | V _D = 0 V | Room | 2 | | | | | |
| On State Input Capacitance | C _{S(on)} | V _S = V _D = 0 V | Room | 10 | | | | | |
| Bandwidth | BW | R _L = 50 Ω | Room | 500 | | | | | MHz |
| Turn-On Time ^e | t _{ON} | R _L = 300 Ω, C _L = 3 pF V _S = ± 2 V, See test circuit, figure 2 | Room | 12 | | 25 | | 25 | ns |
| Turn-Off Time ^e | t _{OFF} | | Room | 8 | | 20 | | 20 | |
| Turn-On Time | t _{ON} | R _L = 300 Ω, C _L = 75 pF V _S = ± 2 V, See test circuit, figure 2 | Room Full | 19 | | 35 50 | | 35 50 | |
| Turn-Off Time | t _{OFF} | | Room Full | 16 | | 25 35 | | 25 35 | |
| Charge Injection ^e | Q | C _L = 1 nF, V _S = 0 V | Room | 4 | | | | | pC |
| Ch. Injection Change ^{e,g} | ΔQ | C _L = 1 nF, V _S ≤ 3 V | Room | 3 | | 4 | | 4 | |
| Off Isolation ^e | OIRR | R _{IN} = 50 Ω, R _L = 50 Ω f = 5 MHz | Room | 74 | | | | | dB |
| Crosstalk ^e | X _{TALK} | R _{IN} = 10 Ω, R _L = 50 Ω f = 5 MHz | Room | 87 | | | | | |
| Power Supplies | | | | | | | | | |
| Positive Supply Current | I ₊ | V _{IN} = 0 V or 5 V | Room Full | 0.005 | | 1 5 | | 1 5 | μA |
| Negative Supply Current | I ₋ | | Room Full | -0.005 | -1 -5 | | -1 -5 | | |
| Logic Supply Current | I _L | | Room Full | 0.005 | | 1 5 | | 1 5 | |
| Ground Current | I _{GND} | | Room Full | -0.005 | -1 -5 | | -1 -5 | | |

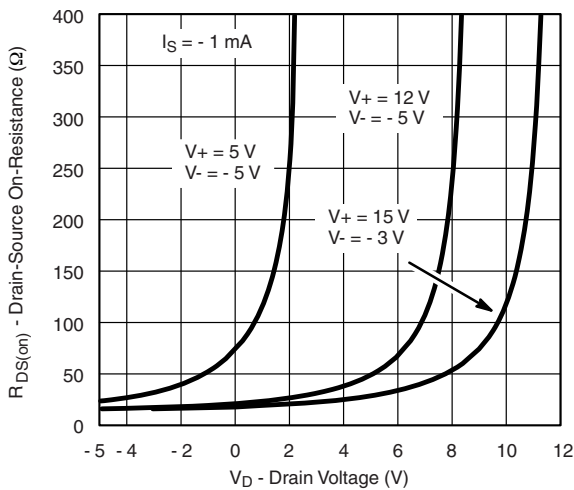
| SPECIFICATIONS FOR UNIPOLAR SUPPLIES ^a | | | | | | | | | |
|---|--------------|---|--------------------|-------------------|------------------------------|-------------------|-----------------------------|-------------------|----------|
| Parameter | Symbol | Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$, $V_- = -3\text{ V}$ $V_L = 5\text{ V}$, $V_{IN} = 4\text{ V}$, 1 V^f | Temp. ^b | Ty.p ^c | A Suffix -55 °C to 125 °C | | D Suffix -40 °C to 85 °C | | Unit |
| | | | | | Min. ^d | Max. ^d | Min. ^d | Max. ^d | |
| Analog Switch | | | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | | 0 | 7 | 0 | 7 | V |
| Switch On-Resistance | $R_{DS(on)}$ | $I_S = -1\text{ mA}$, $V_D = 1\text{ V}$ | Room | 25 | | 60 | | 60 | Ω |
| Dynamic Characteristics | | | | | | | | | |
| Turn-On Time ^e | t_{ON} | $R_L = 300\ \Omega$, $C_L = 3\text{ pF}$ $V_S = 2\text{ V}$, See test circuit, figure 2 | Room | 15 | | 30 | | 30 | ns |
| Turn-Off Time ^e | t_{OFF} | | Room | 10 | | 25 | | 25 | |

Notes:

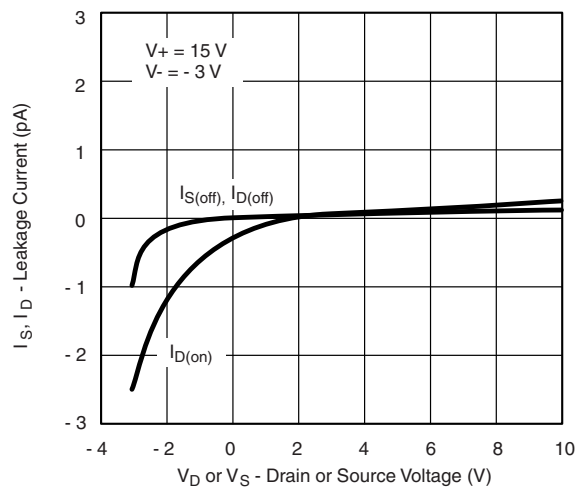
- Refer to PROCESS OPTION FLOWCHART.
- Room = 25 °C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.
- $\Delta Q = |Q \text{ at } V_S = 3\text{ V} - Q \text{ at } V_S = -3\text{ V}|$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

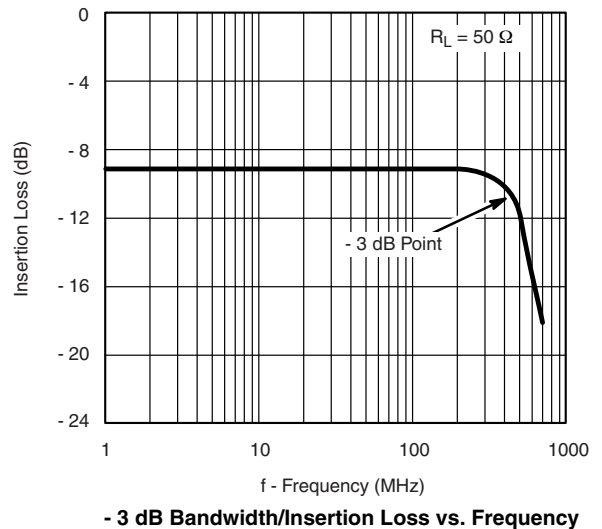
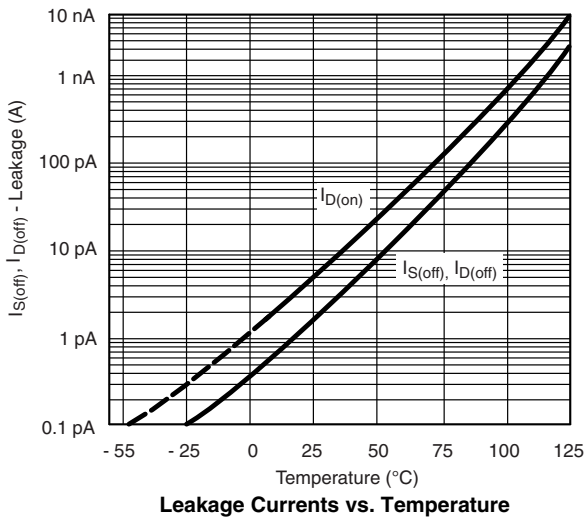
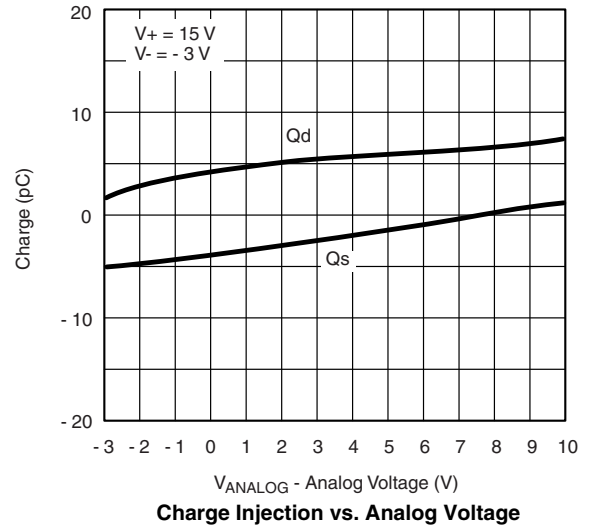
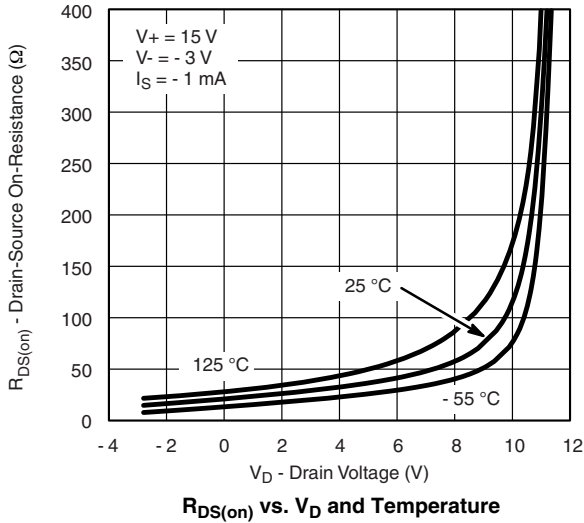
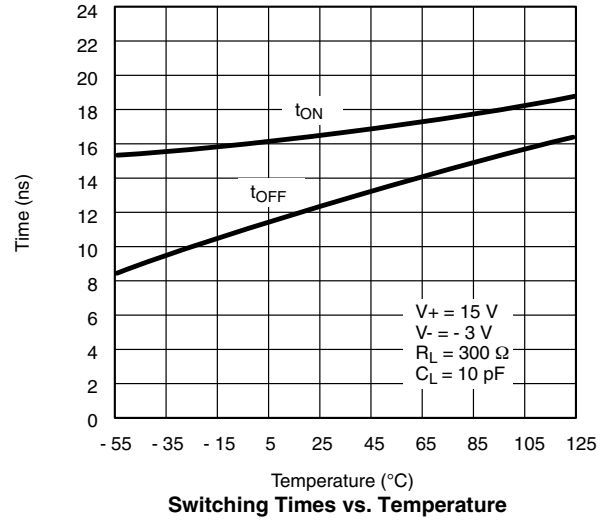
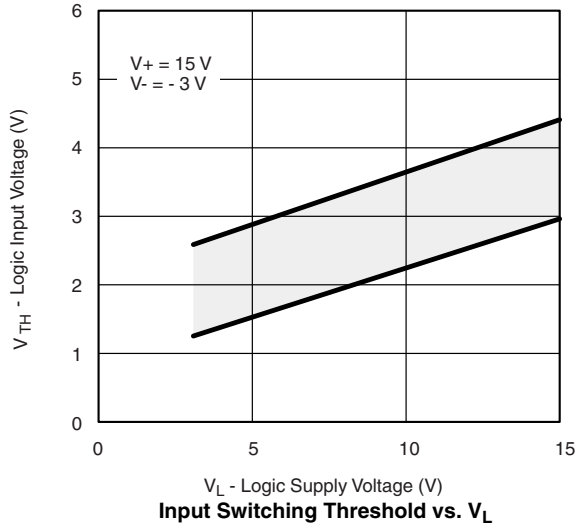


$R_{DS(on)}$ vs. V_D and Power Supply Voltages

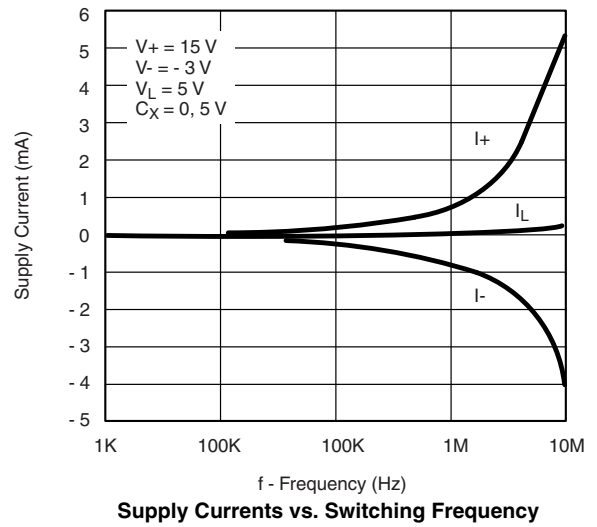
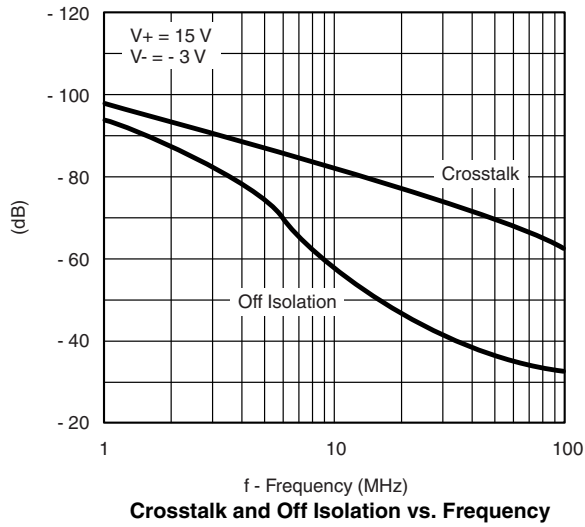


Leakage Current vs. Analog Voltage

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



SCHEMATIC DIAGRAM (Typical Channel)

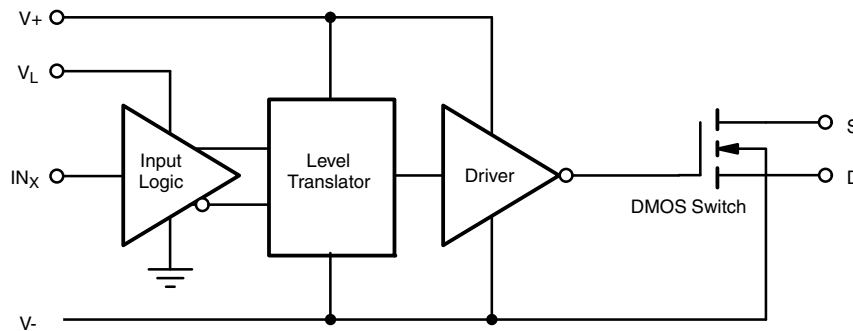


Figure 1.

TEST CIRCUITS

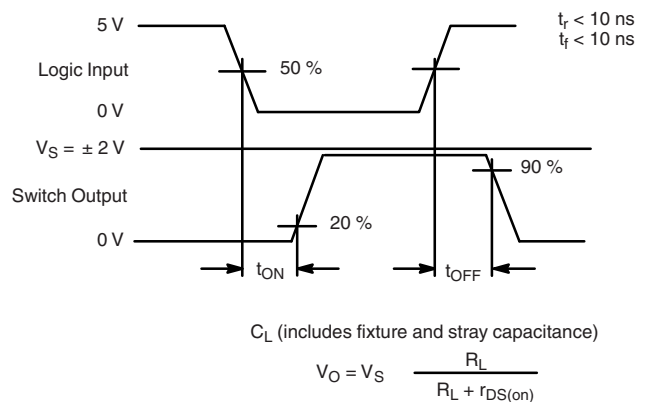
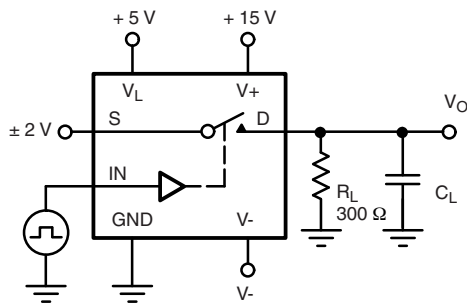


Figure 2. Switching Time

TEST CIRCUITS

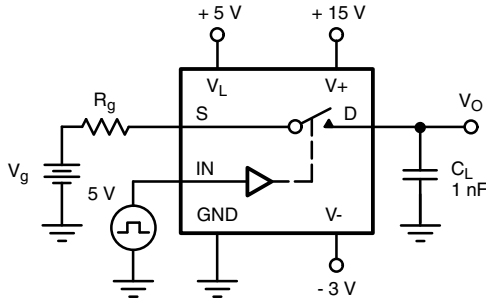


Figure 3. Charge Injection

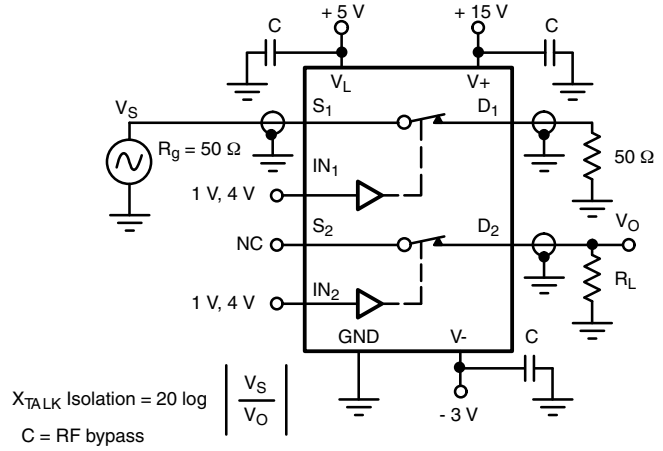


Figure 4. Crosstalk

APPLICATIONS

High-Speed Sample-and-Hold

In a fast sample-and-hold application, the analog switch characteristics are critical. A fast switch reduces aperture uncertainty. A low charge injection eliminates offset (step) errors. A low leakage reduces droop errors. The CLC111, a fast input buffer, helps to shorten acquisition and settling times. A low leakage, low dielectric absorption hold capacitor must be used. Polycarbonate, polystyrene and polypropylene are good choices. The JFET output buffer reduces droop due to its low input bias current. (see figure 5.)

Pixel-Rate Switch

Windows, picture-in-picture, title overlays are economically generated using a high-speed analog switch such as the DG613. For this application the two video sources must be sync locked. The glitch-less analog switch eliminates halos. (see figure 6.)

GaAs FET Drivers

Figure 7 illustrates a high-speed GaAs FET driver. To turn the GaAs FET on 0 V are applied to its gate via S₁, whereas to turn it off, - 8 V are applied via S₂. This high-speed, low-power driver is especially suited for applications that require a large number of RF switches, such as phased array radars.

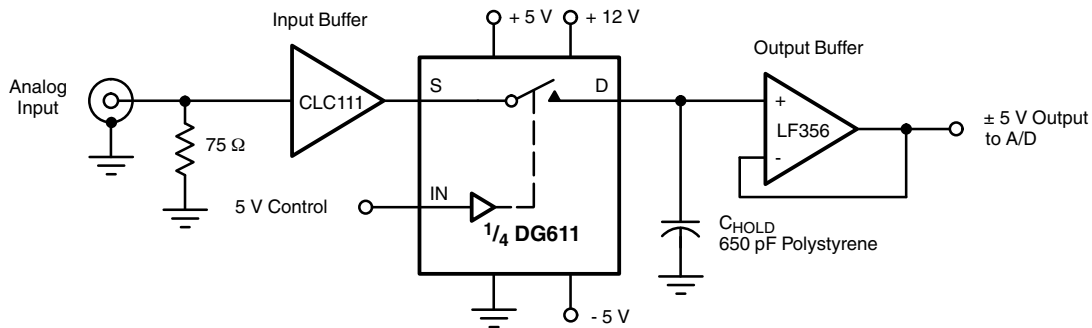


Figure 5. High-Speed Sample-and-Hold

APPLICATIONS

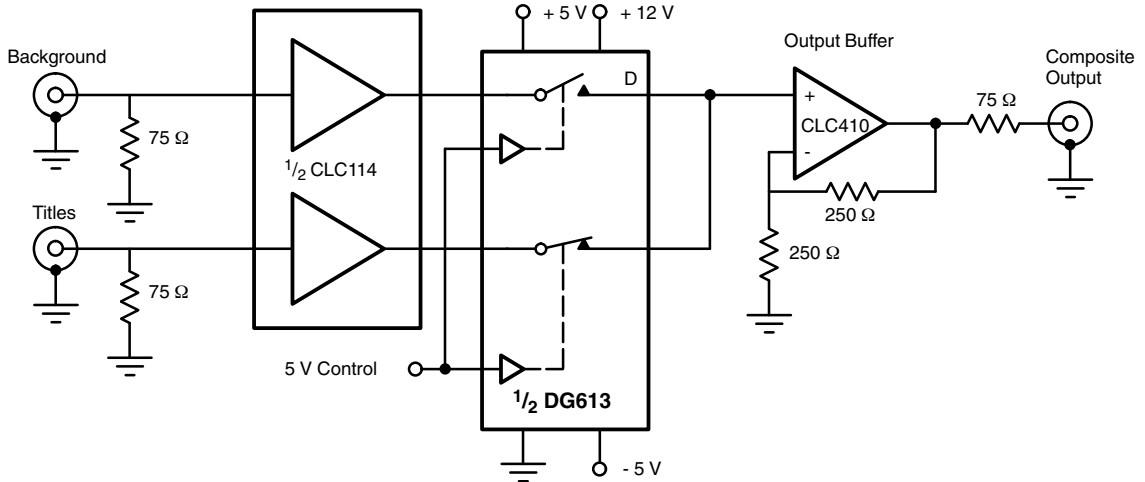


Figure 6. A Pixel-Rate Switch Creates Title Overlays

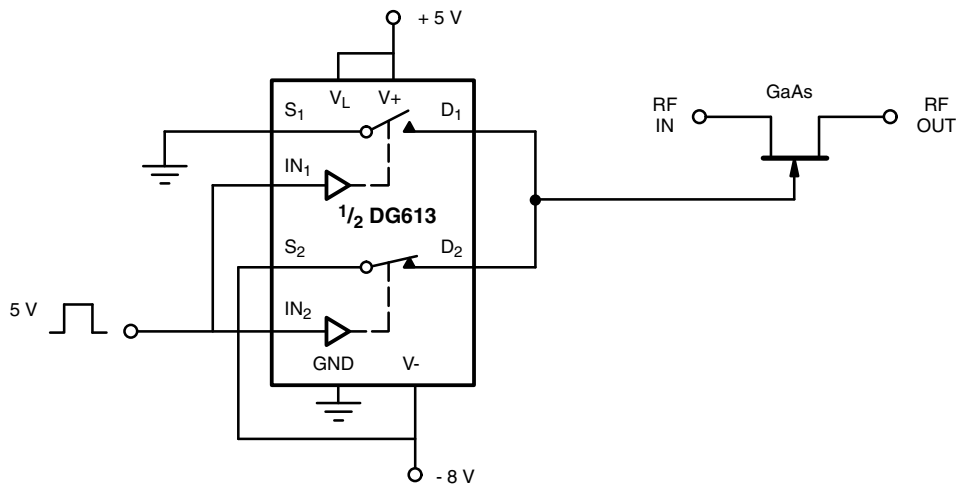
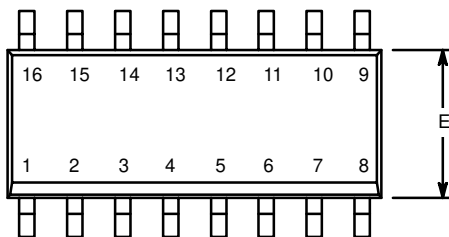


Figure 7. A High-Speed GaAs FET Driver that Saves Power

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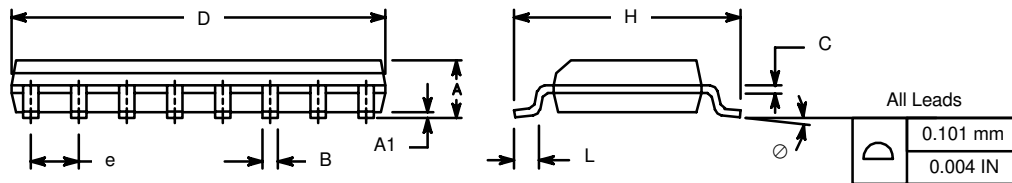


SOIC (NARROW): 16-LEAD
JEDEC Part Number: MS-012

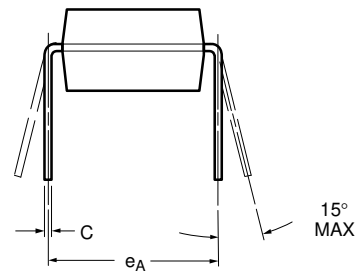
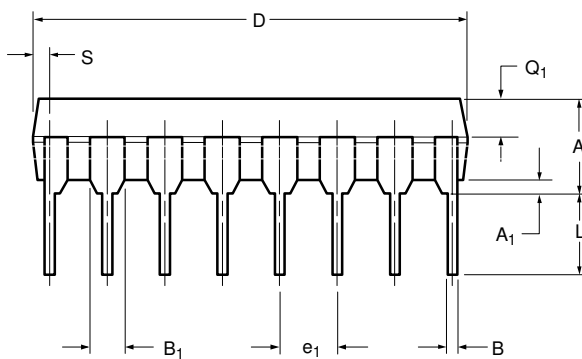
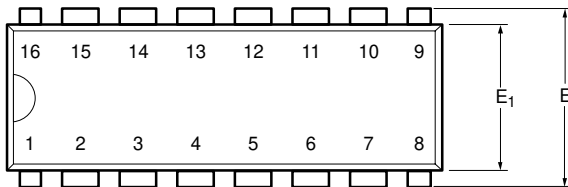


| Dim | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A ₁ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| C | 0.18 | 0.23 | 0.007 | 0.009 |
| D | 9.80 | 10.00 | 0.385 | 0.393 |
| E | 3.80 | 4.00 | 0.149 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| ∅ | 0° | 8° | 0° | 8° |

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



PDIP: 16-LEAD

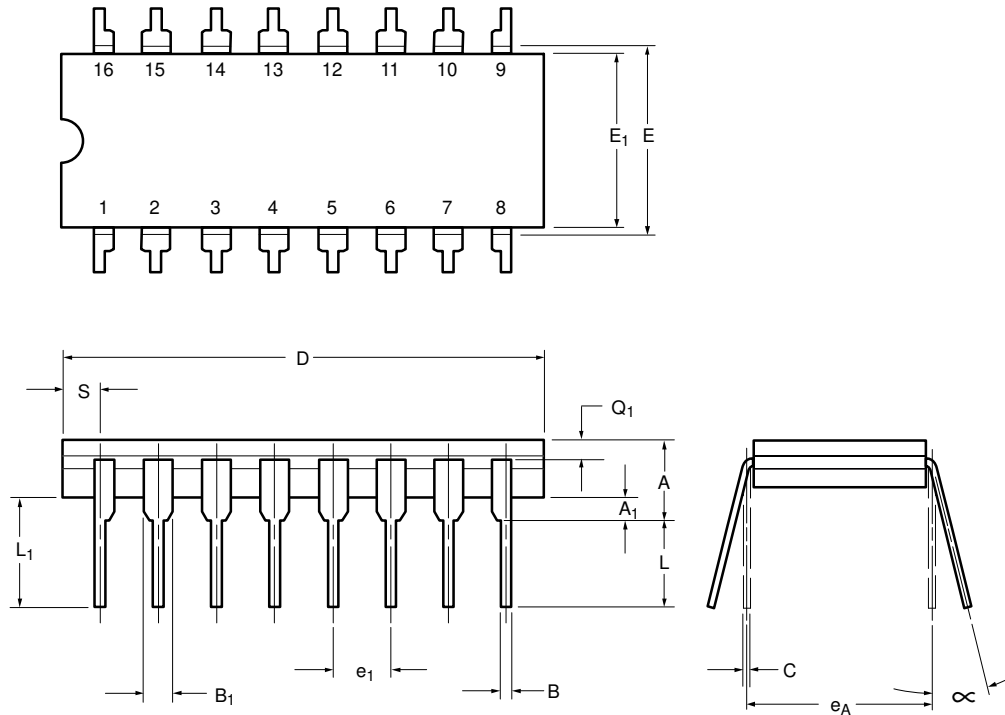


| Dim | MILLIMETERS | | INCHES | |
|----------------------|-------------|-------|--------|-------|
| | Min | Max | Min | Max |
| A | 3.81 | 5.08 | 0.150 | 0.200 |
| A₁ | 0.38 | 1.27 | 0.015 | 0.050 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| B₁ | 0.89 | 1.65 | 0.035 | 0.065 |
| C | 0.20 | 0.30 | 0.008 | 0.012 |
| D | 18.93 | 21.33 | 0.745 | 0.840 |
| E | 7.62 | 8.26 | 0.300 | 0.325 |
| E₁ | 5.59 | 7.11 | 0.220 | 0.280 |
| e₁ | 2.29 | 2.79 | 0.090 | 0.110 |
| e_A | 7.37 | 7.87 | 0.290 | 0.310 |
| L | 2.79 | 3.81 | 0.110 | 0.150 |
| Q₁ | 1.27 | 2.03 | 0.050 | 0.080 |
| S | 0.38 | 1.52 | .015 | 0.060 |

ECN: S-03946—Rev. D, 09-Jul-01
DWG: 5482



CERDIP: 16-LEAD

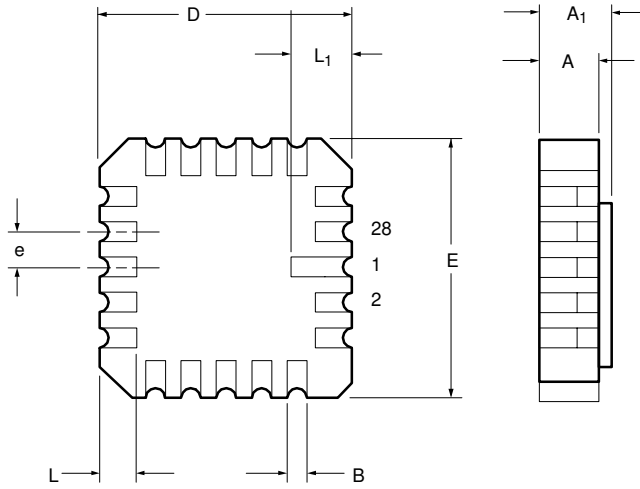


| Dim | MILLIMETERS | | INCHES | |
|----------------------|-------------|-------|-----------|-------|
| | Min | Max | Min | Max |
| A | 4.06 | 5.08 | 0.160 | 0.200 |
| A₁ | 0.51 | 1.14 | 0.020 | 0.045 |
| B | 0.38 | 0.51 | 0.015 | 0.020 |
| B₁ | 1.14 | 1.65 | 0.045 | 0.065 |
| C | 0.20 | 0.30 | 0.008 | 0.012 |
| D | 19.05 | 19.56 | 0.750 | 0.770 |
| E | 7.62 | 8.26 | 0.300 | 0.325 |
| E₁ | 6.60 | 7.62 | 0.260 | 0.300 |
| e₁ | 2.54 BSC | | 0.100 BSC | |
| e_A | 7.62 BSC | | 0.300 BSC | |
| L | 3.18 | 3.81 | 0.125 | 0.150 |
| L₁ | 3.81 | 5.08 | 0.150 | 0.200 |
| Q₁ | 1.27 | 2.16 | 0.050 | 0.085 |
| S | 0.38 | 1.14 | 0.015 | 0.045 |
| ∞ | 0° | 15° | 0° | 15° |

ECN: S-03946—Rev. G, 09-Jul-01
DWG: 5403



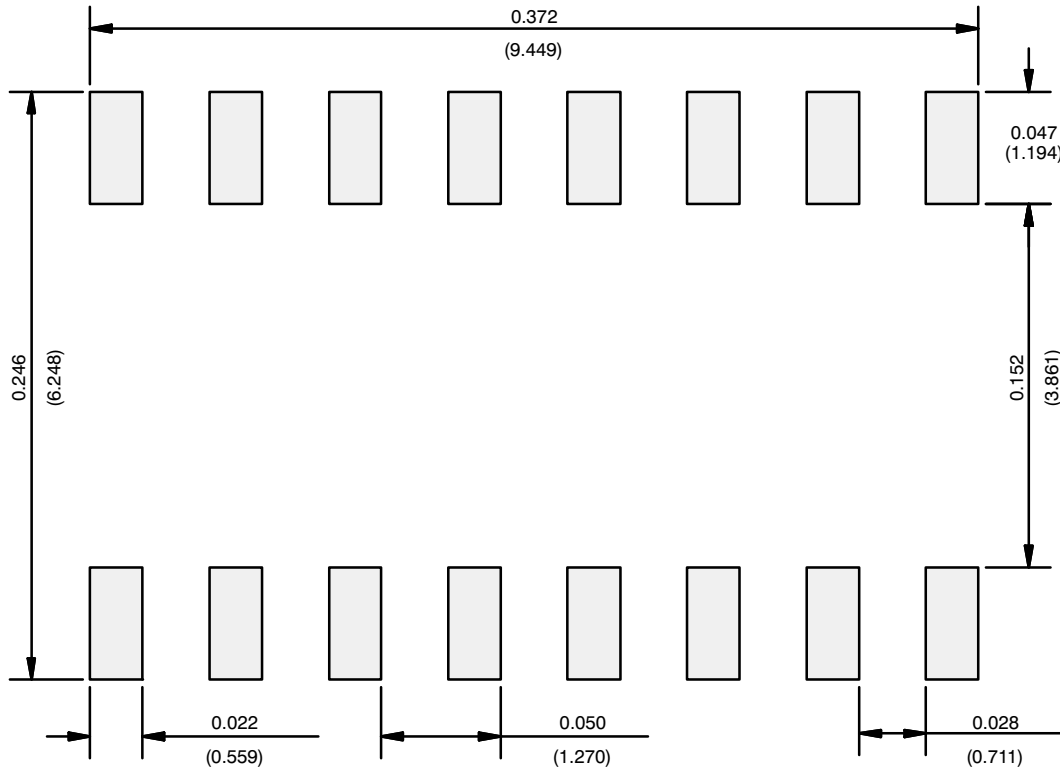
20-LEAD LCC



| Dim | MILLIMETERS | | INCHES | |
|----------------------|-------------|------|-----------|-------|
| | Min | Max | Min | Max |
| A | 1.37 | 2.24 | 0.054 | 0.088 |
| A₁ | 1.63 | 2.54 | 0.064 | 0.100 |
| B | 0.56 | 0.71 | 0.022 | 0.028 |
| D | 8.69 | 9.09 | 0.342 | 0.358 |
| E | 8.69 | 9.09 | 0.442 | 0.358 |
| e | 1.27 BSC | | 0.050 BSC | |
| L | 1.14 | 1.40 | 0.045 | 0.055 |
| L₁ | 1.96 | 2.36 | 0.077 | 0.093 |

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5321

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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