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100G Development Kit, Stratix V GX Edition

User Guide

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San Jose, CA 95134
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UG-01111-1.2

Contents

Appendix A. Programming the Flash Memory Device

Additional Information

1. About This Kit

The Altera® Stratix® V GX 100G Development Kit is a complete design environment that includes both the hardware and software you need to develop Stratix V GX FPGA designs.

Kit Features

This section briefly describes the Stratix V GX 100G Development Kit contents.

For a complete list of this kit's contents and capabilities, refer to the 100G Development Kit, Stratix V GX page.

Hardware

The Stratix V GX 100G Development Kit includes the following hardware:

- Stratix V GX 100G development board—A development platform that allows you to develop and prototype hardware designs running on the Stratix V GX FPGA.

  For detailed information about the board components and interfaces, refer to the *100G Development Kit, Stratix V GX Edition Reference Manual*.

- CFP loopback board
- SFP loopback module
- QSFP loopback module
- Heatsink and fan
- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - Ethernet and USB cables

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Software

Your kit includes a license for the Development Kit Edition (DKE) of the Quartus II software (Windows platform only). For one year, this license entitles you to most of the features of the Subscription Edition (excluding the IP Base Suite).

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web Edition or purchase a subscription to Quartus II software. For more information, refer to the Design Software page of the Altera website.

The Quartus II Development Kit Edition (DKE) software includes the following items:

- Quartus II Software—The Quartus II software, including the Qsys system integration tool, provides a comprehensive environment for network on a chip (NoC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system.
  - Verify functionality of your design, and quickly and easily evaluate its size and speed.
  - Generate time-limited device programming files for designs that include MegaCore functions.
  - Program a device and verify your design in hardware.

  The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

  For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.
- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allows you to develop embedded software for the Nios II processor, which you can include in your Altera FPGA designs.

Stratix V GX 100G Development Kit Installer

The license-free Stratix V GX 100G Development Kit installer includes all the documentation and design examples for the kit.

For information on installing the Development Kit Installer, refer to "Software Installation" on page 3–1.

2. Getting Started

The remaining chapters in this user guide lead you through the following Stratix V GX 100G development board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the 100G development board
- Configuring the Stratix V GX FPGA
- Running the Board Test System designs

For complete information about the 100G development board, refer to the *100G Development Kit, Stratix V GX Edition Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the boards to verify that you received all of the items listed in "Kit Features" on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Boards

To inspect each board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the 100G Development Kit, Stratix V GX page.
- For additional daughter cards available for purchase, refer to the Development Board Daughtercards page.
- For the Stratix V GX device documentation, refer to the Literature: Stratix V Devices page.
- To purchase devices from the eStore, refer to the Devices page.
- For Stratix V GX OrCAD symbols, refer to the Capture CIS Symbols page.

- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

This chapter explains how to install the following software:

- Quartus II Subscription Edition Software
- Stratix V GX 100G Development Kit
- USB-Blaster™ II driver

Installing the Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software provides the necessary tools for developing hardware and software for Altera devices. Included in the Quartus II Subscription Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. The Quartus II software (including Qsys) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this kit. To install the Altera development tools, perform the following steps:

1. Download the Quartus II Subscription Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.
2. Follow the on-screen instructions to complete the installation process.

If you have difficulty installing the Quartus II software, refer to *Altera Software Installation and Licensing Manual*.

Licensing Considerations

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus II software.

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web Edition or purchase a subscription to Quartus II software.

Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, you need to obtain and install a license file. To begin, go to the Self Service Licensing Center page of the Altera website, log into or create your myAltera account, and take the following actions:

1. On the Activate Products page, enter the serial number provided with your development kit in the **License Activation Code** box.

Your serial number is printed on the development kit box below the bottom bar code. The number is 10 or 11 alphanumeric characters and does not contain hyphens. Figure 3–1 shows *3S150SPXXXX* as an example serial number.

Figure 3–1. Locating Your Serial Number

2. Consult the Activate Products table, to determine how to proceed.
   a. If the administrator listed for your product is someone other than you, skip the remaining steps and contact your administrator to become a licensed user.
   b. If the administrator listed for your product is you, proceed to step 3.
   c. If the administrator listed for your product is *Stocking*, activate the product, making you the administrator, and proceed to step 3.
3. Use the Create New License page to license your product for a specific user (you) on specific computers. The Manage Computers and Manage Users pages allow you to add users and computers not already present in the licensing system.

   To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

4. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus_II software to enable the software.

For complete licensing details, refer to *Altera Software Installation and Licensing Manual*.

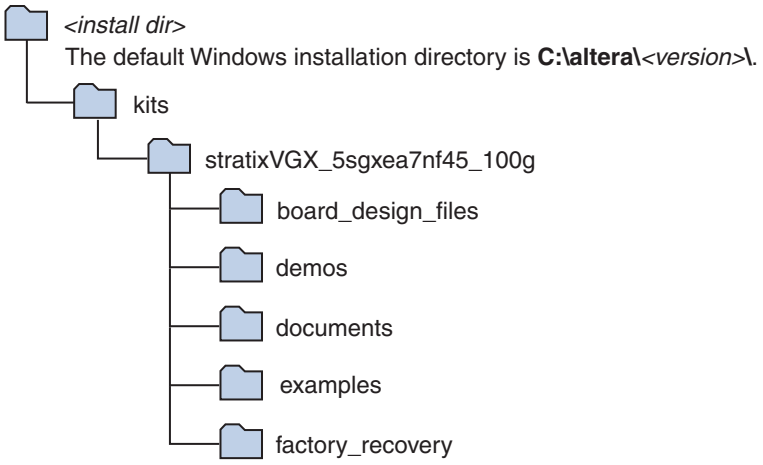
Installing the Development Kit

To install the Stratix V GX 100G Development Kit, perform the following steps:

1. Download the Stratix V GX 100G Development Kit installer from the 100G Development Kit, Stratix V GX page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.
2. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you choose is in the same relative location to the Quartus II software installation.

The installation program creates the Stratix V GX 100G Development Kit directory structure shown in Figure 3–2.

Figure 3–2. Stratix V GX 100G Development Kit Installed Directory Structure *(1)*



Note to Figure 3–2:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Stratix V GX 100G Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster II Driver

The Stratix V GX 100G development board includes integrated USB-Blaster II circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster driver II on the host computer.

Installation instructions for the USB-Blaster II driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

For USB-Blaster II configuration details, refer to the On-Board USB-Blaster II page.

4. Development Board Setup

This chapter explains how to set up the Stratix V GX 100G development board.

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Stratix V GX 100G development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch Settings" on page 4–2 to return the board to its factory settings before proceeding.
2. Connect the +19 V, 120 W to the DC Power Jack (J1) on the FPGA board and plug the cord into a power outlet.

   CAUTION: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

3. Set the POWER switch (SW1) to the on position. When power is supplied to the board, blue LED (D1) illuminates indicating that the board has power.

The MAX II device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. Pressing the PGM_SEL (S8) push-button loads the design into the FPGA from flash using the PFL in the MAX II device.

When configuration is complete, the MAX_CONF_DN LED (D25) illuminates, signaling that the Stratix V GX device configured successfully.

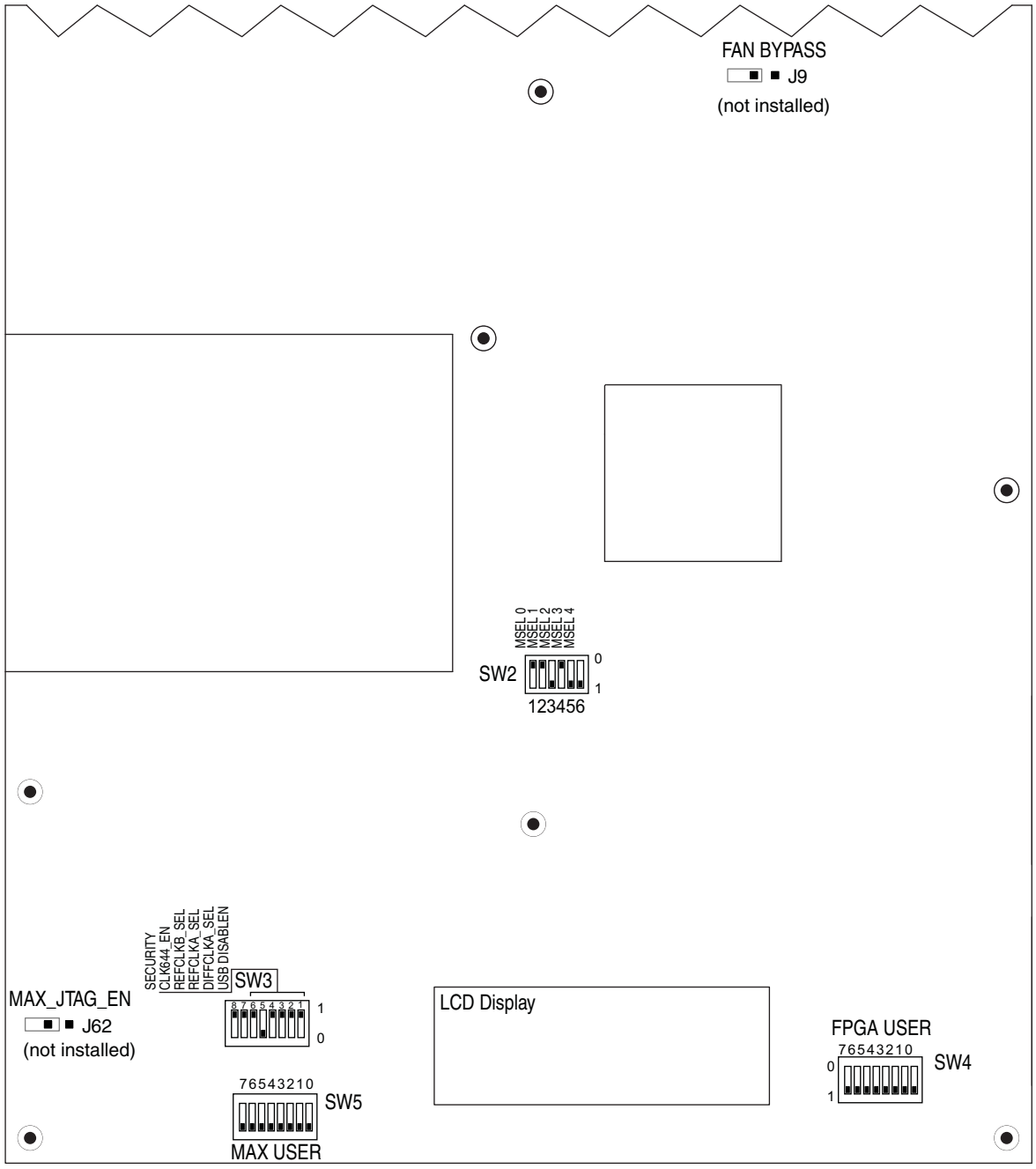
The kit includes a MAX II design which contains the MAX II PFL megafunction. The design resides in the *<install dir>***kits****stratixVGX_5sgxea7nf45_100g****examples****max2** directory.

For more information about the PFL megafunction, refer to *AN 386: Parallel Flash Loader Megafunction User Guide*.

Factory Default Switch Settings

This section shows the factory switch settings for the Stratix V GX 100G development board. Figure 4–1 shows the switch locations and the default position of each switch.

Figure 4–1. Switch Locations and Default Settings



To restore the switches to their factory default settings, perform the following steps:

1. Set DIP switch bank (SW2) to match Table 4–1 and Figure 4–1.

Table 4–1. SW2 Dip Switch Settings

Switch	Board Label	Function	Default Position
0	MSEL 0	Switch 0 has the following options: ■ Open = Logic 1 ■ Closed = Logic 0	Closed
1	MSEL 1	Switch 1 has the following options: ■ Open = Logic 1 ■ Closed = Logic 0	Closed
2	MSEL 2	Switch 2 has the following options: ■ Open = Logic 1 ■ Closed = Logic 0	Open
3	MSEL 3	Switch 4 has the following options: ■ Open = Logic 1 ■ Closed = Logic 0	Closed
4	MSEL 4	Switch 4 has the following options: ■ Open = Logic 1 ■ Closed = Logic 0	Open
5	—	Switch 4 has the following options: ■ Open = Logic 1 ■ Closed = Logic 0	Closed

2. Set DIP switch bank (SW3) to match Table 4–2 and Figure 4–1.

Table 4–2. SW3 DIP Switch Settings (Part 1 of 2)

Switch	Board Label	Function	Default Position
1	USB_DISABLEN	Switch 4 has the following options: ■ When off (1), USB is enabled. ■ When on (0), USB is disabled.	1
2	DIFFCLKA_SEL	Switch 4 has the following options: ■ When off (1), SMA is selected. ■ When on (0), PLL is selected.	1
3	REFCLKA_SEL	Switch 3 has the following options: ■ When off (1), SMA is selected. ■ When on (0), PLL is selected.	1
4	DIFFCLKB_SEL	Switch 4 has the following options: ■ When off (1), SMA is selected. ■ When on (0), PLL is selected.	1

Table 4–2. SW3 DIP Switch Settings (Part 2 of 2)

Switch	Board Label	Function	Default Position
5	REFCLKB_SEL	Switch 5 has the following options: ■ When on (1), the SMA is selected. ■ When off (0), the PLL is selected.	0
6	CLK_644_EN	Switch 6 has the following options: ■ When on (1), 644-MHz clock is enabled. ■ When off (10, 644-MHz clock is disabled.	1
7	SECURITY	Switch 7 has the following options: ■ When on (1), configuration security is enabled. ■ When off (0), configuration security is disabled. When enabled, the FPGA cannot be accessed via JTAG if the device has already been programmed by the PFL.	1
8	—	—	—

3. Set jumper blocks (J9, J62) to match Table 4–3 and Figure 4–1.

Table 4–3. Jumper Settings

Board Reference	Description	Shunt Position
J9	Fan Bypass — Shut installed forces the fan to ON and at full speed.	Not Installed
J62	MAX_JTAG_EN (logic 1) — Shunt installed removes MAX II from JTAG chain.	Not Installed

For more information about the FPGA board settings, refer to the *100G Development Kit, Stratix V GX Edition Reference Manual*.

5. Board Update Portal

The Stratix V GX 100G Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board, the FPGA configures with the with the Board Update Portal design example from flash memory. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware 1 portion of flash memory and provides kit-specific links and design resources.

The source code for the Board Update Portal design resides in the *<install dir>***kits****stratixVGX_5sgxea7nf45_100g****examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page A–4 to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.

Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. Attach the Ethernet cable from the board to your LAN.
2. Power up the board. The board connects to the LAN's gateway router, and then obtains an IP address. The LCD on the board displays the IP address.
3. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

   You can click *Stratix V GX 100G Development Kit* on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user hardware 1 portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Design files available from the 100G Development Kit, Stratix V GX page include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Preparing Design Files for Flash Programming" on page A–2 for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" to access the Board Update Portal web page.
2. In the **Hardware File Name** field specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field; otherwise, leave the **Software File Name** field blank.
3. Click **Upload**.
4. To configure the FPGA with the new user design after the flash memory upload process is complete, press PGM_SEL (S8) until POF 1 LED (D34) illuminates, and then press LOAD (S5) to configure the user hardware portion of flash memory.

As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user hardware 1 portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "Restoring the Flash Device to the Factory Settings" on page A–4.

6. Board Test System

The kit includes a design example and an application called the Board Test System to test the functionality of the Stratix V GX 100G development board. The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the application to test board components, modify functional parameters, observe performance, and measure power usage. (While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.) The application is also useful as a reference for designing systems. To install the application, follow the steps in "Installing the Development Kit" on page 3–3.

The Board Test System GUI communicates over the JTAG bus to a test design running in the Stratix V GX device.

Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

Preparing the Board

With the power to the board off, following these steps:

1. Connect the USB cable to the board.
2. Ensure that the development board switches and jumpers are set to the default positions as shown in the "Factory Default Switch Settings" section starting on page 4–2.

   For more information about the board's DIP switch and jumper settings, refer to the *100G Development Kit, Stratix V GX Edition Reference Manual*.

3. Turn on the power to the board. The board loads the design stored in the user hardware 1 portion of flash memory into the FPGA. If your board is still in the factory configuration, or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design loads the GPIO and flash memory tests.

   CAUTION: To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the <*install dir*>**\kits\stratixVGX_5sgxea7nf45_100g\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

On Windows, click **Start** > **All Programs** > **Altera** > **Stratix V GX 100G Development Kit** <*version*> > **Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA.

CAUTION

If using the optic modules (CFP, SFP, QSFP) you must set the user switch SW4.7 to enabled (1) to turn on the laser. When done using the optics, set SW4.7 to disabled (0).

Using the Board Test System

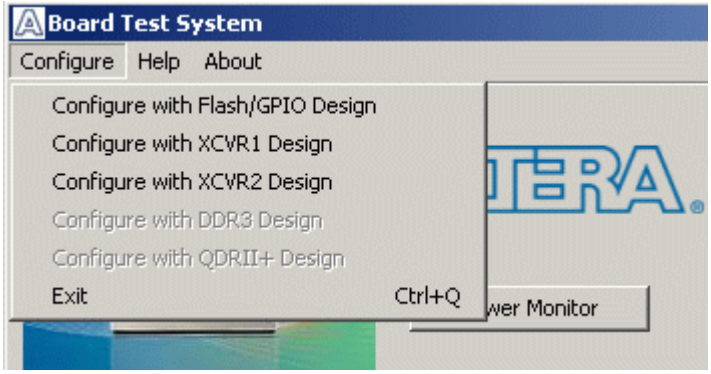
This section describes each control in the Board Test System application.

The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

The Configure Menu

Use the Configure menu (Figure 6–1) to select the design you want to use. Each design example tests different functions that corresponds to one or more application tabs.

Figure 6–1. The Configure Menu



To configure the FPGA with a test system design, perform the following steps:

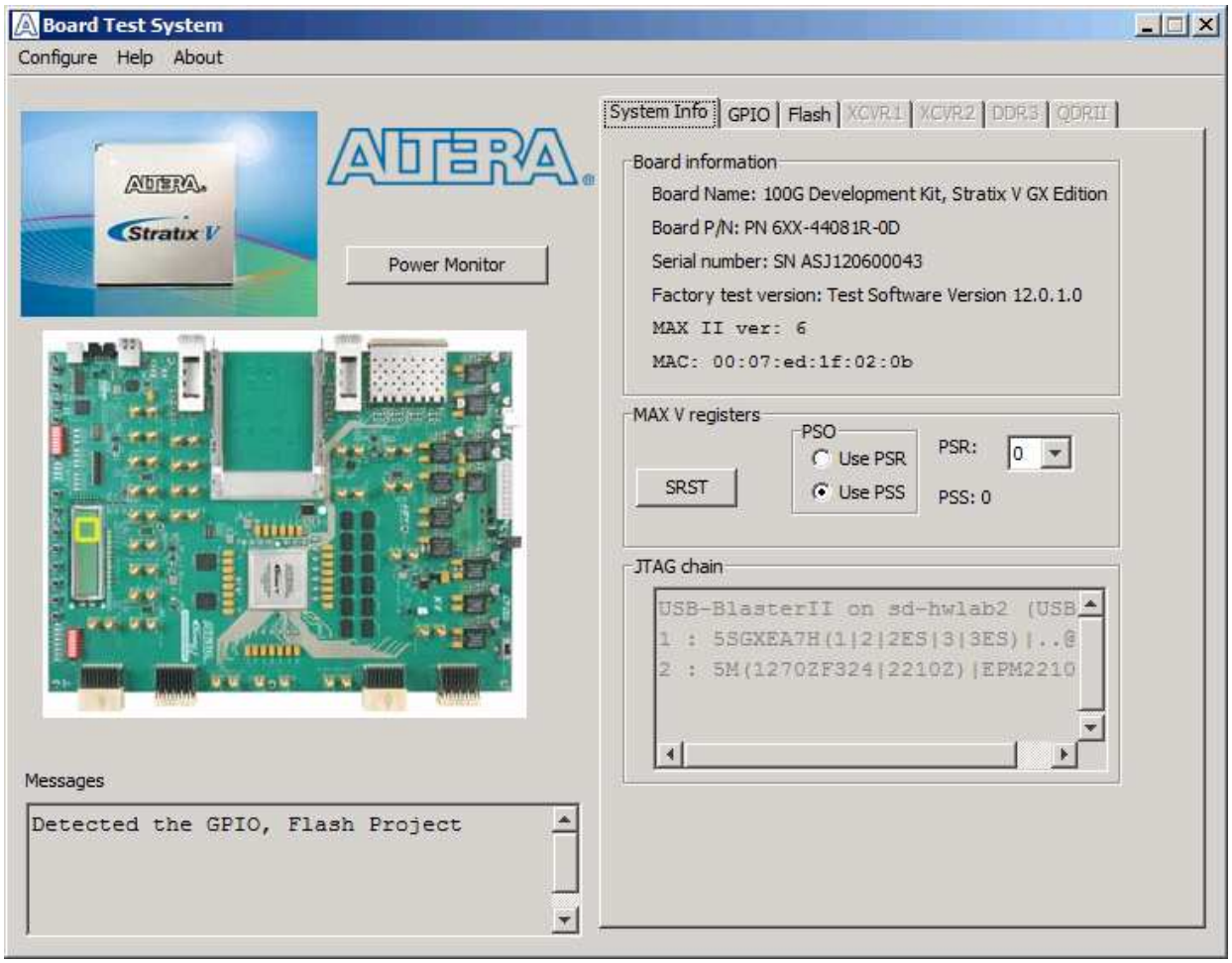
1. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click **Configure** or **Download Start** to download the corresponding design's Raw-Binary Format (**.rbf**) configuration file to the FPGA. The download process usually takes about a minute.
3. When configuration finishes, close the Quartus II Programmer if open. The design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled.

The System Info Tab

The **System Info** tab shows board's current configuration. This tab displays the contents of the MAX II registers, the JTAG chain, the board's MAC address, the flash memory map, and other details stored on the board.

Figure 6–2 shows the initial GUI for a board that is in the factory configuration.

Figure 6–2. Board Test System Graphical User Interface



The following sections describe the controls on the **System Info** tab.

Power Monitor

This button starts the Power Monitor application that measures and reports current power and temperature information for the board. Because the application communicates over the JTAG bus to the MAX II device, you can measure the power of any design in the FPGA, including your own designs. For details, refer to "The Power Monitor" on page 6–13.

Board Information

The **Board information** controls display static information about your board.

- **Name**—Indicates the official name of the board, given by the Board Test System.
- **Part number**—Indicates the part number of the board.
- **Serial number**—Indicates the serial number of the board.
- **Factory test version**—Indicates the version of the Board Test System currently running on the board.
- **Factory test date**—Indicates the release date of the Board Test System currently running on the board.
- **MAX II ver**—Indicates the version of MAX II code currently running on the board, which resides in the *<install dir>***kits\stratixVGX_5sgxea7nf45_100g\examples** directory. Newer revisions of this code might be available on the 100G Development Kit, Stratix V GX page of the Altera website.
- **MAC address**—Indicates the MAC address of the board.

MAX II Registers

The **MAX II registers** control allow you to view and change the current MAX II register values as described in Table 6–1. Changes to the register values with the GUI take effect immediately. For example, writing a 0 to SRST resets the board.

Table 6–1. MAX II Registers

Register Name	Read/Write Capability	Description
System Reset (SRST)	Write only	Set to 0 to initiate an FPGA reconfiguration.
Page Select Register (PSR)	Read / Write	Determines which of the flash memory to use for FPGA reconfiguration. The flash memory ships with pages 0 and 1 preconfigured.
Page Select Override (PSO)	Read / Write	When set to 0, the value in PSR determines the page of flash memory to use for FPGA reconfiguration. When set to 1, the value in PSS determines the page of flash memory to use for FPGA reconfiguration.
Page Select Switch (PSS)	Read only	Holds the current value of the illuminated USER_POF LEDs (D32, D33, D34). ■ 0 = USER_POF1 LED (D34) ■ 1 = USER_POF2 LED (D33) ■ 2 = USER_POF3 LED (D32) CAUTION This state selects a page not supported by the default memory map. Use of this extra page may require the flash to be re-imaged if you want to return to the factory state.

- **SRST**—Resets the system and reloads the FPGA with a design from flash memory based on the other MAX II register values.

- **PSO**—Sets the MAX II PSO register. The following options are available:
  - **Use PSR**—Allows the PSR to determine the page of flash memory to use for FPGA reconfiguration.
  - **Use PSS**—Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.
- **PSS**—Displays the MAX II PSS register value.
- **PSR**—Sets the MAX II PSR register. The numerical values in the list corresponds to the page of flash memory to load during FPGA reconfiguration. Refer to Table 6–1 for more information.

Because the **System Info** tab requires that a specific design is running in the FPGA at a specific clock speed, writing a 0 to SRST; or changing the PSO value can cause the Board Test System to stop running.

JTAG Chain

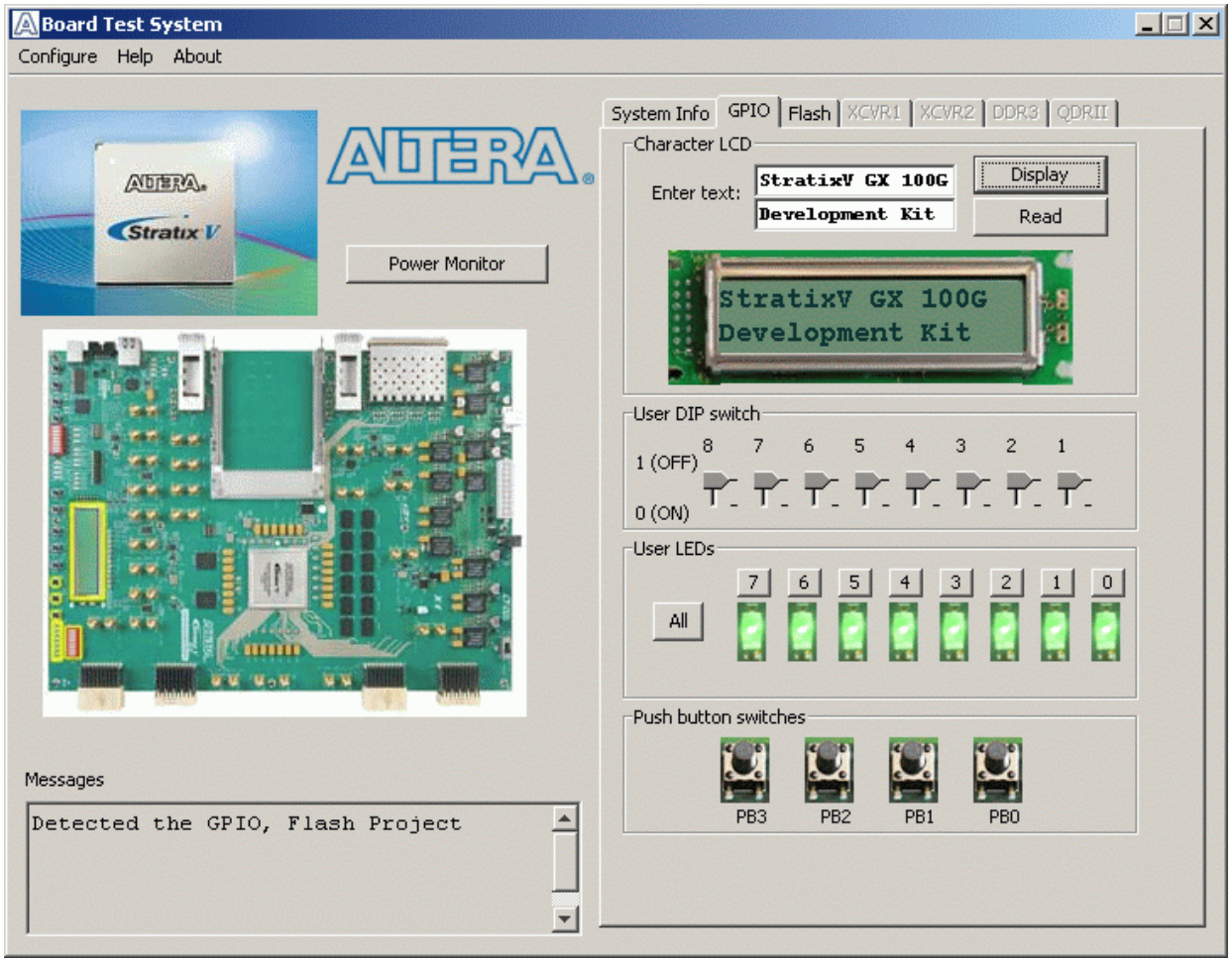
The **JTAG chain** control shows all the devices currently in the JTAG chain. The Stratix V GX device is always the first device in the chain.

MAX_JTAG_EN (J62) includes the MAX II device in the JTAG chain when a jumper is not installed. To remove the MAX II device from the chain, install a jumper to J62.

The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. Figure 6–3 shows the **GPIO** tab.

Figure 6–3. The GPIO Tab



The following sections describe the controls on the **GPIO** tab.

Character LCD

This controls allows you to display text strings on the character LCD on your board. Type text in the text boxes and then click **Display**.

If you exceed the 16 character display limit on either line, a warning message appears.

User DIP Switch

The read-only User DIP switch control displays the current positions of the switches in the user DIP switch bank (SW4). Change the switches on the board to see the graphical display change accordingly.

User LEDs

This control displays the current state of the user LEDs.

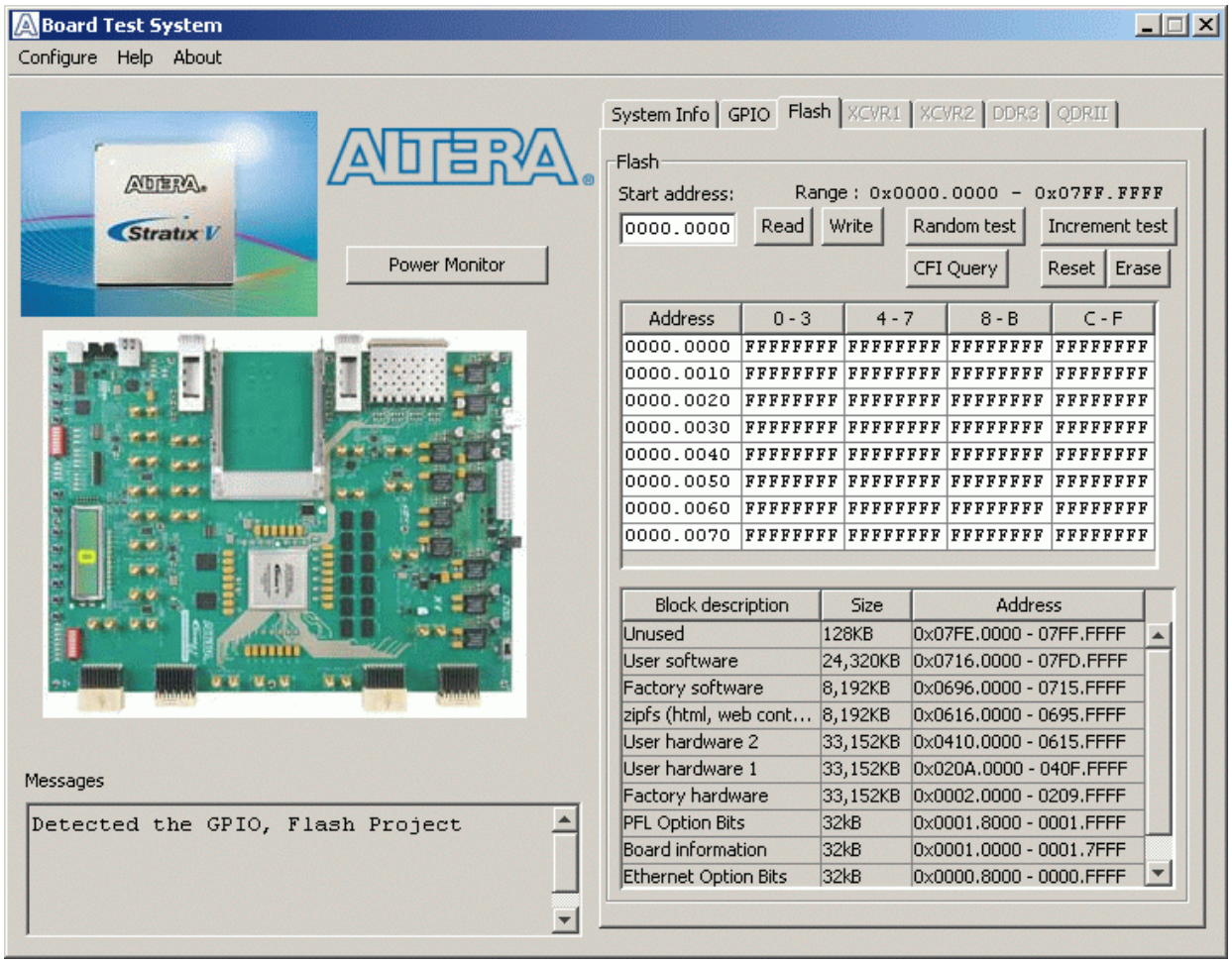
Push Button Switches

This read-only control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

The Flash Tab

The **Flash** tab allows you to read and write flash memory on your board. Figure 6–4 shows the **Flash** tab.

Figure 6–4. The Flash Tab



The following sections describe the controls on the **Flash** tab.

Start address

This control allows you to enter an 8-hex digit (preceding with the 0x hex identifier).