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Stratix IV Device Handbook

Volume 1

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Additional Information

Chapter Revision Dates

The chapters in this document, Stratix IV Device Handbook, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Overview for the Stratix IV Device Family
Revised: *January 2016*
Part Number: *SIV51001-3.5*

Chapter 2. Logic Array Blocks and Adaptive Logic Modules in Stratix IV Devices
Revised: *February 2011*
Part Number: *SIV51002-3.1*

Chapter 3. TriMatrix Embedded Memory Blocks in Stratix IV Devices
Revised: *December 2011*
Part Number: *SIV51003-3.3*

Chapter 4. DSP Blocks in Stratix IV Devices
Revised: *February 2011*
Part Number: *SIV51004-3.1*

Chapter 5. Clock Networks and PLLs in Stratix IV Devices
Revised: *September 2012*
Part Number: *SIV51005-3.4*

Chapter 6. I/O Features in Stratix IV Devices
Revised: *September 2012*
Part Number: *SIV51006-3.4*

Chapter 7. External Memory Interfaces in Stratix IV Devices
Revised: *February 2011*
Part Number: *SIV51007-3.2*

Chapter 8. High-Speed Differential I/O Interfaces and DPA in Stratix IV Devices
Revised: *September 2012*
Part Number: *SIV51008-3.4*

Chapter 9. Hot Socketing and Power-On Reset in Stratix IV Devices
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Part Number: *SIV51009-3.2*

Chapter 10. Configuration, Design Security, and Remote System Upgrades in Stratix IV Devices
Revised: *September 2012*
Part Number: *SIV51010-3.5*

Chapter 11. SEU Mitigation in Stratix IV Devices
Revised: *February 2011*
Part Number: *SIV51011-3.2*

Chapter 12. JTAG Boundary-Scan Testing in Stratix IV Devices

Revised: *February 2011*
Part Number: *SIV51012-3.2*

Chapter 13. Power Management in Stratix IV Devices
Revised: *February 2011*
Part Number: *SIV51013-3.2*

Section I. Device Core

This section provides a complete overview of all features relating to the Stratix® IV device family, which is the most architecturally advanced, high-performance, low-power FPGA in the market place. This section includes the following chapters:

- Chapter 1, Overview for the Stratix IV Device Family
- Chapter 2, Logic Array Blocks and Adaptive Logic Modules in Stratix IV Devices
- Chapter 3, TriMatrix Embedded Memory Blocks in Stratix IV Devices
- Chapter 4, DSP Blocks in Stratix IV Devices
- Chapter 5, Clock Networks and PLLs in Stratix IV Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

1. Overview for the Stratix IV Device Family

SIV51001-3.5

Altera® Stratix® IV FPGAs deliver a breakthrough level of system bandwidth and power efficiency for high-end applications, allowing you to innovate without compromise. Stratix IV FPGAs are based on the Taiwan Semiconductor Manufacturing Company (TSMC) 40-nm process technology and surpass all other high-end FPGAs, with the highest logic density, most transceivers, and lowest power requirements.

The Stratix IV device family contains three optimized variants to meet different application requirements:

- Stratix IV E (Enhanced) FPGAs—up to 813,050 logic elements (LEs), 33,294 kilobits (Kb) RAM, and 1,288 18 x 18 bit multipliers
- Stratix IV GX transceiver FPGAs—up to 531,200 LEs, 27,376 Kb RAM, 1,288 18 x 18-bit multipliers, and 48 full-duplex clock data recovery (CDR)-based transceivers at up to 8.5 Gbps
- Stratix IV GT—up to 531,200 LEs, 27,376 Kb RAM, 1,288 18 x 18-bit multipliers, and 48 full-duplex CDR-based transceivers at up to 11.3 Gbps

The complete Altera high-end solution includes the lowest risk, lowest total cost path to volume using HardCopy® IV ASICs for all the family variants, a comprehensive portfolio of application solutions customized for end-markets, and the industry leading Quartus® II software to increase productivity and performance.

For information about upcoming Stratix IV device features, refer to the *Upcoming Stratix IV Device Features* document.

For information about changes to the currently published *Stratix IV Device Handbook*, refer to the *Addendum to the Stratix IV Device Handbook* chapter.

This chapter contains the following sections:

Feature Summary

The following list summarizes the Stratix IV device family features:

- Up to 48 full-duplex CDR-based transceivers in Stratix IV GX and GT devices supporting data rates up to 8.5 Gbps and 11.3 Gbps, respectively
- Dedicated circuitry to support physical layer functionality for popular serial protocols, such as PCI Express (PCIe) (PIPE) Gen1 and Gen2, Gbps Ethernet (GbE), Serial RapidIO, SONET/SDH, XAUI/HiGig, (OIF) CEI-6G, SD/HD/3G-SDI, Fibre Channel, SFI-5, and Interlaken
- Complete PCIe protocol solution with embedded PCIe hard IP blocks that implement PHY-MAC layer, Data Link layer, and Transaction layer functionality

  For more information, refer to the *IP Compiler for PCI Express User Guide*.
- Programmable transmitter pre-emphasis and receiver equalization circuitry to compensate for frequency-dependent losses in the physical medium
- Typical physical medium attachment (PMA) power consumption of 100 mW at 3.125 Gbps and 135 mW at 6.375 Gbps per channel
- 72,600 to 813,050 equivalent LEs per device
- 7,370 to 33,294 Kb of enhanced TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and FIFO buffers
- High-speed digital signal processing (DSP) blocks configurable as 9 x 9-bit, 12 x 12-bit, 18 x 18-bit, and 36 x 36-bit full-precision multipliers at up to 600 MHz
- Up to 16 global clocks (GCLK), 88 regional clocks (RCLK), and 132 periphery clocks (PCLK) per device
- Programmable power technology that minimizes power while maximizing device performance
- Up to 1,120 user I/O pins arranged in 24 modular I/O banks that support a wide range of single-ended and differential I/O standards
- Support for high-speed external memory interfaces including DDR, DDR2, DDR3 SDRAM, RLDRAM II, QDR II, and QDR II+ SRAM on up to 24 modular I/O banks
- High-speed LVDS I/O support with serializer/deserializer (SERDES), dynamic phase alignment (DPA), and soft-CDR circuitry at data rates up to 1.6 Gbps
- Support for source-synchronous bus standards, including SGMII, GbE, SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
- Pinouts for Stratix IV E devices designed to allow migration of designs from Stratix III to Stratix IV E with minimal PCB impact

Stratix IV GX Devices

Stratix IV GX devices provide up to 48 full-duplex CDR-based transceiver channels per device:

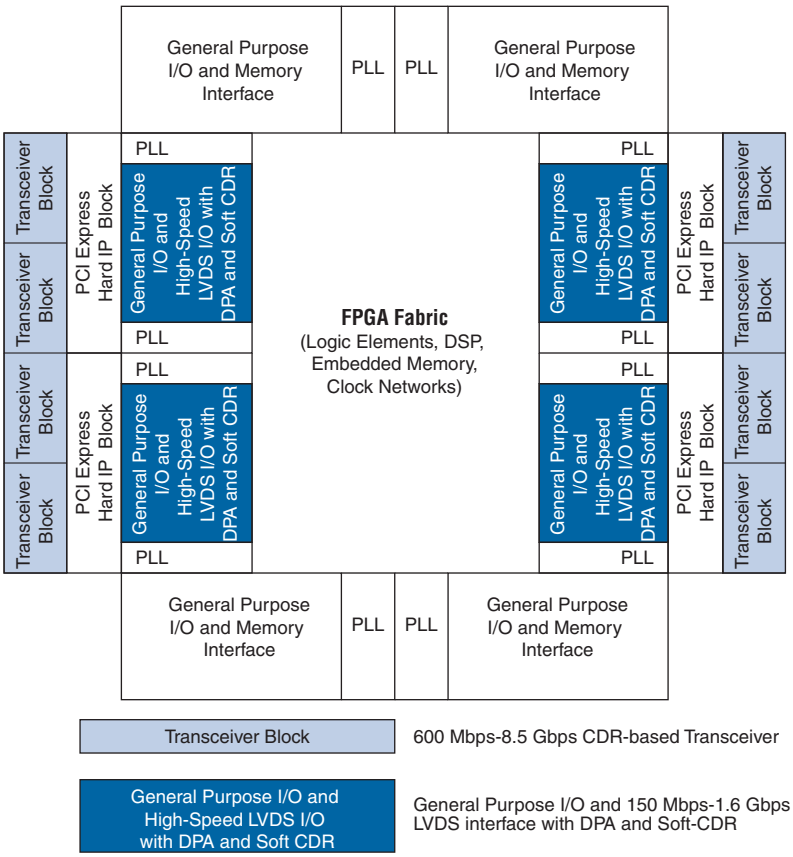
- Thirty-two out of the 48 transceiver channels have dedicated physical coding sublayer (PCS) and physical medium attachment (PMA) circuitry and support data rates between 600 Mbps and 8.5 Gbps
- The remaining 16 transceiver channels have dedicated PMA-only circuitry and support data rates between 600 Mbps and 6.5 Gbps

The actual number of transceiver channels per device varies with device selection. For more information about the exact transceiver count in each device, refer to Table 1–1 on page 1–11.

For more information about transceiver architecture, refer to the *Transceiver Architecture in Stratix IV Devices* chapter.

Figure 1–1 shows a high-level Stratix IV GX chip view.

Figure 1–1. Stratix IV GX Chip View (1)



Note to Figure 1–1:

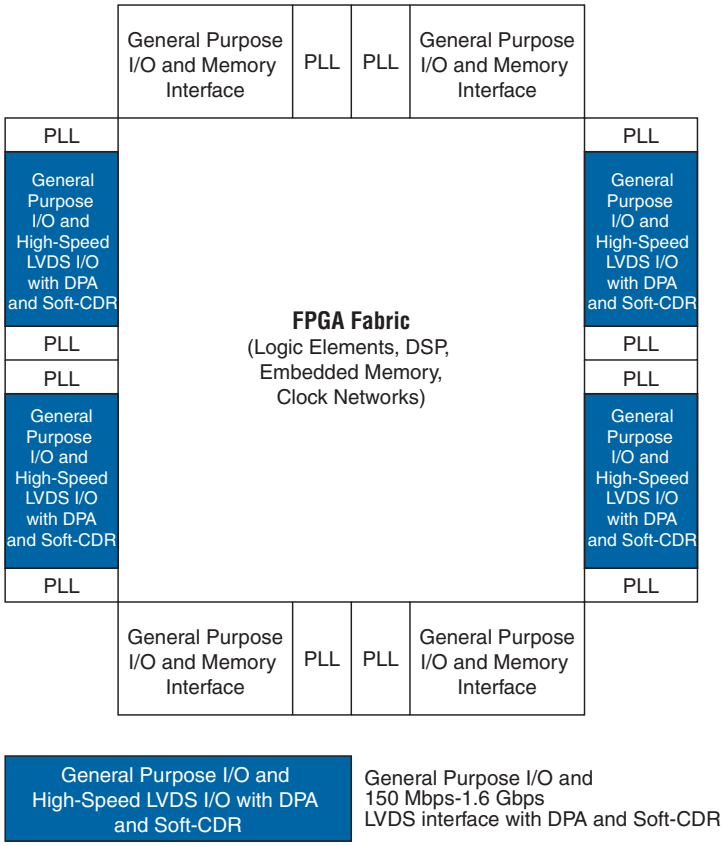
(1) Resource counts vary with device selection, package selection, or both.

Stratix IV E Device

Stratix IV E devices provide an excellent solution for applications that do not require high-speed CDR-based transceivers, but are logic, user I/O, or memory intensive.

Figure 1–2 shows a high-level Stratix IV E chip view.

Figure 1–2. Stratix IV E Chip View (1)



Note to Figure 1–2:

(1) Resource counts vary with device selection, package selection, or both.

Stratix IV GT Devices

Stratix IV GT devices provide up to 48 CDR-based transceiver channels per device:

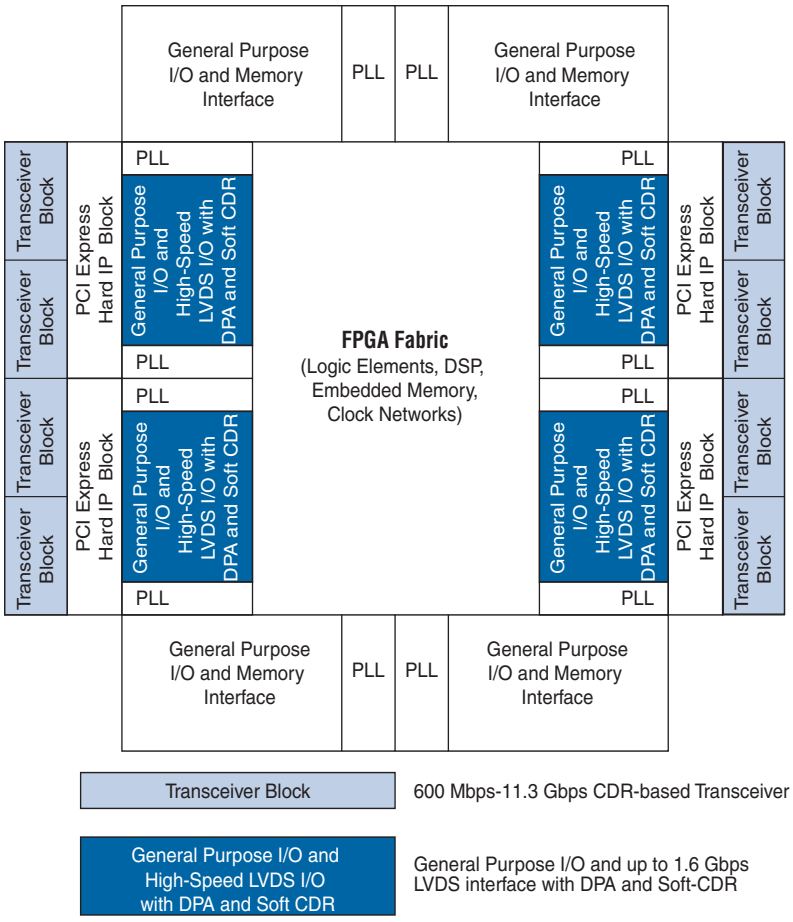
- Thirty-two out of the 48 transceiver channels have dedicated PCS and PMA circuitry and support data rates between 600 Mbps and 11.3 Gbps
- The remaining 16 transceiver channels have dedicated PMA-only circuitry and support data rates between 600 Mbps and 6.5 Gbps

The actual number of transceiver channels per device varies with device selection. For more information about the exact transceiver count in each device, refer to Table 1–7 on page 1–16.

For more information about Stratix IV GT devices and transceiver architecture, refer to the *Transceiver Architecture in Stratix IV Devices* chapter.

Figure 1–3 shows a high-level Stratix IV GT chip view.

Figure 1–3. Stratix IV GT Chip View (1)



Note to Figure 1–3:

(1) Resource counts vary with device selection, package selection, or both.

Architecture Features

The Stratix IV device family features are divided into high-speed transceiver features and FPGA fabric and I/O features.

The high-speed transceiver features apply only to Stratix IV GX and Stratix IV GT devices.

High-Speed Transceiver Features

The following sections describe high-speed transceiver features for Stratix IV GX and GT devices.

Highest Aggregate Data Bandwidth

Up to 48 full-duplex transceiver channels supporting data rates up to 8.5 Gbps in Stratix IV GX devices and up to 11.3 Gbps in Stratix IV GT devices.

Wide Range of Protocol Support

Physical layer support for the following serial protocols:

- Stratix IV GX—PCIe Gen1 and Gen2, GbE, Serial RapidIO, SONET/SDH, XAUI/HiGig, (OIF) CEI-6G, SD/HD/3G-SDI, Fibre Channel, SFI-5, GPON, SAS/SATA, HyperTransport 1.0 and 3.0, and Interlaken
- Stratix IV GT—40G/100G Ethernet, SFI-S, Interlaken, SFI-5.1, Serial RapidIO, SONET/SDH, XAUI/HiGig, (OIF) CEI-6G, 3G-SDI, and Fibre Channel
- Extremely flexible and easy-to-configure transceiver data path to implement proprietary protocols
- PCIe Support
  - Complete PCIe Gen1 and Gen2 protocol stack solution compliant to PCI Express base specification 2.0 that includes PHY-MAC, Data Link, and transaction layer circuitry embedded in PCI Express hard IP blocks

    For more information, refer to the *PCI Express Compiler User Guide*.

  - Root complex and end-point applications
  - x1, x4, and x8 lane configurations
  - PIPE 2.0-compliant interface
  - Embedded circuitry to switch between Gen1 and Gen2 data rates
  - Built-in circuitry for electrical idle generation and detection, receiver detect, power state transitions, lane reversal, and polarity inversion
  - 8B/10B encoder and decoder, receiver synchronization state machine, and ± 300 parts per million (ppm) clock compensation circuitry
  - Transaction layer support for up to two virtual channels (VCs)

- XAUI/HiGig Support
  - Compliant to IEEE802.3ae specification
  - Embedded state machine circuitry to convert XGMII idle code groups (||I||) to and from idle ordered sets (||A||, ||K||, ||R||) at the transmitter and receiver, respectively
  - 8B/10B encoder and decoder, receiver synchronization state machine, lane deskew, and ± 100 ppm clock compensation circuitry
- GbE Support
  - Compliant to IEEE802.3-2005 specification
  - Automatic idle ordered set (/I1/, /I2/) generation at the transmitter, depending on the current running disparity
  - 8B/10B encoder and decoder, receiver synchronization state machine, and ± 100 ppm clock compensation circuitry
- Support for other protocol features such as MSB-to-LSB transmission in SONET/SDH configuration and spread-spectrum clocking in PCIe configurations

Diagnostic Features

- Serial loopback from the transmitter serializer to the receiver CDR for transceiver PCS and PMA diagnostics
- Reverse serial loopback pre- and post-CDR to transmitter buffer for physical link diagnostics
- Loopback master and slave capability in PCI Express hard IP blocks

For more information, refer to the *PCI Express Compiler User Guide*.

Signal Integrity

Stratix IV devices simplify the challenge of signal integrity through a number of chip, package, and board-level enhancements to enable efficient high-speed data transfer into and out of the device. These enhancements include:

- Programmable 3-tap transmitter pre-emphasis with up to 8,192 pre-emphasis levels to compensate for pre-cursor and post-cursor inter-symbol interference (ISI)
- Up to 900% boost capability on the first pre-emphasis post-tap
- User-controlled and adaptive 4-stage receiver equalization with up to 16 dB of high-frequency gain
- On-die power supply regulators for transmitter and receiver phase-locked loop (PLL) charge pump and voltage controlled oscillator (VCO) for superior noise immunity
- On-package and on-chip power supply decoupling to satisfy transient current requirements at higher frequencies, thereby reducing the need for on-board decoupling capacitors
- Calibration circuitry for transmitter and receiver on-chip termination (OCT) resistors

FPGA Fabric and I/O Features

The following sections describe the Stratix IV FPGA fabric and I/O features.

Device Core Features

- Up to 531,200 LEs in Stratix IV GX and GT devices and up to 813,050 LEs in Stratix IV E devices, efficiently packed in unique and innovative adaptive logic modules (ALMs)
- Ten ALMs per logic array block (LAB) deliver faster performance, improved logic utilization, and optimized routing
- Programmable power technology, including a variety of process, circuit, and architecture optimizations and innovations
- Programmable power technology available to select power-driven compilation options for reduced static power consumption

Embedded Memory

- TriMatrix embedded memory architecture provides three different memory block sizes to efficiently address the needs of diversified FPGA designs:
  - 640-bit MLAB
  - 9-Kb M9K
  - 144-Kb M144K
- Up to 33,294 Kb of embedded memory operating at up to 600 MHz
- Each memory block is independently configurable to be a single- or dual-port RAM, FIFO, ROM, or shift register

Digital Signal Processing (DSP) Blocks

- Flexible DSP blocks configurable as 9 x 9-bit, 12 x 12-bit, 18 x 18-bit, and 36 x 36-bit full-precision multipliers at up to 600 MHz with rounding and saturation capabilities
- Faster operation due to fully pipelined architecture and built-in addition, subtraction, and accumulation units to combine multiplication results
- Optimally designed to support advanced features such as adaptive filtering, barrel shifters, and finite and infinite impulse response (FIR and IIR) filters

Clock Networks

- Up to 16 global clocks and 88 regional clocks optimally routed to meet the maximum performance of 800 MHz
- Up to 112 and 132 periphery clocks in Stratix IV GX and Stratix IV E devices, respectively
- Up to 66 (16 GCLK + 22 RCLK + 28 PCLK) clock networks per device quadrant in Stratix IV GX and Stratix IV GT devices
- Up to 71 (16 GCLK + 22 RCLK + 33 PCLK) clock networks per device quadrant in Stratix IV E devices

PLLs

- Three to 12 PLLs per device supporting spread-spectrum input tracking, programmable bandwidth, clock switchover, dynamic reconfiguration, and delay compensation
- On-chip PLL power supply regulators to minimize noise coupling

I/O Features

- Sixteen to 24 modular I/O banks per device with 24 to 48 I/Os per bank designed and packaged for optimal simultaneous switching noise (SSN) performance and migration capability
- Support for a wide range of industry I/O standards, including single-ended (LVTTL/CMOS/PCI/PCIX), differential (LVDS/mini-LVDS/RSDS), voltage-referenced single-ended and differential (SSTL/HSTL Class I/II) I/O standards
- On-chip series (R_S) and on-chip parallel (R_T) termination with auto-calibration for single-ended I/Os and on-chip differential (R_D) termination for differential I/Os
- Programmable output drive strength, slew rate control, bus hold, and weak pull-up capability for single-ended I/Os
- User I/O:GND:V_{CC} ratio of 8:1:1 to reduce loop inductance in the package—PCB interface
- Programmable transmitter differential output voltage (V_{OD}) and pre-emphasis for high-speed LVDS I/O

High-Speed Differential I/O with DPA and Soft-CDR

- Dedicated circuitry on the left and right sides of the device to support differential links at data rates from 150 Mbps to 1.6 Gbps
- Up to 98 differential SERDES in Stratix IV GX devices, up to 132 differential SERDES in Stratix IV E devices, and up to 47 differential SERDES in Stratix IV GT devices
- DPA circuitry at the receiver automatically compensates for channel-to-channel and channel-to-clock skew in source synchronous interfaces
- Soft-CDR circuitry at the receiver allows implementation of asynchronous serial interfaces with embedded clocks at up to 1.6 Gbps data rate (SGMII and GbE)

External Memory Interfaces

- Support for existing and emerging memory interface standards such as DDR SDRAM, DDR2 SDRAM, DDR3 SDRAM, QDRII SRAM, QDRII+ SRAM, and RLDRAM II
- DDR3 up to 1,067 Mbps/533 MHz
- Programmable DQ group widths of 4 to 36 bits (includes parity bits)
- Dynamic OCT, trace mismatch compensation, read-write leveling, and half-rate register capabilities provide a robust external memory interface solution

System Integration

- All Stratix IV devices support hot socketing
- Four configuration modes:
  - Passive Serial (PS)
  - Fast Passive Parallel (FPP)
  - Fast Active Serial (FAS)
  - JTAG configuration
- Ability to perform remote system upgrades
- 256-bit advanced encryption standard (AES) encryption of configuration bits protects your design against copying, reverse engineering, and tampering
- Built-in soft error detection for configuration RAM cells

For more information about how to connect the PLL, external memory interfaces, I/O, high-speed differential I/O, power, and the JTAG pins to PCB, refer to the *Stratix IV GX and Stratix IV E Device Family Pin Connection Guidelines* and the *Stratix IV GT Device Family Pin Connection Guidelines*.

Table 1–1 lists the Stratix IV GX device features.

Table 1–1. Stratix IV GX Device Features (Part 1 of 2)

Feature	EP4SGX70		EP4SGX110			EP4SGX180				EP4SGX230				EP4SGX290						EP4SGX360						EP4SGX530	
Package Option	F780	F1152	F780	F1152		F780	F1152		F1517	F780	F1152		F1517	F780	F1152		F1517	F1760	F1932	F780	F1152		F1517	F1760	F1932	F1760	F1932
ALMs	29,040		42,240			70,300				91,200				116,480						141,440						212,480	
LEs	72,600		105,600			175,750				228,000				291,200						353,600						531,200	
0.6 Gbps-8.5 Gbps Transceivers (PMA + PCS) (1)	—	16	—	—	16	—	—	16	24	—	—	16	24	—	—	16	24	24	32	—	—	16	24	24	32	24	32
0.6 Gbps-6.5 Gbps Transceivers (PMA + PCS) (1)	8	—	8	16	—	8	16	—	—	8	16	—	—	16	16	—	—	—	—	16	16	—	—	—	—	—	—
PMA-only CMU Channels (0.6 Gbps-6.5 Gbps)	—	8	—	—	8	—	—	8	12	—	—	8	12	—	—	8	12	12	16	—	—	8	12	12	16	12	16
PCI Express hard IP Blocks	1	2	1	2		1	2			1	2			2					4	2					4	4	
High-Speed LVDS SERDES (up to 1.6 Gbps) (4)	28	56	28	28	56	28	44		88	28	44		88	—	44		88	88	98	—	44		88	88	98	88	98
SPI-4.2 Links	1		1			1	2		4	1	2		4	—	2		4			—	2		4			4	