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Stratix V Advanced Systems Development Kit

User Guide

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UG-01132-1.0

Contents

1. About This Kit

The Altera® Stratix® V Advanced Systems Development Kit is a complete design environment that includes both the hardware and software you need to develop Stratix V GX FPGA designs.

Kit Features

This section briefly describes the development kit contents.

For a complete list of this kit's contents and capabilities, refer to the Stratix V Advanced Systems Development Kit.

Hardware

The Stratix V Advanced Systems Development Kit includes the following hardware:

- Stratix V GX advanced systems board—A development platform that allows you to develop and prototype hardware designs running on the Stratix V GX FPGA.

  For detailed information about the board components and interfaces, refer to the *Stratix V Advanced Systems Development Board Reference Manual*.

- HSMC loopback board—A daughtercard that allows for loopback testing all signals on the HSMC interface using the Board Test System.
- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - Standard USB A to mini-USB cable

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Software

Your kit includes a license for the Development Kit Edition (DKE) of the Quartus II software (Windows platform only). For one year, this license entitles you to most of the features of the Subscription Edition (excluding the IP Base Suite).

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software. For more information, refer to the Design Software page of the Altera website.

The Quartus II Development Kit Edition (DKE) software includes the following items:

- Quartus II Software—The Quartus II software, including the Qsys system integration tool, provides a comprehensive environment for network on a chip (NoC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system.
  - Verify functionality of your design, and quickly and easily evaluate its size and speed.
  - Generate time-limited device programming files for designs that include MegaCore functions.
  - Program a device and verify your design in hardware.

  The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

  For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.
- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allows you to develop embedded software for the Nios II processor, which you can include in your Altera FPGA designs.

The Kit Installer

The license-free Stratix V Advanced Systems Development Kit installer includes all the documentation and design examples for the kit.

For information on installing the Development Kit Installer, refer to "Software Installation" on page 3–1.

2. Getting Started

The remaining chapters in this user guide lead you through the following Stratix V GX advanced systems board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the advanced systems board
- Configuring the Stratix V GX FPGA
- Running the Board Test System designs

For complete information about the advanced systems board, refer to the *Stratix V Advanced Systems Development Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in "Kit Features" on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Board

To inspect the board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.

For information about measuring board and FPGA temperature in real time, refer to "The Power Monitor" on page 5–13.

For information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the Stratix V Advanced Systems Development Kit page.
- For additional daughter cards available for purchase, refer to the Development Board Daughtercards page.

- For the Stratix V GX device documentation, refer to the Literature: Stratix V Devices page.
- To purchase devices from the eStore, refer to the Devices page.
- For Stratix V GX OrCAD symbols, refer to the Capture CIS Symbols page.
- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

This chapter explains how to install the following software:

- Quartus II Subscription Edition Software
- Stratix V Advanced Systems Development Kit
- USB-Blaster™ II driver

Installing the Quartus II Subscription Edition Software

Included in the Quartus II Subscription Edition Software are the Quartus II software (including Qsys), the Nios II EDS, and the MegaCore IP Library. To install the Altera development tools, perform the following steps:

1. Download the Quartus II Subscription Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.
2. Follow the on-screen instructions to complete the installation process. Choose an installation directory that is relative to the Quartus II software installation directory.

If you have difficulty installing the Quartus II software, refer to the *Altera Software Installation and Licensing Manual*.

Licensing Considerations

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus II software.

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software.

Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, you need to obtain and install a license file. To begin, go to the Self Service Licensing Center page of the Altera website, log into or create your myAltera account, and take the following actions:

1. On the Activate Products page, enter the serial number provided with your development kit in the **License Activation Code** box.

   Your serial number is printed on the development kit box below the bottom bar code. The number is consists of alphanumeric characters, such as *5SGXASxxxxxxxx*, and does not contain hyphens.

2. Consult the Activate Products table, to determine how to proceed.
   a. If the administrator listed for your product is someone other than you, skip the remaining steps and contact your administrator to become a licensed user.
   b. If the administrator listed for your product is you, proceed to step 3.
   c. If the administrator listed for your product is *Stocking*, activate the product, making you the administrator, and proceed to step 3.
3. Use the Create New License page to license your product for a specific user (you) on specific computers. The Manage Computers and Manage Users pages allow you to add users and computers not already present in the licensing system.

   To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

4. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus_II software to enable the software.

For complete licensing details, refer to the *Altera Software Installation and Licensing Manual*.

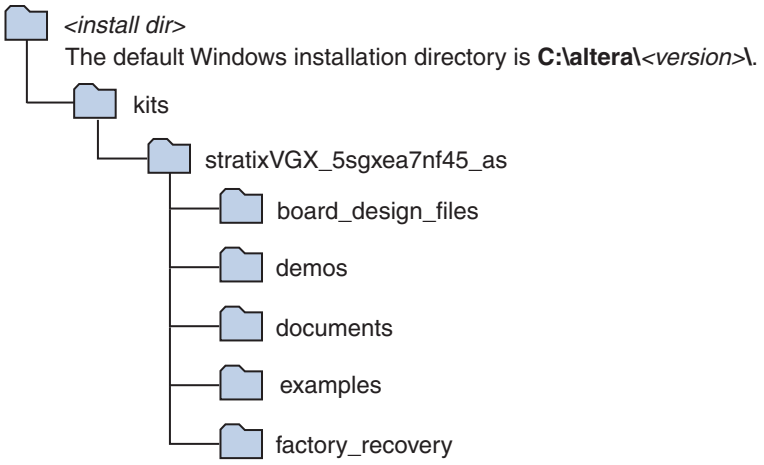
Installing the Stratix V Advanced Systems Development Kit

To install the Stratix V Advanced Systems Development Kit, perform the following steps:

1. Download the Stratix V Advanced Systems Development Kit installer from the Stratix V Advanced Systems Development Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.
2. Run the Stratix V Advanced Systems Development Kit installer.
3. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you choose is in the same relative location to the Quartus II software installation.

The installation program creates the Stratix V Advanced Systems Development Kit directory structure shown in Figure 3–1.

Figure 3–1. Stratix V Advanced Systems Development Kit Installed Directory Structure *(1)*



Note to Figure 3–1:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications when available.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Stratix V Advanced Systems Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster II Driver

The Stratix V GX advanced systems board includes integrated On-Board USB-Blaster II circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster II driver on the host computer.

Installation instructions for the USB-Blaster II driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

4. Development Board Setup

The instructions in this chapter explain how to set up the Stratix V GX advanced systems board.

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Stratix V GX advanced systems board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch and Jumper Settings" on page 4–2 to return the board to its factory settings before proceeding.
2. The advanced systems board ships with design examples stored in the flash memory device. Verify the DIP switch SW4.6 is set to the on (0) position to load the design stored in the factory portion of flash memory. Figure 4–2 shows the DIP switch location on the back of the board.
3. Verify that the HSMC card is installed on connector J1 of the board.
4. Ensure that the power switch SW2 is in the off position.
5. Connect the Power Adpater +15 V, 8.00 A to the DC Power Jack (J7) on the advanced systems board and plug the cord into a power outlet.

   CAUTION: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

   For designs requiring more than 120 W, a PCIe 2x4 ATX connector (J10) providing an additional 12 V and 12.5 A is also available. This is the standard PCIe 2x4 connector in a chassis or available with an ATX power supply.

   Alternatively, the board can be powered by the PCIe host adapter or the laptop power adapter. If you want to power the board by the PCIe host system, plug the FPGA development card into a standard PCIe connector.

6. Set the POWER switch (SW2) to the on position. When power is supplied to the board, the blue LED (D27) illuminates indicating that the board has power.

The MAX V device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. DIP switch SW4.6 controls whether the FPP is active and loads the designs from flash into the Stratix V devices. When the switch is in the on (0) position, the PFL loads the design from flash memory. For FPP to function properly, the MSEL pins for both FPGAs must be set for FPP x8 on MSEL DIP switches SW5 and SW6.

The kit includes a MAX V design which contains the MAX V PFL megafunction. The design resides in the <*install dir*>**\kits\stratixVGX_5sgxea7nf45_as\examples\max5** directory.

When configuration is complete, the Config Done LED (D13) illuminates, signaling that the Stratix V GX devices configured successfully.

For more information about the PFL megafunction, refer to *AN 386: Parallel Flash Loader Megafunction User Guide*.

Factory Default Switch and Jumper Settings

This section shows the factory switch and jumper settings for the Stratix V GX advanced systems board.

Figure 4–1 shows the switch locations and the default position of each switch and jumper on the top side of the board.

Figure 4–1. Default Settings on the Board Top (Detail)

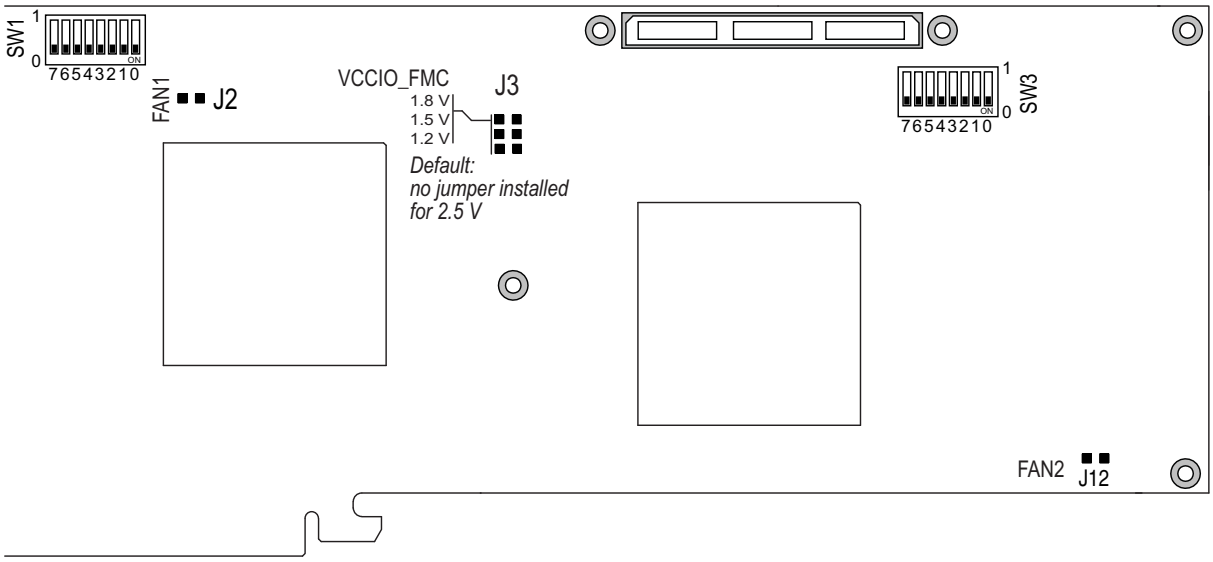
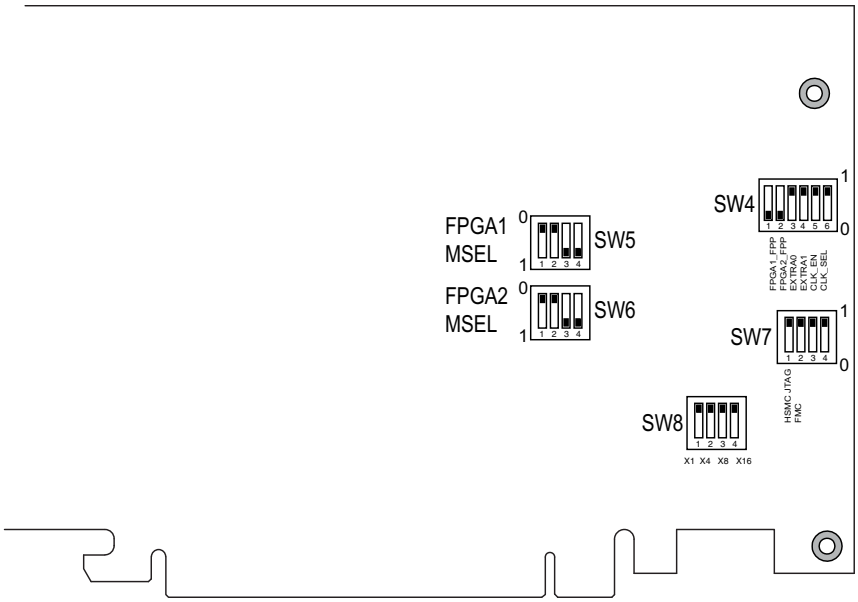


Figure 4–2 shows the switch locations and the default position of each switch on the bottom side of the board.

Figure 4–2. Default Settings on the Board Bottom (Detail)



To restore the switches to their factory default settings, perform the following steps:

1. Set DIP switch (SW4) to match Table 4–1 and Figure 4–2 on page 4–3.

Table 4–1. SW4 DIP Switch Settings

Switch	Board Label	Function	Default Position
1	FPGA1_FPP	Switch 1 has the following options: ■ When on (0), FPP x8 is enabled to configure FPGA1 from flash location 0 and FPGA2 from flash location 1. FPGA1 MSEL (SW5) pins and FPGA2 MSEL (SW6) pins must be set correctly. ■ When off (1), no design is configured to FPGA1 or FPGA2 using FPP x8.	On
2	FPGA2_FPP	—	On
3	EXTRA0	—	Off
4	EXTRA1	—	Off
5	CLK_EN	Switch 5 has the following options: ■ When on (0), the on-board oscillator is disabled. ■ When off (1), the on-board oscillator is enabled.	Off
6	CLK_SEL	Switch 6 has the following options: ■ When on (0), the SMA input clock is selected. ■ When off (1), the programmable oscillator clock is selected.	On

2. Set DIP switch (SW5) to match Table 4–2 and Figure 4–2 on page 4–3.

Table 4–2. SW5 FPGA1 MSEL DIP Switch Settings (1) (2) (3)

Switch	Board Label	Function	Default Position
1	FPGA1 MSEL0	FPGA1 MSEL bit 0 configuration setting	On (0)
2	FPGA1 MSEL1	FPGA1 MSEL bit 1 configuration setting	On (0)
3	FPGA1 MSEL2	FPGA1 MSEL bit 2 configuration setting	Off (1)
4	—	—	—

Notes to Table 4–2:

(1) FPGA1 MSEL[4:3]=10 is hard wired on the board.
(2) FPGA1 MSEL[4:0] to valid configuration schemes as listed in the *Stratix V Device Handbook*.
(3) By default, FPGA1 MSEL is set for FPP x8.

3. Set DIP switch (SW6) to match Table 4–3 and Figure 4–2 on page 4–3.

Table 4–3. SW6 FPGA2 MSEL DIP Switch Settings (1) (2) (3)

Switch	Board Label	Function	Default Position
1	FPGA2 MSEL0	FPGA2 MSEL bit 0 configuration setting	On (0)
2	FPGA2 MSEL1	FPGA2 MSEL bit 1 configuration setting	On (0)
3	FPGA2 MSEL2	FPGA2 MSEL bit 2 configuration setting	Off (1)
4	—	—	—

Notes to Table 4–3:

(1) FPGA2 MSEL[4:3]=10 is hard wired on the board.
(2) FPGA2 MSEL[4:0] to valid configuration schemes as listed in the *Stratix V Device Handbook*.
(3) By default, FPGA2 MSEL is set for FPP x8.

4. Set DIP switch (SW7) to match Table 4–4 and Figure 4–2 on page 4–3.

Table 4–4. SW7 JTAG DIP Switch Settings (1)

Switch	Board Label	Function	Default Position
1	HSMC	Switch 1 has the following options: ■ When on (1), removes the HSMC from the JTAG chain. ■ When off (0), includes the HSMC in the JTAG chain.	On (1)
2	FMC	Switch 1 has the following options: ■ When on (1), removes the FMC from the JTAG chain. ■ When off (0), includes the FMC in the JTAG chain.	On (1)
3	—	—	—
4	—	—	—

Note to Table 4–4:

(1) If you plug in an external USB-Blaster cable to the JTAG header (J11), the On Board USB-Blaster II is disabled. The JTAG chain is normally mastered by the On-board USB-Blaster II.

For details on the JTAG chain, refer to the *Stratix V Advanced Systems Development Board Reference Manual*.

5. Set DIP switch (SW8) to match Table 4–5 and Figure 4–2 on page 4–3.

Table 4–5. SW8 PCIe DIP Switch Settings

Switch	Board Label	Function	Default Position
1	X1	Switch 1 has the following options: ■ When on, x1 presence detect is available. ■ When off, x1 presence detect is unavailable.	Off
2	X4	Switch 2 has the following options: ■ When on, x4 presence detect is available. ■ When off, x4 presence detect is unavailable.	Off
3	X8	Switch 3 has the following options: ■ When on, x8 presence detect is available. ■ When off, x8 presence detect is unavailable.	Off
4	X16	Switch 4 has the following options: ■ When on, x16 presence detect is available. ■ When off, x16 presence detect is unavailable.	Off

6. Set jumper blocks (J2, J3, and J12) to match Table 4–6 and Figure 4–1 on page 4–2.

Table 4–6. Jumper Settings

Board Reference	Description	Shunt Position
J2	Fan 1 — 5 V and GND power	Fan 1 power connected
J3	VCCIO_FMC 1.8 V	Pins 1-2
J3	VCCIO_FMC 1.5 V	Pins 3-4
J3	VCCIO_FMC 1.2 V	Pins 5-6
J3	VCCIO_FMC 2.5 V	Not installed (Default)
J12	Fan 2 — 5 V and GND power	Fan 2 power connected

For more information about the FPGA board settings, refer to the *Stratix V Advanced Systems Development Board Reference Manual*.

5. Board Test System

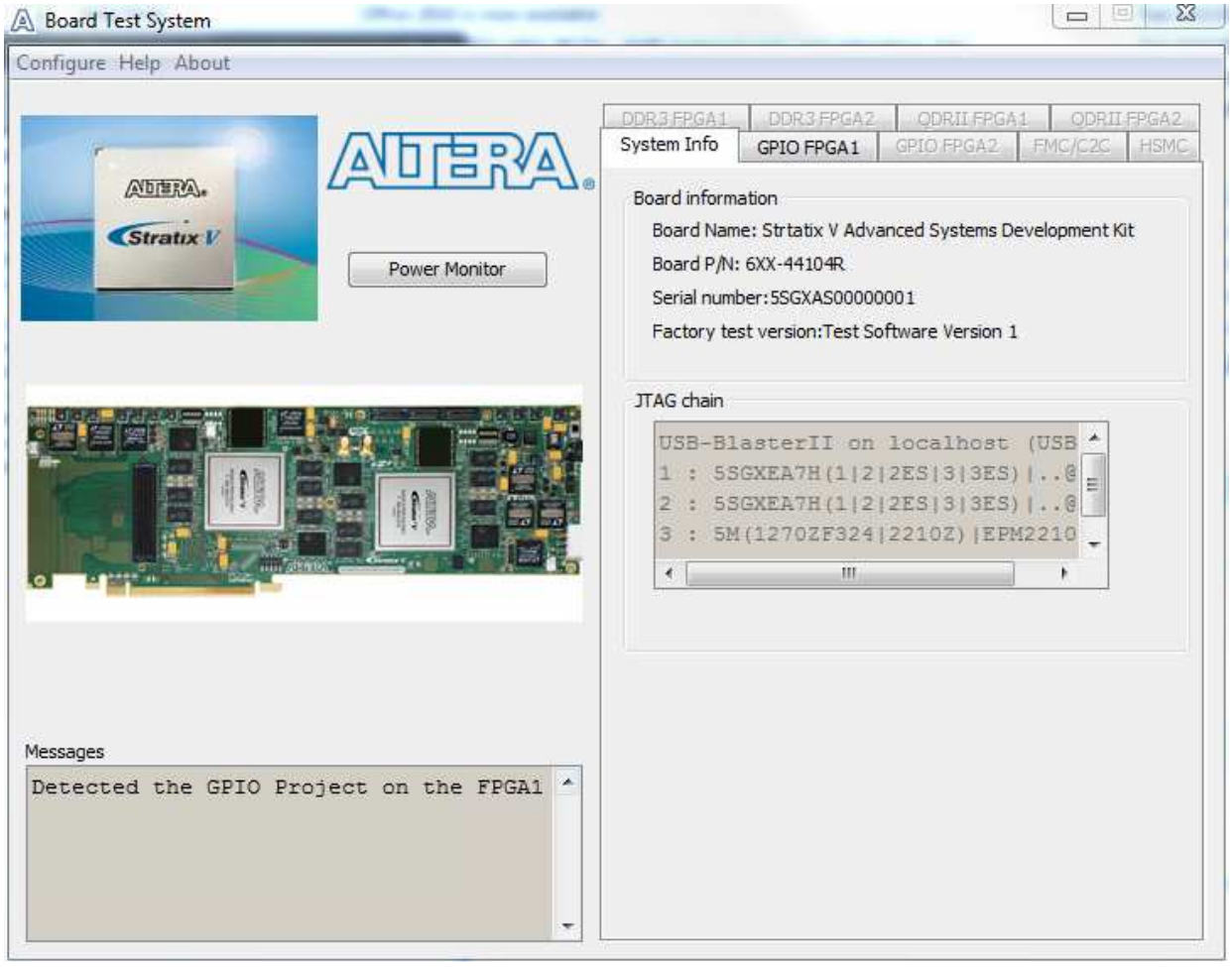
The Stratix V Advanced Systems Development Kit includes an application called the Board Test System (BTS) with related design examples. The BTS provides an easy-to-use interface to alter functional settings and observe the results.

You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage. While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality you are testing. The BTS is also useful as a reference for designing systems.

To install the BTS, follow the steps in "Installing the Stratix V Advanced Systems Development Kit" on page 3–2.

The Board Test System communicates over the JTAG bus to a test design running in the Stratix V GX device. Figure 5–1 shows the initial GUI for a board that is in the factory configuration.

Figure 5–1. Board Test System Graphical User Interface



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The **Power Monitor** button starts the Power Monitor application that measures and reports current power and temperature information for the board. Because the application communicates over the JTAG bus to the MAX V device, you can measure the power of any design in the FPGA, including your own designs.

The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board

With the power to the board off, follow these steps:

1. Connect the mini-USB cable to the board.
2. Ensure that the board DIP switches are set to default positions as shown in the "Factory Default Switch and Jumper Settings" section starting on page 4–2.

   For more information about the board's DIP switch and jumper settings, refer to the *Stratix V Advanced Systems Development Board Reference Manual*.

   FPP x8 mode must be enabled for the BTS functionality to work.

3. Turn on the power to the board. By default, the board loads FPGA1 with the design stored in the factory hardware 0 portion of flash memory and FPGA2 with the factory hardware 1 portion of flash memory. If your board is still in the factory configuration, the design loads the FPGA1 GPIO tests.

   CAUTION

   To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the <*install dir*>**\kits\stratixVGX_5sgxea7nf45_as\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

On Windows, click **Start** > **All Programs** > **Altera** > **Stratix V Advanced Systems Development Kit** <*version*> > **Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The Stratix V GX advanced systems board's flash memory ships preconfigured with the design that corresponds to the GPIO and Flash tabs.

☞ If you power up your board with the DIP switch SW4.6 in a position other than the on (factory default) position, or if you load your own design into the FPGA with the Quartus II Programmer, you receive a message prompting you to configure your board with a valid Board Test System design. Refer to "The Configure Menu" for information about configuring your board.

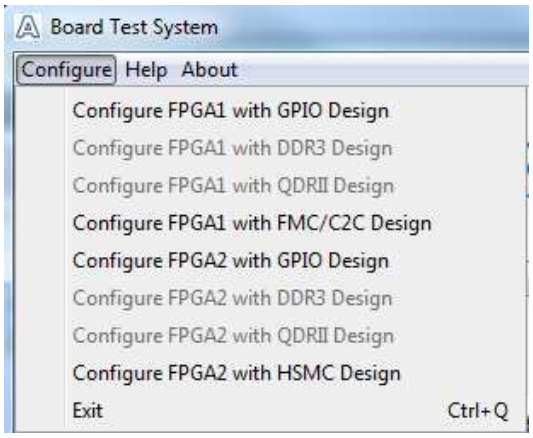
Using the Board Test System

This section describes each control in the Board Test System application.

The Configure Menu

Use the Configure menu (Figure 5–2) to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 5–2. The Configure Menu



To configure the FPGA with a test system design, perform the following steps:

1. Make sure there are no conflicts between the Quartus II software version and the Board Test System GUI version. For example, BTS version 12.1.xx requires Quartus II software version 12.1.
2. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
3. When configuration finishes, close the Quartus II Programmer if open. The design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled.

☞ If the Board Test System is open while you configure FPGAs with the Quartus II Programmer, to use the BTS again, you may need to restart it.

The System Info Tab

The **System Info** tab shows information about the board's current configuration. Figure 5–1 on page 5–1 shows the **System Info** tab. The tab displays the contents of the MAX V registers, the JTAG chain, the flash memory map, and other details stored on the board.

The following sections describe the controls on the **System Info** tab.

Board Information

The **Board information** control displays static information about your board.

- **Board Name**—Indicates the official name of the board.
- **Board P/N**—Indicates the part number of the board.
- **Serial number**—Indicates the serial number of the board.
- **Factory test version**—Indicates the version of the Board Test System currently running on the board.

JTAG Chain

The **JTAG chain** control shows all the devices currently in the JTAG chain. The Stratix V GX devices are always the first devices in the chain, and the MAX V is always the last device in the chain. The JTAG chain is normally mastered by the On-board USB-Blaster II.

If you plug in an external USB-Blaster cable to the JTAG header (J11), the On-Board USB-Blaster II is disabled.

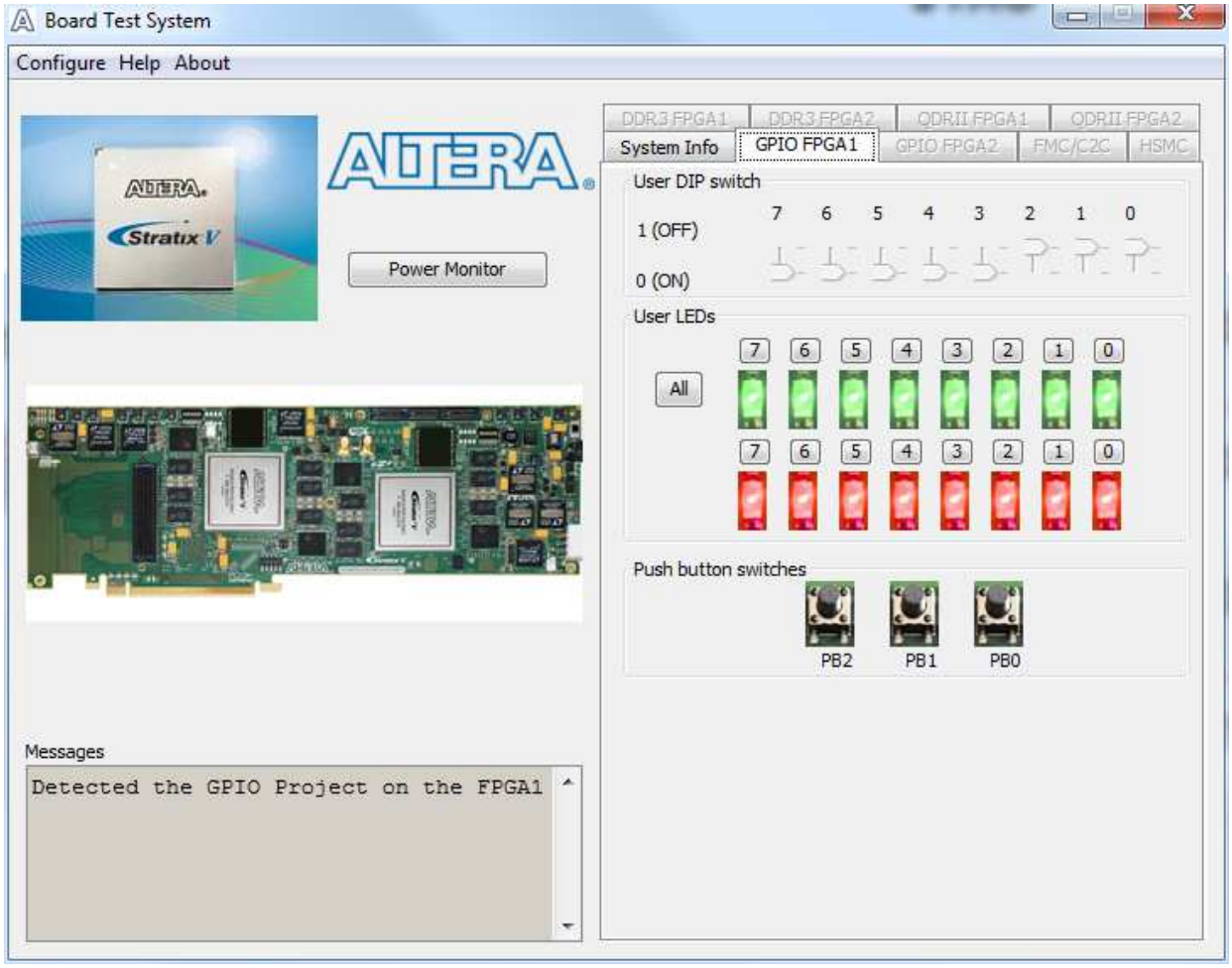
DIP switch SW7 selects which interfaces are in the chain. Set SW7 switch positions in the off position to include the interface in the JTAG chain. Refer to Table 4–4 on page 4–4 for detailed settings.

For details on the JTAG chain, refer to the *Stratix V Advanced Systems Development Board Reference Manual.* For USB-Blaster II configuration details, refer to the On-Board USB-Blaster II page.

The GPIO FPGA1 Tab

The **GPIO FPGA1** tab allows you to interact with all the general purpose user I/O components on your board associated with FPGA1 (U29). You can read DIP switch settings, turn LEDs on or off, and detect push button presses. This test erases FPGA2. Figure 5–3 shows the **GPIO FPGA1** tab.

Figure 5–3. The GPIO FPGA1 Tab



The following sections describe the controls on the **GPIO FPGA1** tab.

User DIP Switches

The read-only **User DIP switch** control displays the current positions of the switches in the user DIP switch bank (SW1). Change the switches on the board to see the graphical display change accordingly.

User LEDs

The **User LEDs** control displays the current state of the user LEDs. To toggle the board LEDs, click the **0** to **7** buttons to toggle red or green LEDs, the **All** button, and the graphical representation of the LEDs.

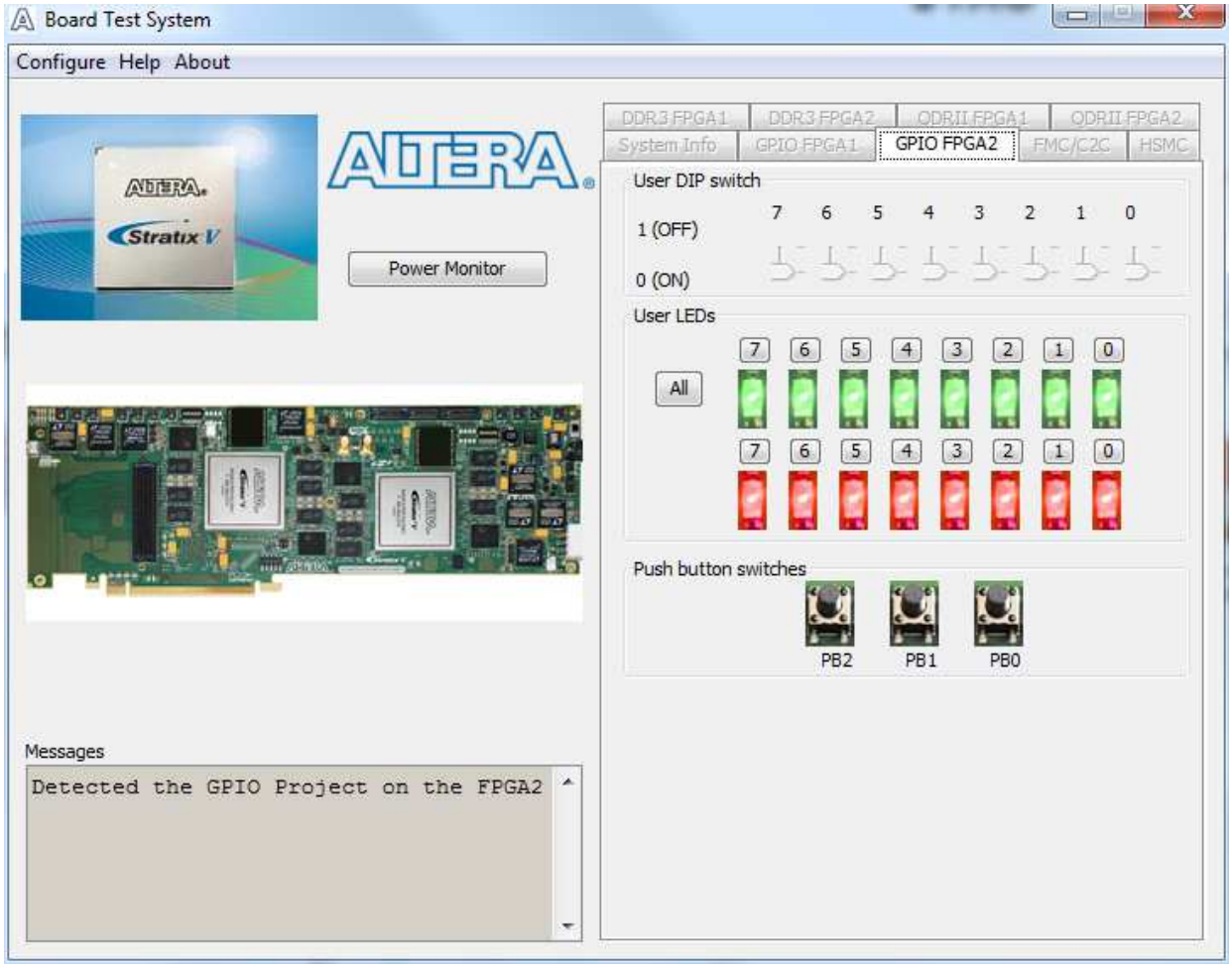
Push Button Switches

The read-only **Push button switches** control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

The GPIO FPGA2 Tab

The **GPIO FPGA2** tab allows you to interact with all the general purpose user I/O components on your board associated with FPGA2 (U35). You can read DIP switch settings, turn LEDs on or off, and detect push button presses. This test erases FPGA1. Figure 5–4 shows the **GPIO FPGA2** tab.

Figure 5–4. The GPIO FPGA2 Tab



The following sections describe the controls on the **GPIO FPGA2** tab.

User DIP Switches

The read-only **User DIP switch** control displays the current positions of the switches in the user DIP switch bank (SW3). Change the switches on the board to see the graphical display change accordingly.

User LEDs

The **User LEDs** control displays the current state of the user LEDs. To toggle the board LEDs, click the **0** to **7** buttons to toggle red or green LEDs, the **All** button, and the graphical representation of the LEDs.

Push Button Switches

The read-only **Push button switches** (S8-S10) control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

The FMC/C2C Tab

The **FMC/C2C** tab allows you to perform loopback tests on the FMC XCVR and FMC parallel ports, Chip-to-Chip (C2C) XCVR, C2C LVDS, and C2C single-ended loopback. FPGA 1 is configured with a design for FMC testing and C2C testing. FPGA2 is configured with a design for C2C testing.

Altera recommends loading the C2C loopback design without Nios configured to FPGA2. Configuring the FPGAs through the BTS GUI handles this by default.