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Arria 10 FPGA Development Kit User Guide

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Contents

Arria 10 FPGA Development Kit Overview

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The Arria® 10 GX FPGA development board provides a hardware platform for evaluating the performance and features of the Altera® Arria 10 GX device.

General Description

Figure 1-1: Arria 10 GX Block Diagram

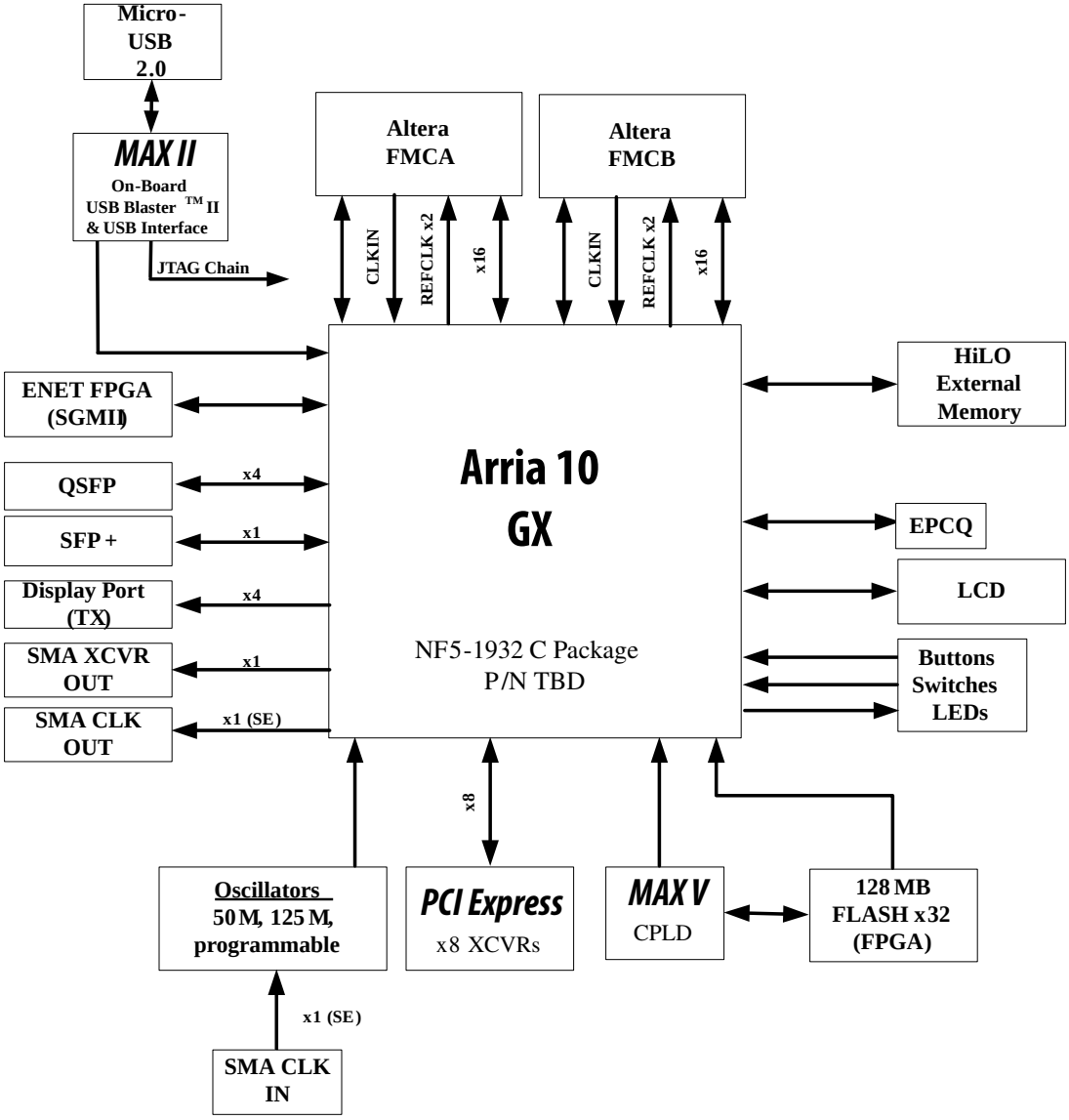


Figure 1-2: Overview of the Development Board Features (ES Edition)

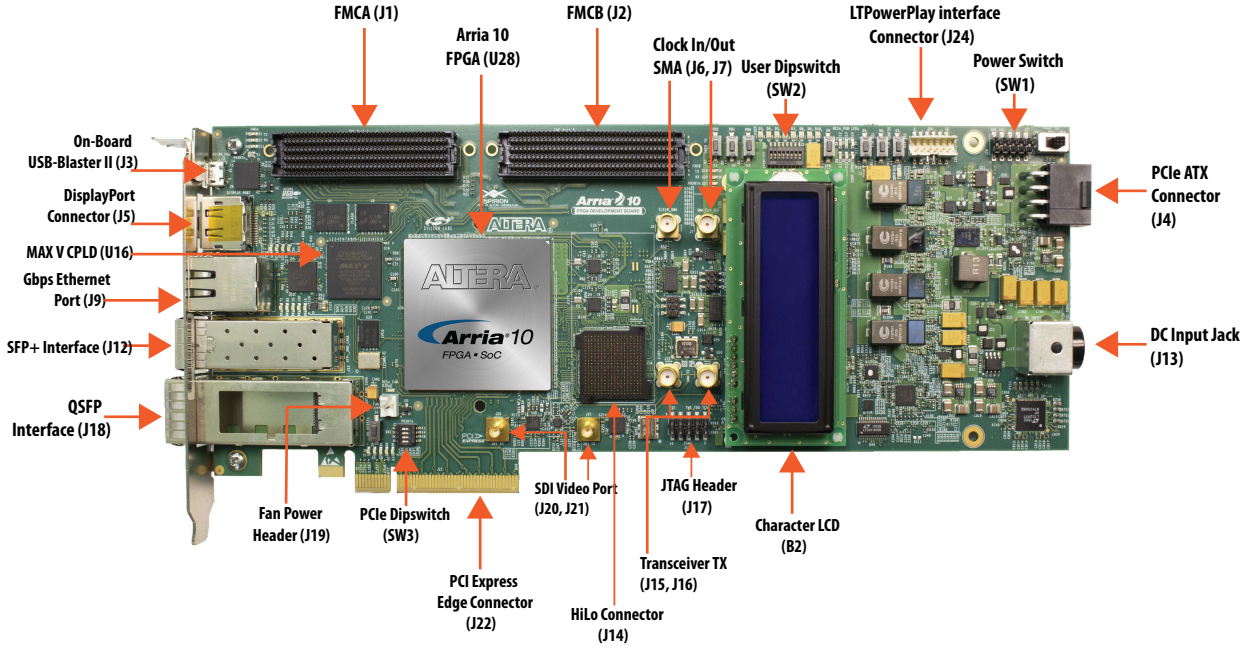
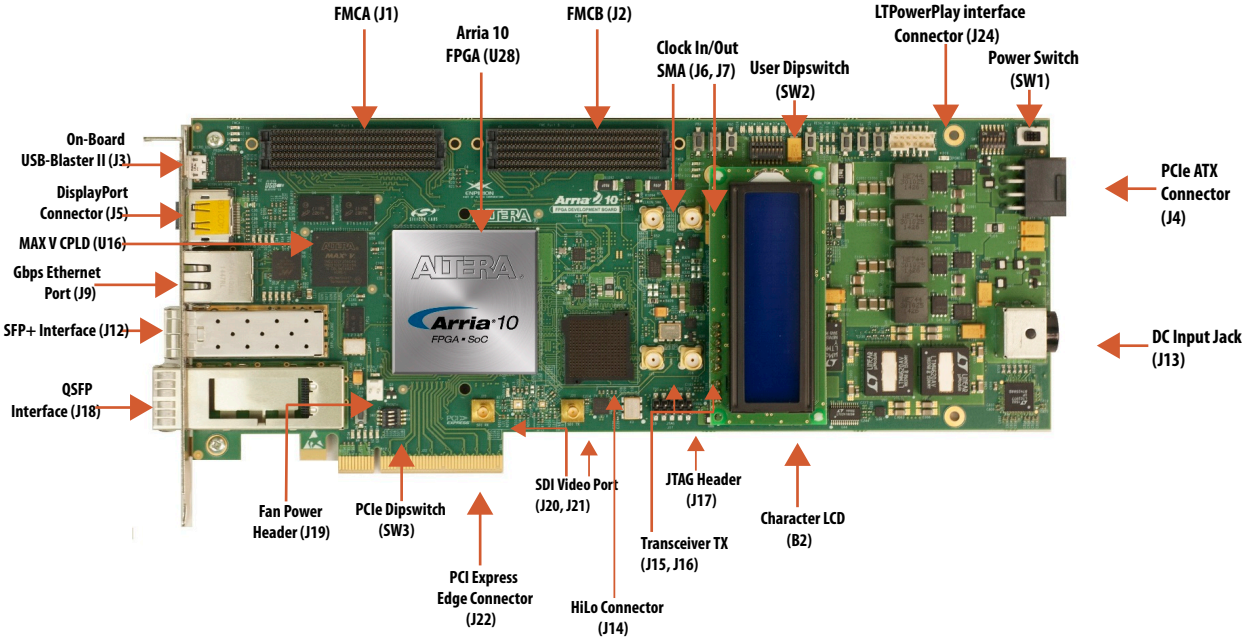


Figure 1-3: Overview of the Development Board Features



Related Information

Board Components on page 6-1
For details on the board components.

Recommended Operating Conditions

- Recommended ambient operating temperature range: 0C to 45C
- Maximum ICC load current: 80A
- Maximum ICC load transient percentage: 35%
- FPGA maximum power supported by the supplied heatsink/fan: 100W

Handling the Board

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Caution: This development kit should not be operated in a Vibration Environment.

Getting Started 2

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Installing the Subscription Edition Software

The Quartus Prime Standard Edition software provides the necessary tools used for developing hardware and software for Altera devices.

Included in the Quartus Prime Standard Edition software are the Quartus Prime software, the Nios II® EDS, and the MegaCore IP Library. To install the Altera development tools, download the Quartus Prime Standard Edition software from the Quartus Prime Standard Edition software page of the Altera website.

Related Information

Quartus Prime Software Page

Activating Your License

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus Prime software. After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus Prime software. To continue using the Quartus Prime software, you should download the free Quartus Prime Lite Edition or purchase a subscription to Quartus Prime Standard or Pro software.

Before using the Quartus Prime software, you must activate your license, identify specific users and computers, and obtain and install a license file. If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, follow these steps:

1. Log on at the **myAltera Account Sign In** web page, and click **Sign In**.
2. On the myAltera Home web page, click the Self-Service Licensing Center link.
3. Locate the serial number printed on the side of the development kit box below the bottom bar code. The number consists of alphanumeric characters and does not contain hyphens.
4. On the Self-Service Licensing Center web page, click the Find it with your License Activation Code link.
5. In the **Find/Activate Products** dialog box, enter your development kit serial number and click **Search**.
6. When your product appears, turn on the check box next to the product name.
7. Click **Activate Selected Products**, and click **Close**.
8. When licensing is complete, Altera emails a `license.dat` file to you. Store the file on your computer and use the License Setup page of the **Options** dialog box in the Quartus Prime software to enable the software.

Related Information

- **Altera Software Installation and Licensing**
  Comprehensive information for installing and licensing Altera software.
- **myAltera Account Sign In web page**

Development Kit Package

1. Download the Arria 10 FPGA Development Kit package zip file available at the Altera website.
2. Extract the contents of the zip file to your hard drive.
   The development kit directory structure is shown in the following figure.

Figure 2-1: Installed Development Kit Directory Structure

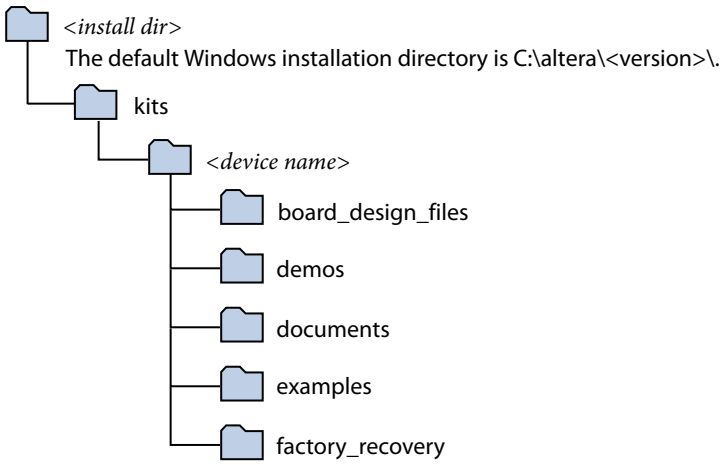

Table 2-1: Installed Directory Contents

Directory Name	Description of Contents
`board_design_files`	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
`demos`	Contains demonstration applications when available.
`documents`	Contains the documentation.
`examples`	Contains the sample design files for this kit.
`factory_recovery`	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Related Information

Link to download zip file for the Arria 10 Development Kit Package

Installing the USB-Blaster Driver

The development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the On-Board USB-Blaster II driver on the host computer.

Installation instructions for the On-Board USB-Blaster II driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

Related Information

Altera Programming Cable Driver Information
Click on the link for your operating system.

Development Board Setup 3

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This section describes how to apply power to the board and provides default switch and jumper settings.

Applying Power to the Board

This development kit ships with its board switches preconfigured to support the design examples in the kit.

If you suspect that your board might not be currently configured with the default settings, follow the instructions in the Default Switch and Jumper Settings section of this chapter.

1. The development board ships with design examples stored in the flash memory device. To load the design stored in the factory portion of flash memory, verify SW6.4 is set to ON. This is the default setting.
2. Connect the supplied power supply to an outlet and the DC Power Jack (J13) on the FPGA board.

   Caution: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.
3. Set the power switch (SW1) to the on position.

When the board powers up, the parallel flash loader (PFL) on the MAX V reads a design from flash memory and configures the FPGA. When the configuration is complete, green LEDs illuminate signaling the device configured successfully. If the configuration fails, the red LED illuminates.

Default Switch and Jumper Settings

This topic shows you how to restore the default factory settings and explains their functions.

Caution: Do not install or remove jumpers (shunts) while the development board is powered on.

Figure 3-1: Default Switch and Jumper Settings on the Top

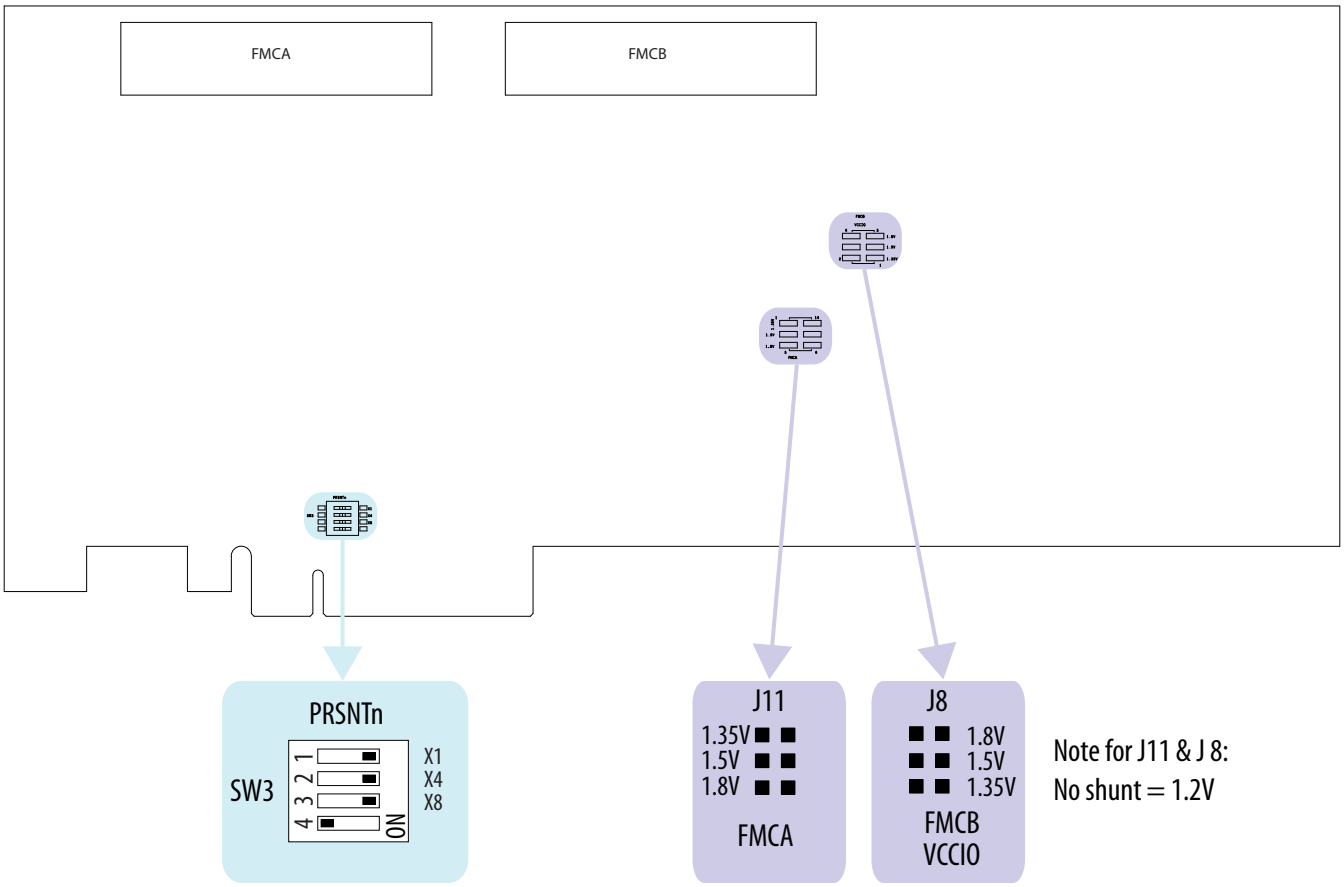
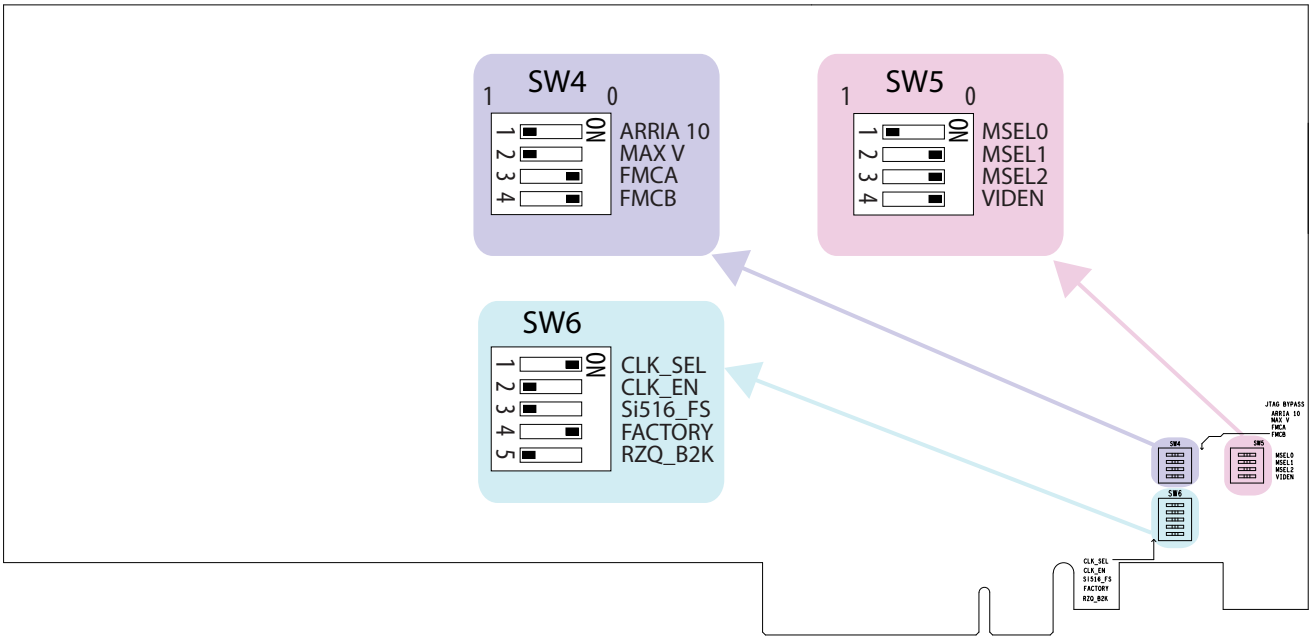


Figure 3-2: Default Switch Settings on the Bottom



1. Set DIP switch bank (SW3) to match the following table.

Table 3-1: SW3 DIP PCIe Switch Default Settings (Board Top)

Switch	Board Label	Function	Default Position
1	x1	ON for PCIe x1	ON
2	x4	ON for PCIe x4	ON
3	x8	ON for PCIe x8	ON
4	—	OFF for 1.35 V MEM_VDD power rail	OFF

2. If all of the jumper blocks are open, the FMCA and FMCB VCCIO value is 1.2 V. To change that value, add shunts as shown in the following table.

Table 3-2: Default Jumper Settings for the FPGA Mezzanine Card (FMC) Ports (Board Top)

Board Reference	Board Label	Description
J8 pins 1-2	1.35V	1.35 V FMCB V_{CCIO} select
J8 pins 3-4	1.5V	1.5 V FMCB V_{CCIO} select
J8 pins 5-6	1.8V	1.8 V FMCB V_{CCIO} select

Board Reference	Board Label	Description
J11 pins 1-2	1.35V	1.35 V FMCA V_{CCIO} select
J11 pins 3-4	1.5V	1.5 V FMCA V_{CCIO} select
J11 pins 5-6	1.8V	1.8 V FMCA V_{CCIO} select

3. Set DIP switch bank (SW4) to match the following table.

Table 3-3: SW4 JTAG DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	ARRIA 10	OFF to enable the Arria 10 in the JTAG chain	OFF
2	MAX V	OFF to enable the MAX V in the JTAG chain	OFF
3	FMCA	ON to bypass the FMCA connector in the JTAG chain	ON
4	FMCB	ON to bypass the FMCB connector in the JTAG chain	ON

4. Set DIP switch bank (SW5) to match the following table.

Table 3-4: SW5 DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	MSEL0	OFF for MSEL0 = 1; for FPP standard mode	OFF
2	MSEL1	ON for MSEL1 = 0; for FPP standard mode	ON
3	MSEL2	ON for MSEL2 = 0; for FPP standard mode	ON
4	VIDEN	OFF for enabling `VID_EN` for the Smart Voltage ID (SmartVID) feature	ON

5. Set DIP switch bank (SW6) to match the following table.

Table 3-5: SW6 DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	CLK_SEL	ON for 100 MHz on-board clock oscillator selection OFF for SMA input clock selection	ON
2	CLK_EN	OFF for setting `CLK_ENABLE` signal high to the MAV V	OFF

Switch	Board Label	Function	Default Position
3	Si516_FS	ON for setting the SDI REFCLK frequency to 148.35 MHz OFF for setting the SDI REFCLK frequency to 148.5 MHz	OFF
4	FACTORY	ON to load factory image from flash OFF to load user image #1 from flash	ON
5	RZQ_B2K	ON for setting RZQ resistor of Bank 2K to 99.17 ohm OFF for setting RZQ resistor of Bank 2K to 240 ohm	OFF

Default Switch and Resistor Settings

This topic shows you how to restore the default factory settings and explains their functions.

Figure 3-3: Default Switch and Resistor Settings on the Top

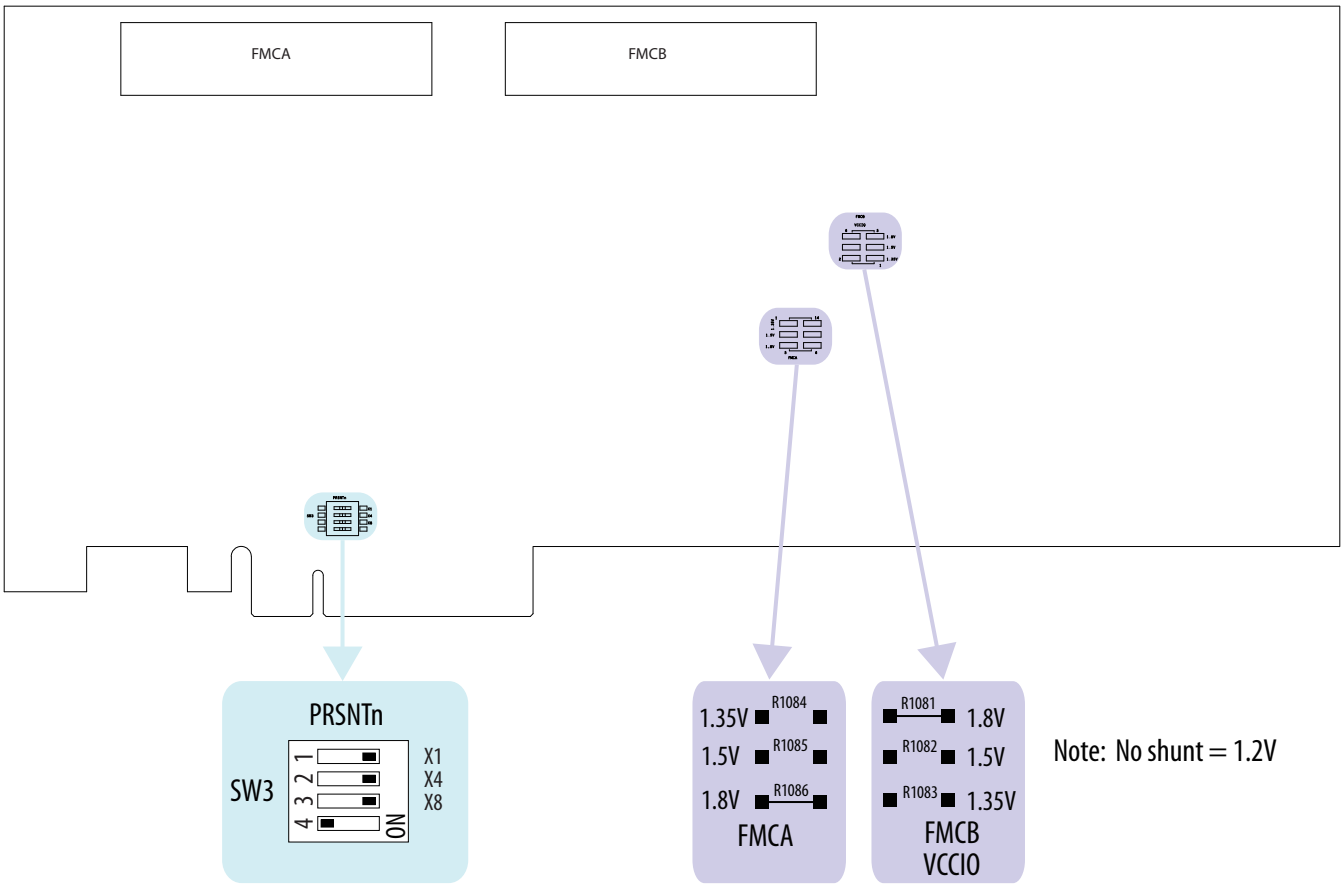
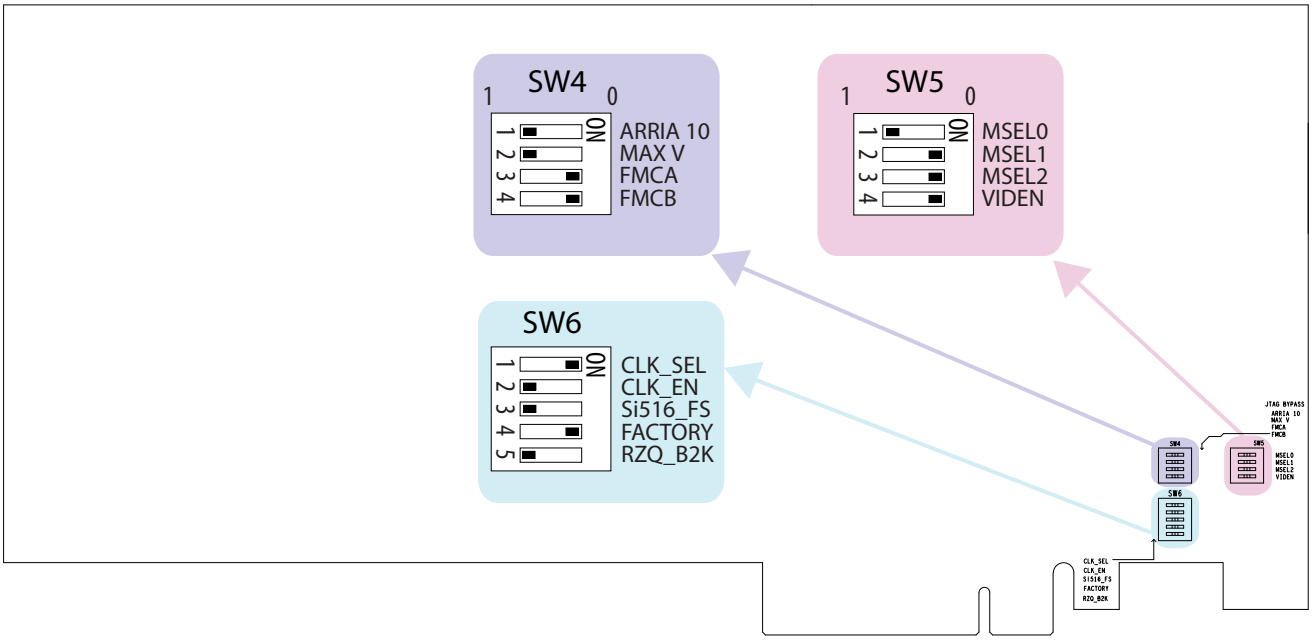


Figure 3-4: Default Switch Settings on the Bottom



1. Set DIP switch bank (SW3) to match the following table.

Table 3-6: SW3 DIP PCIe Switch Default Settings (Board Top)

Switch	Board Label	Function	Default Position
1	x1	ON for PCIe x1	ON
2	x4	ON for PCIe x4	ON
3	x8	ON for PCIe x8	ON
4	—	OFF for 1.35 V MEM_VDD power rail	OFF

2. If all of the resistors are open, the FMCA and FMCB VCCIO value is 1.2 V. To change that value, add resistors as shown in the following table.

Table 3-7: Default Resistor Settings for the FPGA Mezzanine Card (FMC) Ports (Board Top)

Board Reference	Board Label	Description
R1083	1.35V	1.35 V FMCB V_{CCIO} select
R1082	1.5V	1.5 V FMCB V_{CCIO} select
R1081	1.8V	1.8 V FMCB V_{CCIO} select **Note:** A 0 Ohm resistor is installed by default.
R1084	1.35V	1.35 V FMCA V_{CCIO} select
R1085	1.5V	1.5 V FMCA V_{CCIO} select
R1086	1.8V	1.8 V FMCA V_{CCIO} select **Note:** A 0 Ohm resistor is installed by default.

3. Set DIP switch bank (SW4) to match the following table.

Table 3-8: SW4 JTAG DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	ARRIA 10	OFF to enable the Arria 10 in the JTAG chain	OFF
2	MAX V	OFF to enable the MAX V in the JTAG chain	OFF
3	FMCA	ON to bypass the FMCA connector in the JTAG chain	ON
4	FMCB	ON to bypass the FMCB connector in the JTAG chain	ON

4. Set DIP switch bank (SW5) to match the following table.

Table 3-9: SW5 DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	MSEL0	OFF for MSEL0 = 1; for FPP standard mode	OFF
2	MSEL1	ON for MSEL1 = 0; for FPP standard mode	ON
3	MSEL2	ON for MSEL2 = 0; for FPP standard mode	ON
4	VIDEN	OFF for enabling `VID_EN` for the Smart Voltage ID (SmartVID) feature	ON

5. Set DIP switch bank (SW6) to match the following table.

Table 3-10: SW6 DIP Switch Default Settings (Board Bottom)

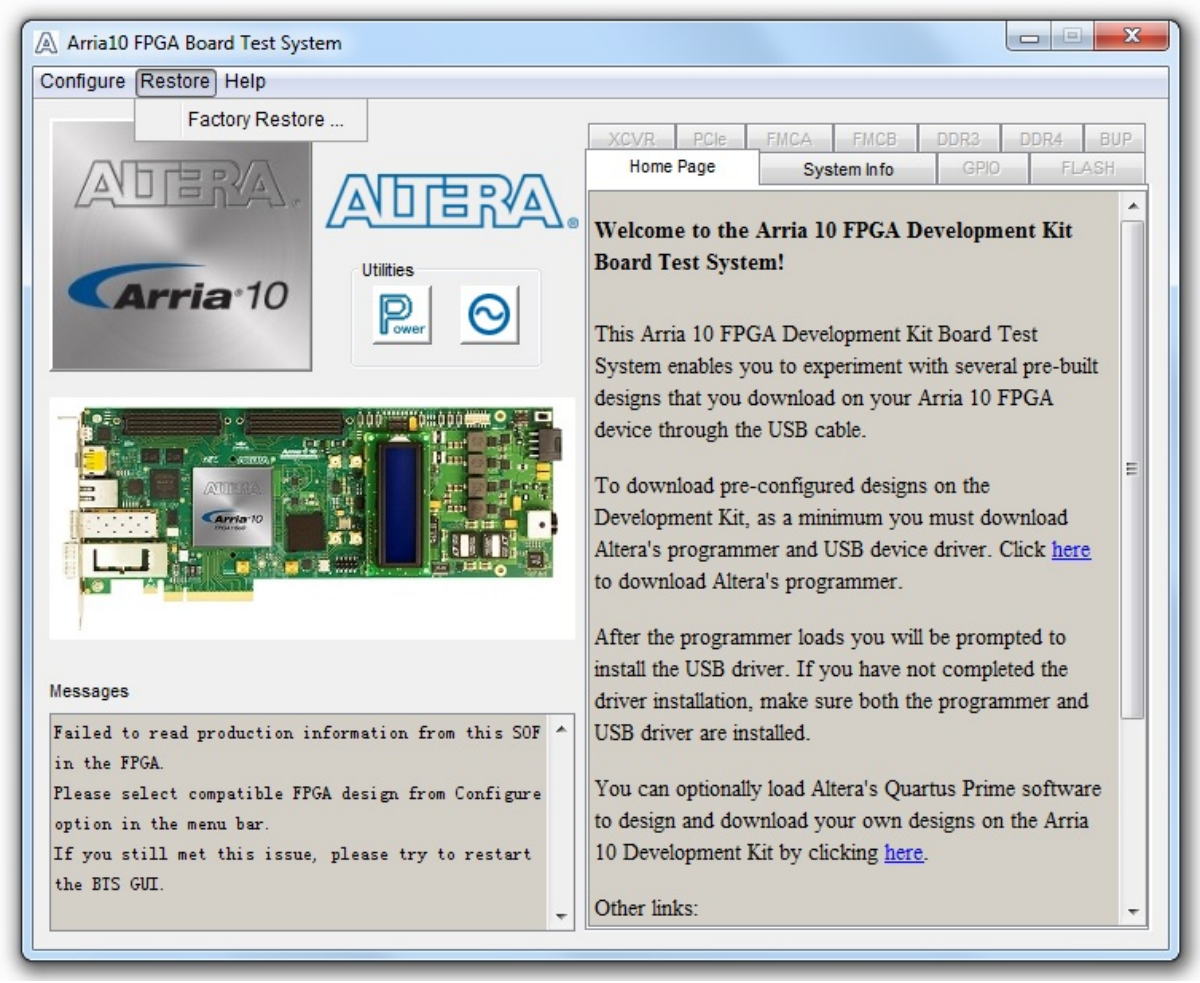
Switch	Board Label	Function	Default Position
1	CLK_SEL	ON for 100 MHz on-board clock oscillator selection OFF for SMA input clock selection	ON
2	CLK_EN	OFF for setting `CLK_ENABLE` signal high to the MAV V	OFF
3	Si516_FS	ON for setting the SDI REFCLK frequency to 148.35 MHz OFF for setting the SDI REFCLK frequency to 148.5 MHz	OFF
4	FACTORY	ON to load factory image from flash OFF to load user image #1 from flash	ON
5	RZQ_B2K	ON for setting RZQ resistor of Bank 2K to 99.17 ohm OFF for setting RZQ resistor of Bank 2K to 240 ohm	OFF

Factory Reset

To do a factory reset, follow these steps:

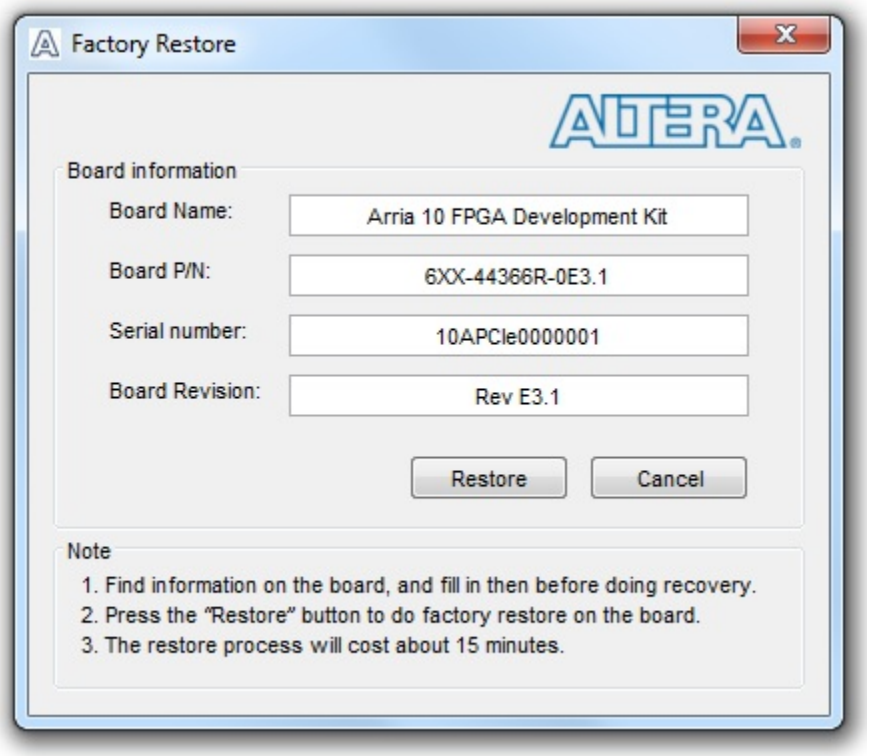
1. Install the latest Altera software tools, including the Quartus Prime software, Nios II processor, and IP functions. If necessary, download the Quartus Prime Pro Edition software from the **Altera Download Center**.
2. Set the board switches to the factory default settings described in "**Default Switch and Resistor Settings**".
3. Open the GUI application "**BoardTestSystem.exe**".
   a. Launch the Nios II command shell, change to directory to `<package dir>\examples\board_test_system\`, and then type in "**./BoardTestSystem.exe**" to open the GUI.
   b. Change directory to `<package dir>\examples\board_test_system\`, and then double click "**BoardTestSystem.exe**" to open the GUI.
4. Select "**Restore** -> **Factory Restore**".

Figure 3-5: Arria 10 FPGA Board Test System Factory Restore Select



5. Set the correct board information and then click restore. The restore process takes about 10 minutes.

Figure 3-6: Factory Restore Window



Related Information

- **Board Update Portal** on page 5-1
- **Using the Board Update Portal to Update User Designs** on page 5-3

Board Test System

4

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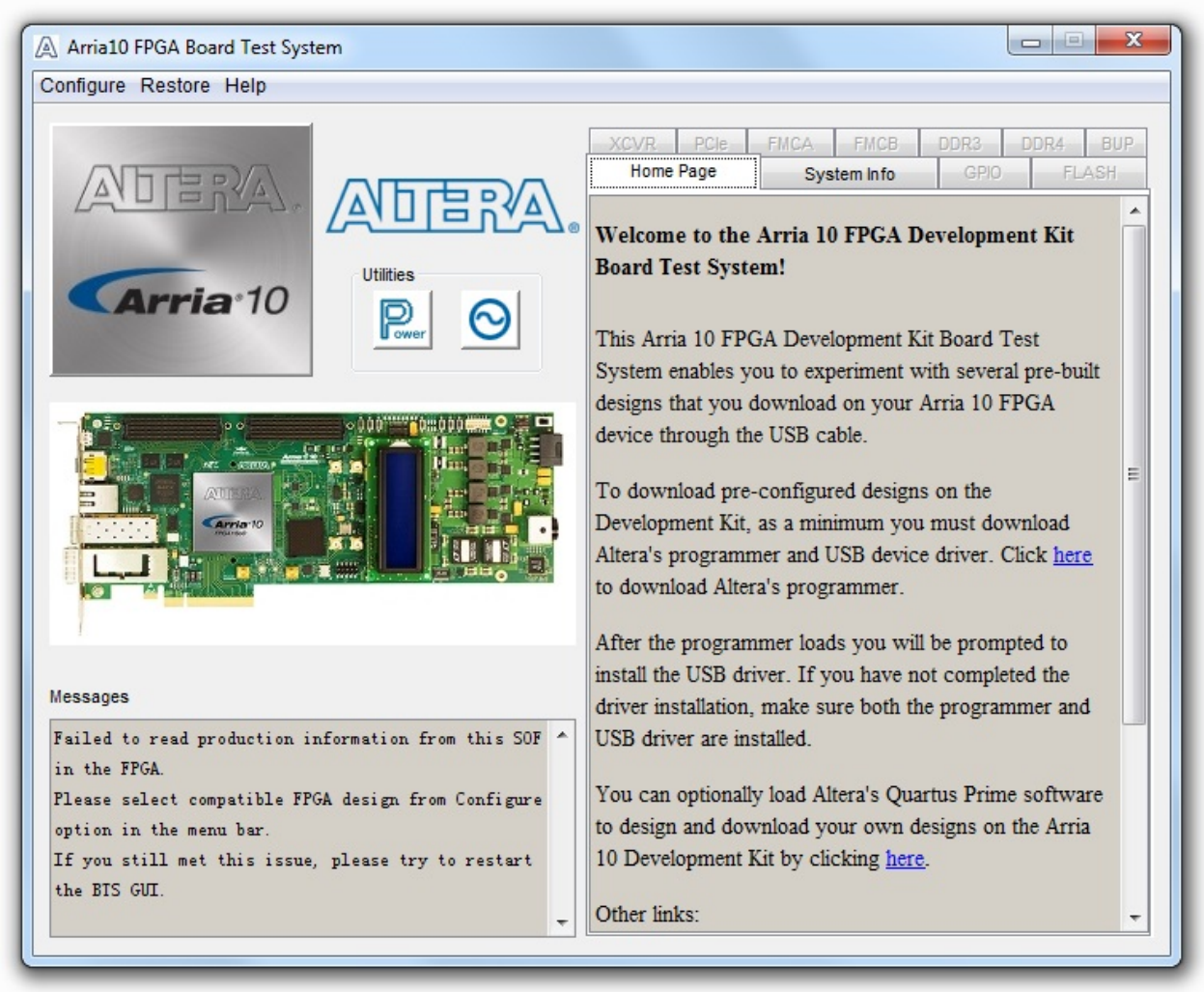
The Board Test System (BTS) provides an easy-to-use interface to alter functional settings and observe the results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage.

Figure 4-1: Board Test System GUI



While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality you are testing. Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears that allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The BTS communicates over the JTAG bus to a test design running in the FPGA. The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the BTS is designed based on the Quartus Programmer and System Console, be sure to close other applications before you use the BTS application.

Preparing the Board

With the power to the board off, follow these steps:

1. Connect the USB cable to your PC and the board.
2. Ensure that the Ethernet patch cord is plugged into the RJ-45 connector.
3. Check the development board switches and jumpers are set according to your preferences. See the "Factory Default Switch and Jumper Settings" section.
4. Set the load selector switch (SW6.4) to OFF for user hardware1 (page #1).

   The development board ships with the CFI flash device preprogrammed with a default:

   - Factory FPGA configuration for running the Board Update Portal design example
   - User configuration for running the Board Test System demonstration
5. Turn on the power to the board. The board loads the design stored in the user hardware1 portion of flash memory into the FPGA. If your board is still in the factory configuration, or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design loads the GPIO, Ethernet, and flash memory tests.

   To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Related Information

Default Switch and Jumper Settings on page 3-2

Running the Board Test System

To run the Board Test System (BTS), navigate to the `<package dir>\examples\board_test_system` directory and run the `BoardTestSystem.exe` application.

On Windows, you can also run the BTS from the **Start** > **All Programs** > **Altera** menu.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The development board's flash memory ships preconfigured with the design that corresponds to the GPIO tab.

Note: The BTS relies on the Quartus Prime software's specific library. Before running the BTS, open the Quartus Prime software. It sets the environment variable `$QUARTUS_ROOTDIR` automatically. The Board Test System uses this environment variable to locate the Quartus Prime library.

The BTS will pick up the Quartus Programmer to configure the FPGA device on your development kit. Make sure the Quartus Prime software you are using is the version supporting the FPGA silicon on the board.

Version Selector

The BTS will prompt you with a Version Selector window once opened. You can also open the Version Selector window through the **Configure** tab by clicking **Select Silicon Version**. Select the silicon version of the Arria 10 device that is installed on your board.

Figure 4-2: Configure Tab Version Selector Option

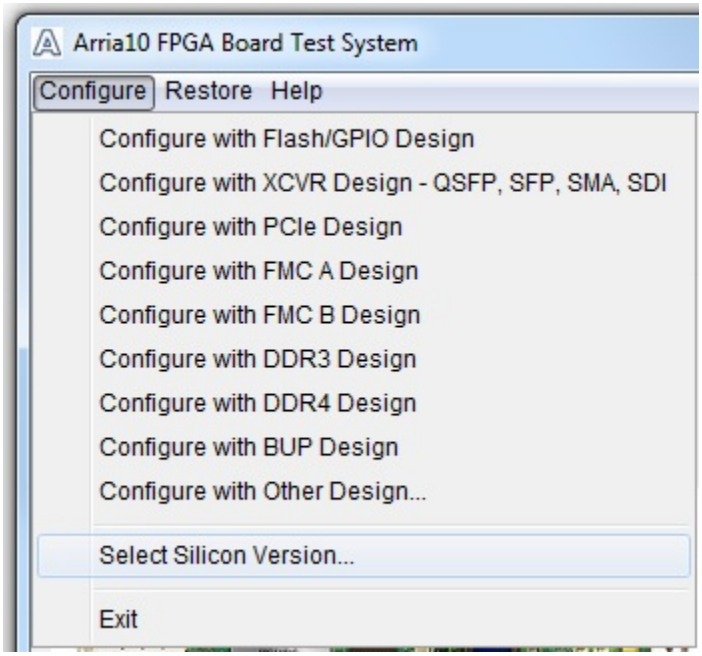


Figure 4-3: Version Selector