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Arria 10 FPGA Development Kit User Guide

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UG-01170
2015.06.26

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San Jose, CA 95134
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Overview 1

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The Arria® 10 GX FPGA development board provides a hardware platform for evaluating the performance and features of the Altera® Arria 10 GX device.

General Description

Figure 1-1: Overview of the Development Board Features

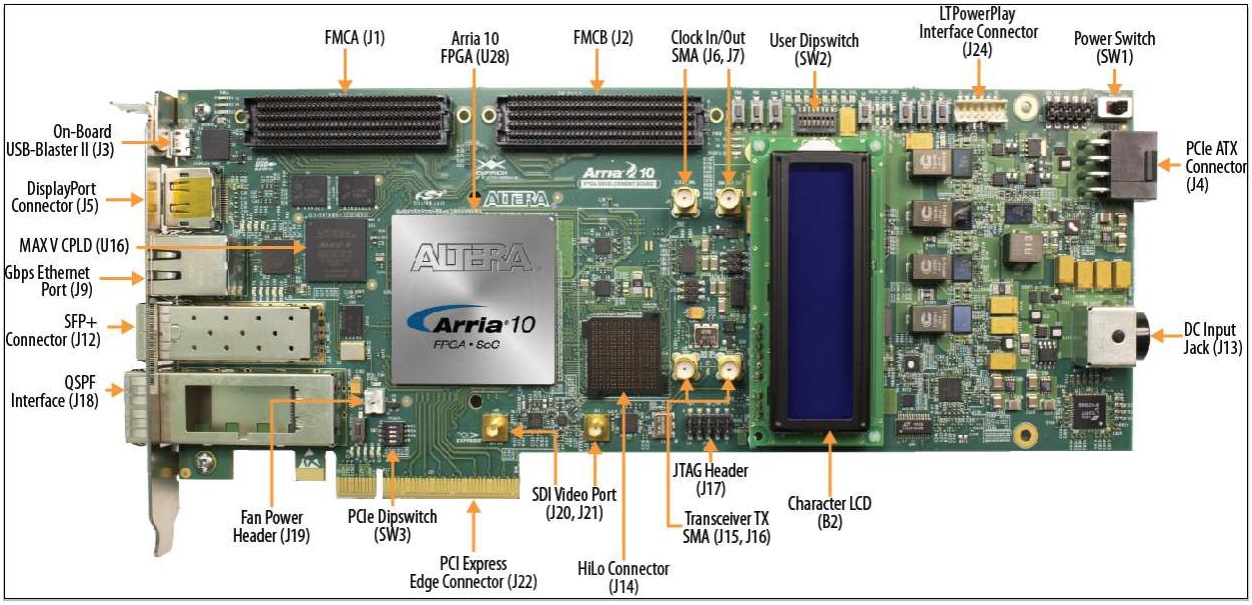

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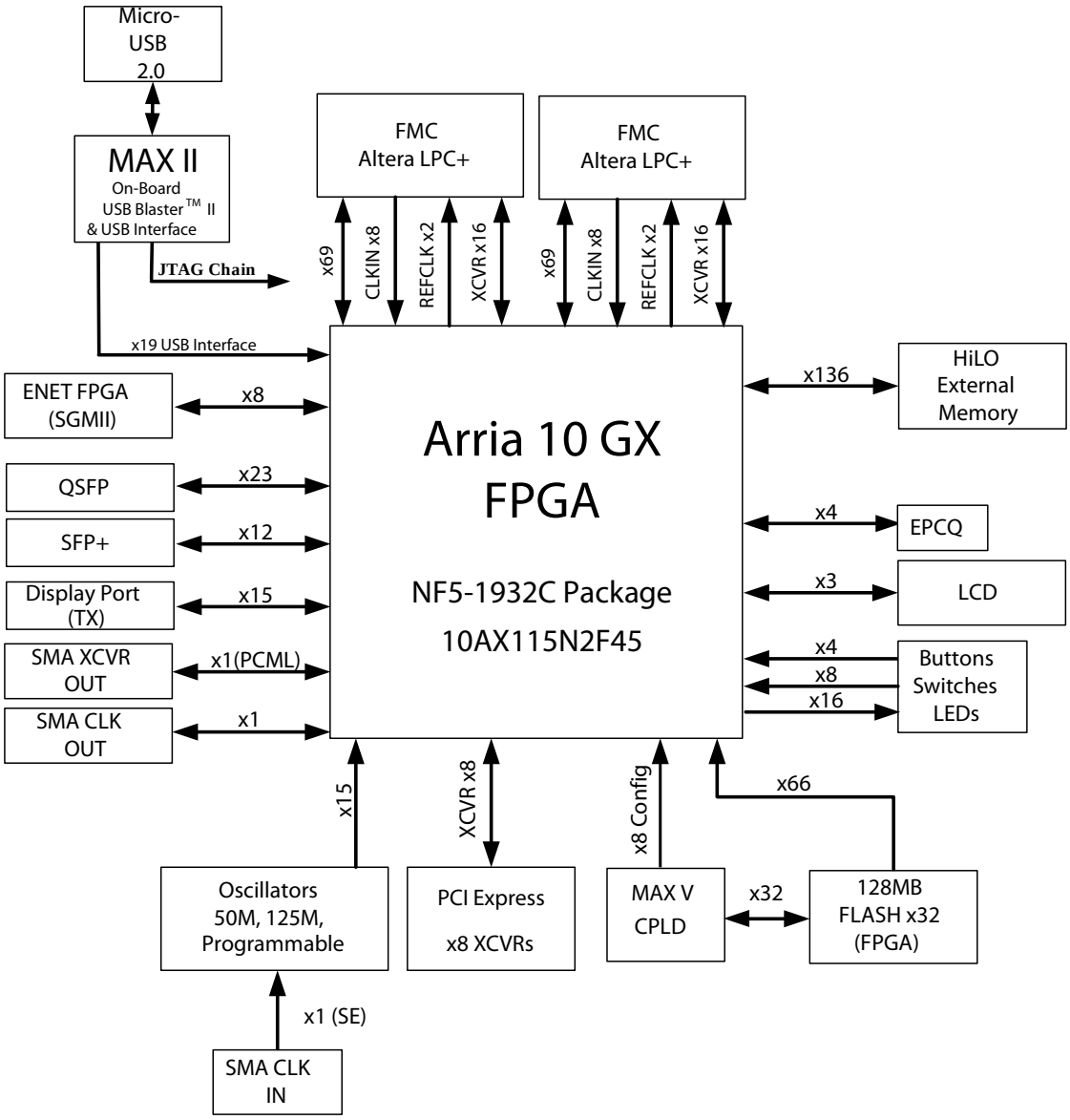
Figure 1-2: Arria 10 GX Block Diagram



Related Information

Board Components on page 5-1
For details on the board components.

Recommended Operating Conditions

- Recommended ambient operating temperature range: 0C to 45C
- Maximum ICC load current: 80A
- Maximum ICC load transient percentage: 35%
- FPGA maximum power supported by the supplied heatsink/fan: 100W

Handling the Board

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Getting Started 2

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Installing the Subscription Edition Software

The Quartus II Subscription Edition Software provides the necessary tools used for developing hardware and software for Altera devices.

Included in the Quartus II Subscription Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. To install the Altera development tools, download the Quartus II Subscription Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.

Related Information

Quartus II Subscription Edition Software page

Activating Your License

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus II software. After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web Edition or purchase a subscription to Quartus II software.

Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file. If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, follow these steps:

1. Log on at the **myAltera Account Sign In** web page, and click **Sign In**.
2. On the myAltera Home web page, click the Self-Service Licensing Center link.
3. Locate the serial number printed on the side of the development kit box below the bottom bar code. The number consists of alphanumeric characters and does not contain hyphens.
4. On the Self-Service Licensing Center web page, click the Find it with your License Activation Code link.
5. In the **Find/Activate Products** dialog box, enter your development kit serial number and click **Search**.

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6. When your product appears, turn on the check box next to the product name.
7. Click **Activate Selected Products**, and click **Close**.
8. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the License Setup page of the **Options** dialog box in the Quartus II software to enable the software.

Related Information

- **Altera Software Installation and Licensing**
  Comprehensive information for installing and licensing Altera software.
- **myAltera Account Sign In web page**

Installing the Development Kit

1. Download the Arria 10 FPGA Development Kit installer from the Arria 10 FPGA Development Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.
2. Run the Arria 10 FPGA Development Kit installer.
3. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you choose is in the same relative location to the Quartus II software installation.
   The installation program creates the development kit directory structure shown in the following figure.

Figure 2-1: Installed Development Kit Directory Structure

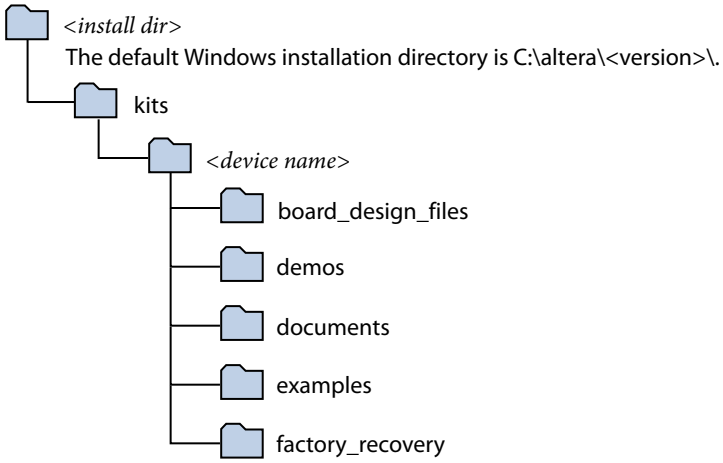

Table 2-1: Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications when available.
documents	Contains the documentation.
examples	Contains the sample design files for this kit.

Directory Name	Description of Contents
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster Driver

The development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the On-Board USB-Blaster II driver on the host computer.

Installation instructions for the On-Board USB-Blaster II driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

Related Information

Altera Programming Cable Driver Information
Click on the link for your operating system.

Development Board Setup 3

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This section describes how to apply power to the board and provides default switch and jumper settings.

Applying Power to the Board

This development kit ships with its board switches preconfigured to support the design examples in the kit.

If you suspect that your board might not be currently configured with the default settings, follow the instructions in the Default Switch and Jumper Settings section of this chapter.

1. The development board ships with design examples stored in the flash memory device. To load the design stored in the factory portion of flash memory, verify SW6.4 is set to OFF. This is the default setting.
2. Connect the supplied power supply to an outlet and the DC Power Jack (J13) on the FPGA board.

   Caution: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.
3. Set the power switch (SW1) to the on position.

When the board powers up, the parallel flash loader (PFL) on the MAX V reads a design from flash memory and configures the FPGA. When the configuration is complete, green LEDs illuminate signaling the device configured successfully. If the configuration fails, the red LED illuminates.

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Default Switch and Jumper Settings

This topic shows you how to restore the default factory settings and explains their functions.

Caution: Do not install or remove jumpers (shunts) while the development board is powered on.

Figure 3-1: Default Switch and Jumper Settings on the Top

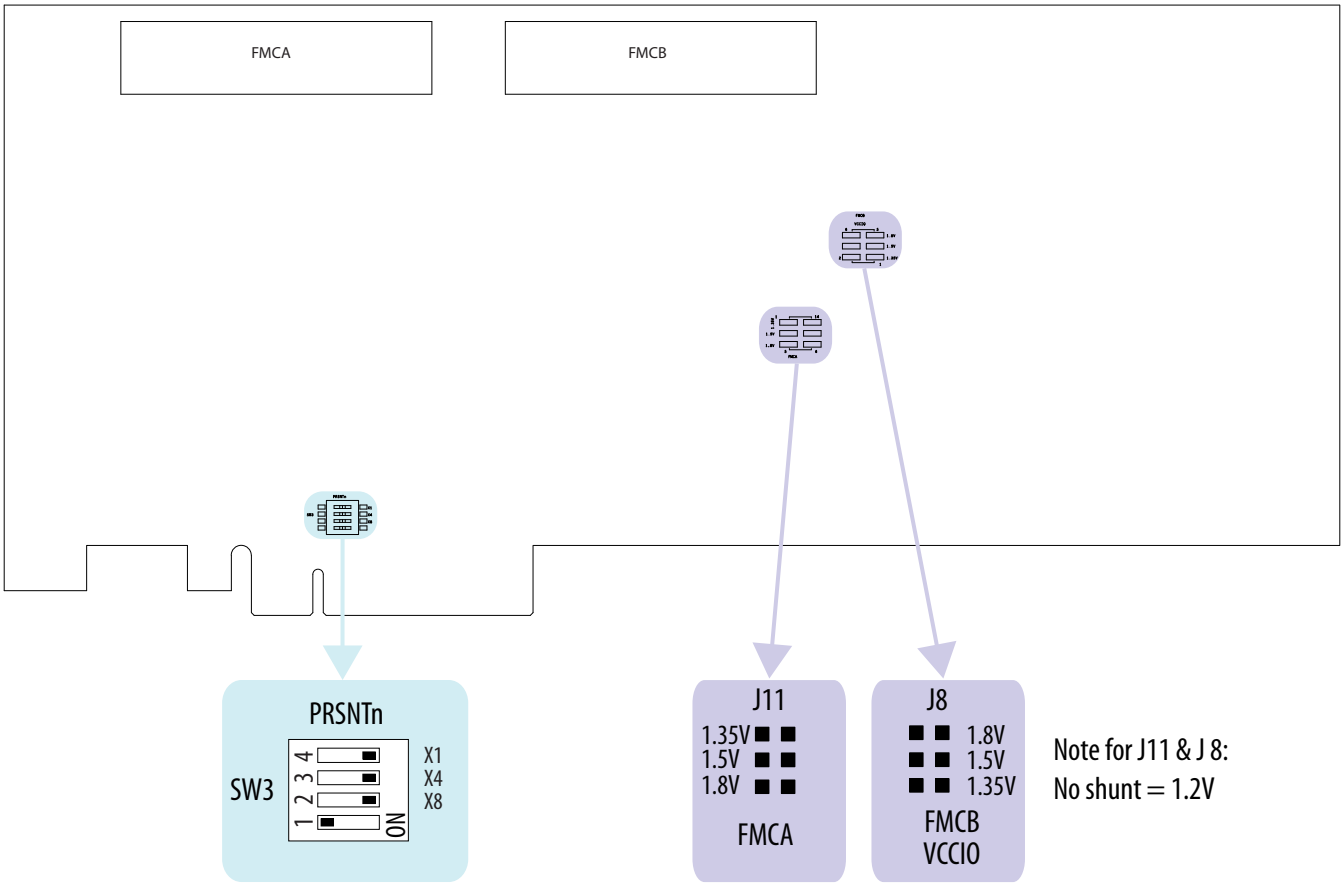
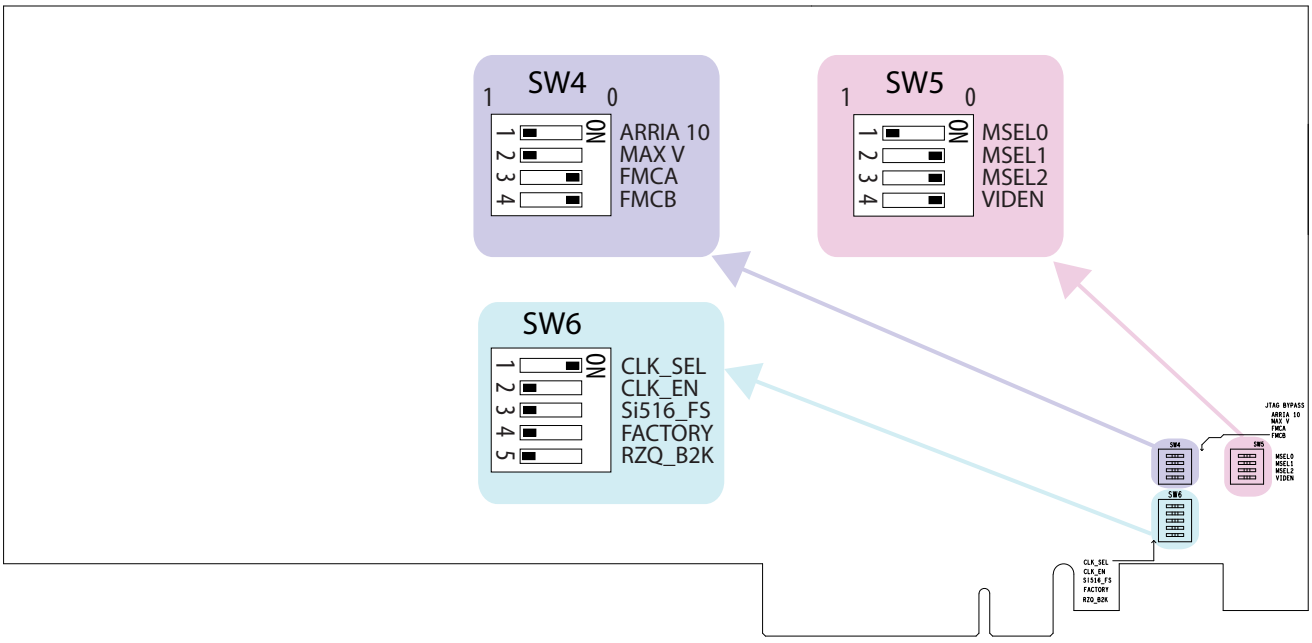


Figure 3-2: Default Switch Settings on the Bottom



1. Set DIP switch bank (SW3) to match the following table.

Table 3-1: SW3 DIP PCIe Switch Default Settings (Board Top)

Switch	Board Label	Function	Default Position
1	x1	ON for PCIe x1	ON
2	x4	ON for PCIe x4	ON
3	x8	ON for PCIe x8	ON
4	—	OFF for 1.35 V MEM_VDD power rail	OFF

2. If all of the jumper blocks are open, the FMCA and FMCB VCCIO value is 1.2 V. To change that value, add shunts as shown in the following table.

Table 3-2: Default Jumper Settings for the FPGA Mezzanine Card (FMC) Ports (Board Top)

Board Reference	Board Label	Description
J8 pins 1-2	1.35V	1.35 V FMCB V_{CCIO} select
J8 pins 3-4	1.5V	1.5 V FMCB V_{CCIO} select
J8 pins 5-6	1.8V	1.8 V FMCB V_{CCIO} select
J11 pins 1-2	1.35V	1.35 V FMCA V_{CCIO} select

Board Reference	Board Label	Description
J11 pins 3-4	1.5V	1.5 V FMCA V_{CCIO} select
J11 pins 5-6	1.8V	1.8 V FMCA V_{CCIO} select

3. Set DIP switch bank (SW4) to match the following table.

Table 3-3: SW4 JTAG DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	ARRIA 10	OFF to enable the Arria 10 in the JTAG chain	OFF
2	MAX V	OFF to enable the MAX V in the JTAG chain	OFF
3	FMCA	ON to bypass the FMCA connector in the JTAG chain	ON
4	FMCB	ON to bypass the FMCB connector in the JTAG chain	ON

4. Set DIP switch bank (SW5) to match the following table.

Table 3-4: SW5 DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	MSEL0	ON for MSEL0 = 1; for FPP standard mode	OFF
2	MSEL1	ON for MSEL1 = 0; for FPP standard mode	ON
3	MSEL2	ON for MSEL2 = 0; for FPP standard mode	ON
4	VIDEN	OFF for enabling `VID_EN` for the Smart Voltage ID (SmartVID) feature	ON

5. Set DIP switch bank (SW6) to match the following table.

Table 3-5: SW6 DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	CLK_SEL	ON for 100 MHz on-board clock oscillator selection OFF for SMA input clock selection	ON
2	CLK_EN	OFF for setting `CLK_ENABLE` signal high to the MAV V	OFF
3	Si516_FS	ON for setting the SDI REFCLK frequency to 148.35 MHz OFF for setting the SDI REFCLK frequency to 148.5 MHz	OFF

Switch	Board Label	Function	Default Position
4	FACTORY	ON to load user hardware1 from flash OFF to load factory from flash	OFF
5	RZQ_B2K	ON for setting RZQ resistor of Bank 2K to 99.17 ohm OFF for setting RZQ resistor of Bank 2K to 240 ohm	OFF

Board Test System

4

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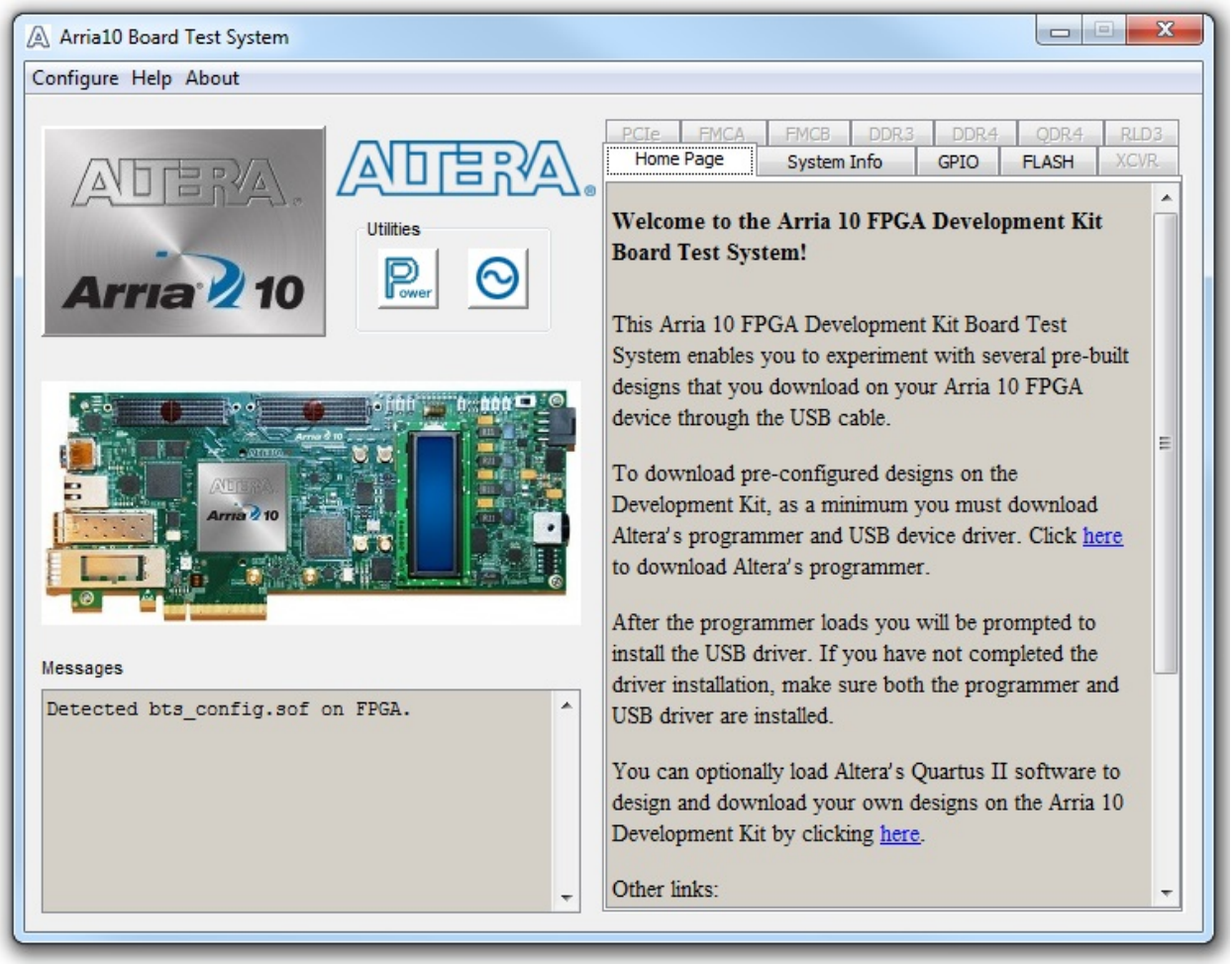
This kit includes an application called the Board Test System (BTS).

The BTS provides an easy-to-use interface to alter functional settings and observe the results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage. While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.

Figure 4-1: Board Test System GUI



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Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears that allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components

The BTS communicates over the JTAG bus to a test design running in the FPGA. The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board

With the power to the board off, follow these steps:

1. Connect the USB cable to your PC and the board.
2. Ensure that the Ethernet patch cord is plugged into the RJ-45 connector.
3. Check the development board switches and jumpers are set according to your preferences. See the "Factory Default Switch and Jumper Settings" section.
4. Set the load selector switch (SW6.4) to OFF for user hardware1 (page #1).

   The development board ships with the CFI flash device preprogrammed with a default:

   - Factory FPGA configuration for running the Board Update Portal design example
   - User configuration for running the Board Test System demonstration
5. Turn on the power to the board. The board loads the design stored in the user hardware1 portion of flash memory into the FPGA. If your board is still in the factory configuration, or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design loads the GPIO, Ethernet, and flash memory tests.

   To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Related Information

Default Switch and Jumper Settings on page 3-2

Running the Board Test System

To run the Board Test System (BTS), navigate to the **<*install dir*> \kits\<*device name*>\examples\board_test_system** directory and run the **BoardTestSystem(32-bit).exe or BoardTestSystem(64-bit).exe** application.

On Windows, you can also run the BTS from the **Start** > **All Programs** > **Altera** menu.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The development board's flash memory ships preconfigured with the design that corresponds to the GPIO tab.

Note: The BTS relies on the Quartus II software's specific library. Before running the BTS, open the Quartus II software. It sets the environment variable `$QUARTUS_ROOTDIR` automatically. The Board Test System uses this environment variable to locate the Quartus II library.

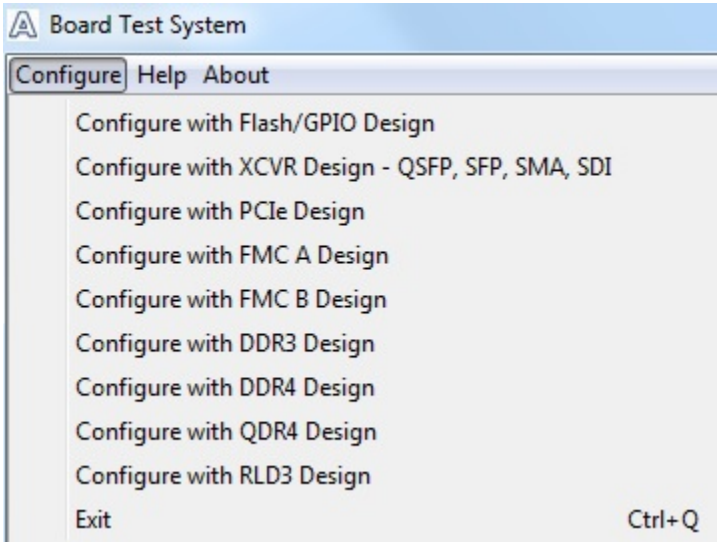
Using the Board Test System

This section describes each control in the Board Test System application.

Using the Configure Menu

Use the Configure menu to select the design you want to use. Each design example tests different board features. Choose a design from this menu and the corresponding tabs become active for testing.

Figure 4-2: The Configure Menu



To configure the FPGA with a test system design, perform the following steps:

1. On the **Configure** menu, click the configure command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design to the FPGA.
3. When configuration finishes, close the Quartus II Programmer if open. The design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled.

If you use the Quartus II Programmer for configuration, rather than the Board Test System GUI, you may need to restart the GUI.

The System Info Tab

The System Info tab shows the board's current configuration. The tab displays the contents of the MAX V registers, the JTAG chain, the board's MAC address, the Qsys memory map, and other details stored on the board.

Figure 4-3: The System Info Tab

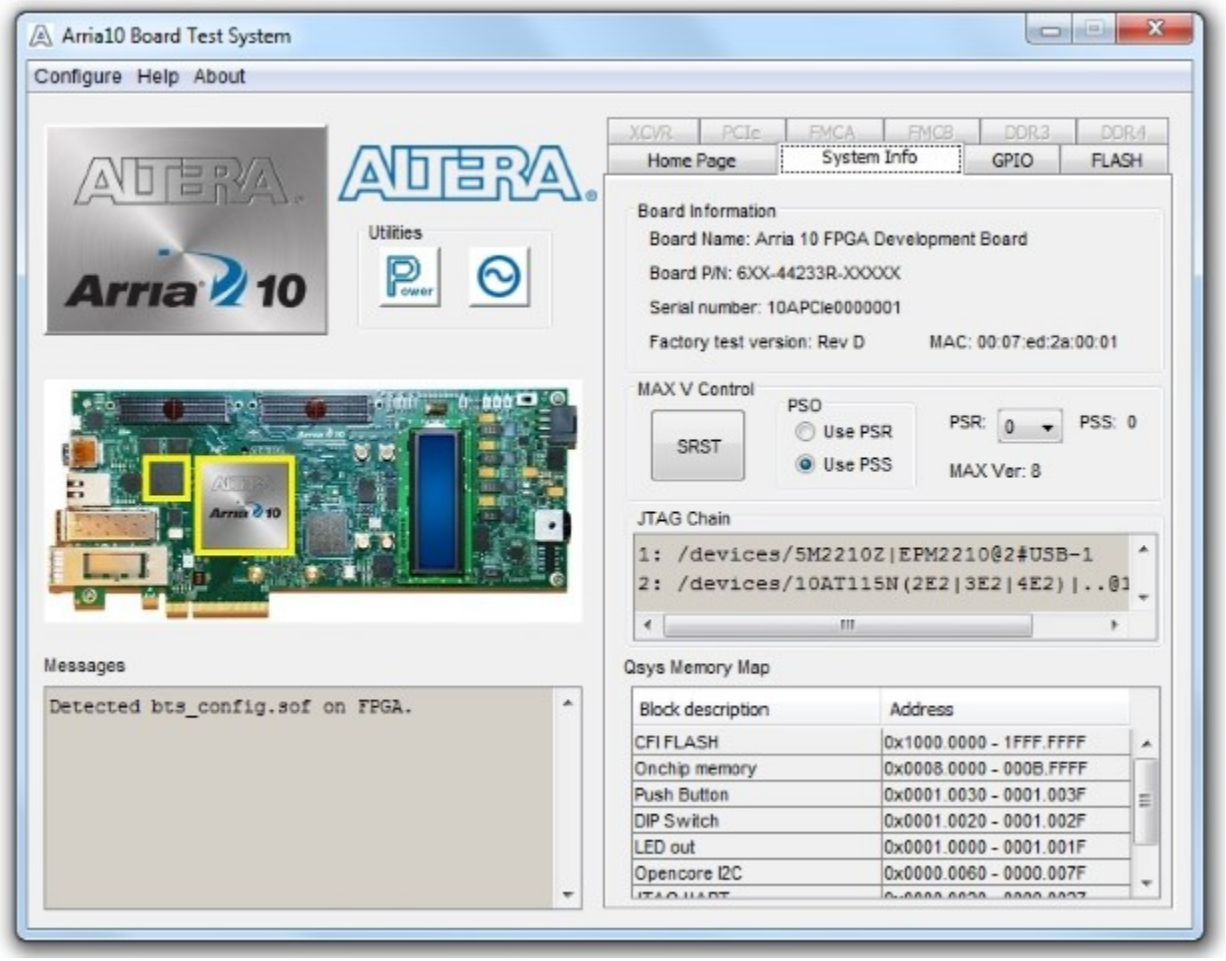


Table 4-1: Controls on the System Info Tab

Controls	Description
Board Information Controls	The board information is updated once the GPIO design is configured. Otherwise, this control displays the default static information about your board.
Board Name	Indicates the official name of the board, given by the Board Test System.
Board P/N	Indicates the part number of the board.
Serial Number	Indicates the serial number of the board.

Controls	Description
Factory Test Version	Indicates the version of the Board Test System currently running on the board.
MAC	Indicates the MAC address of the board.
MAX V Control	Allows you to view and change the current register values, which take effect immediately: System Reset (SRST) — Write only. Click to reset the FPGA. Page Select Override (PSO) — Read/Write Page Select Register (PSR) — Read/Write Page Select Switch (PSS) — Read only MAX Ver: Indicates the version of MAX V code currently running on the board.
JTAG Chain	Shows all the devices currently in the JTAG chain.
Qsys Memory Map	Shows the memory map of the Qsys system on your board.

The GPIO Tab

The GPIO tab allows you to interact with all the general purpose user I/O components on your board. You can write to the character LCD, read DIP switch settings, turn LEDs on or off, and detect push button presses.

Figure 4-4: The GPIO Tab

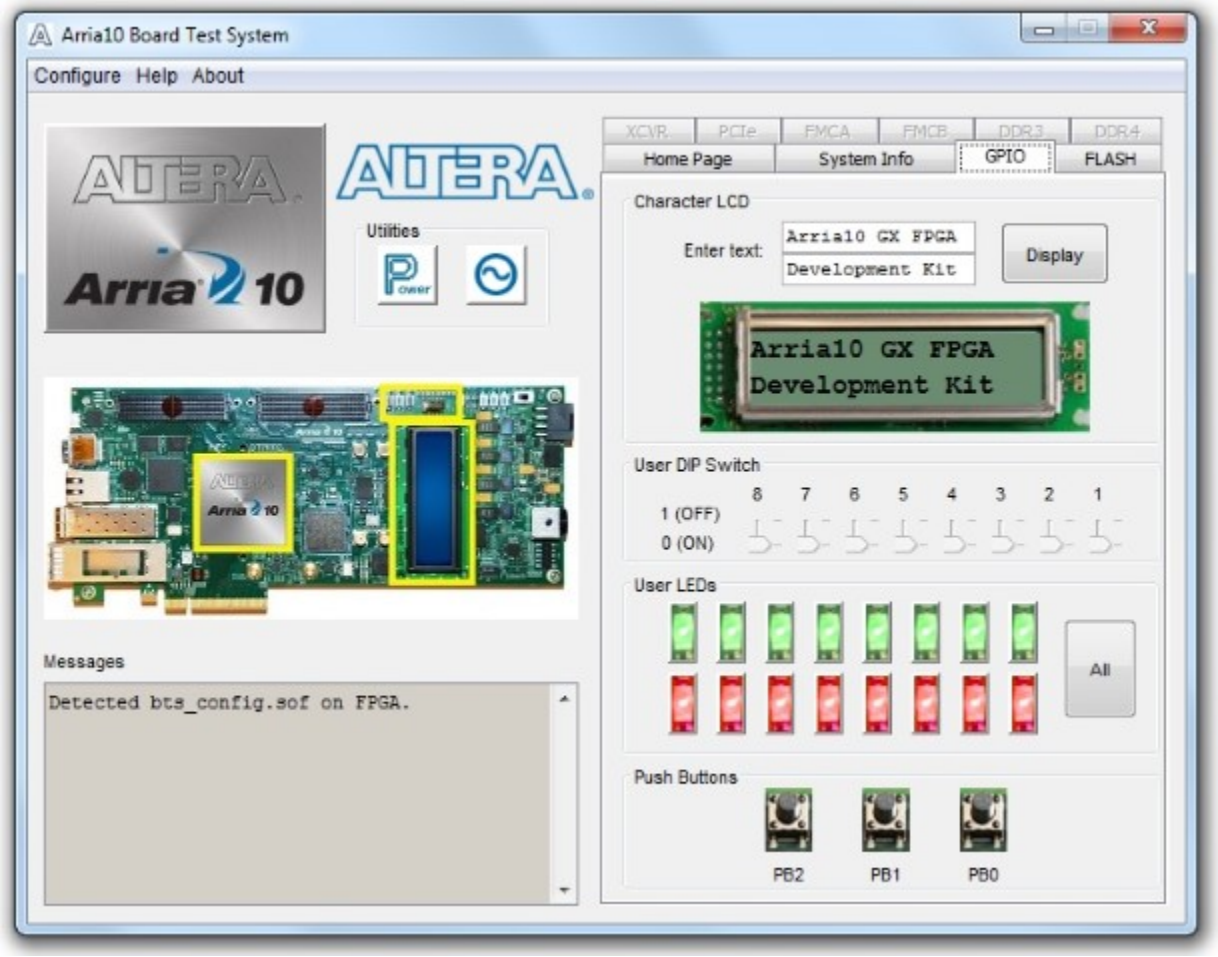


Table 4-2: Controls on the GPIO Tab

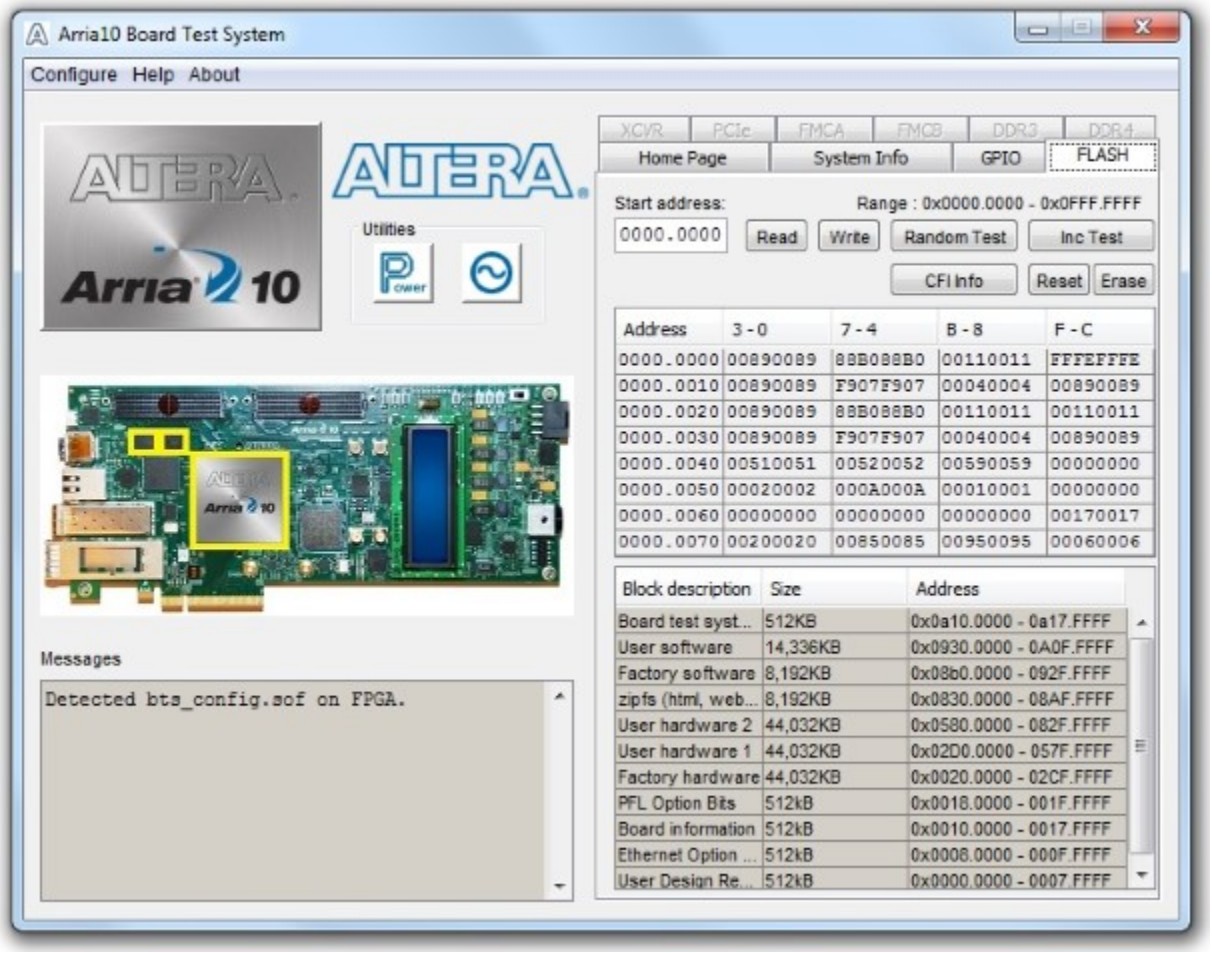
Character LCD	Allows you to display text strings on the character LCD on your board. Type text in the text boxes and then click **Display**.
User DIP Switch	Displays the current positions of the switches in the user DIP switch bank (SW2). Change the switches on the board to see the graphical display change accordingly.
User LEDs	Displays the current state of the user LEDs for the FPGA. To toggle the board LEDs, click the **0** to **7** buttons to toggle red or green LEDs, or click the **All** button.

Push Button Switches	Read-only control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

The Flash Tab

The **Flash Tab** allows you to read and write flash memory on your board. The memory table will display the CFI ROM table contents by default after you configure the FPGA.

Figure 4-5: The Flash Tab



Control	Description
Read	Reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click Read. Values starting at the specified address appear in the table.
Write	Writes the flash memory on your board. To update the flash memory contents, change values in the table and click Write. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.
Random Test	Starts a random data pattern test to flash memory, limited to the 512 K test system scratch page.

Control	Description
CFI Query	Updates the memory table, displaying the CFI ROM table contents from the flash device.
Increment Test	Starts an incrementing data pattern test to flash memory, limited to the 512 K test system scratch page.
Reset	Executes the flash device's reset command and updates the memory table displayed on the **Flash** tab.
Erase	Erases flash memory.
Flash Memory Map	Displays the flash memory map for the development board.

The XCVR Tab

This tab allows you to perform loopback tests on the QSFP, SFP, SMA, and SDI ports.

Figure 4-6: The XCVR Tab