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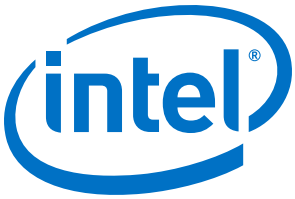

Intel® Stratix® 10 GX FPGA Development Kit User Guide

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Contents

1. Overview

The Stratix® 10 GX FPGA development board provides a hardware platform for evaluating the performance and features of the Intel® Stratix 10 GX device.

This development board comes in two different versions as shown in the table below.

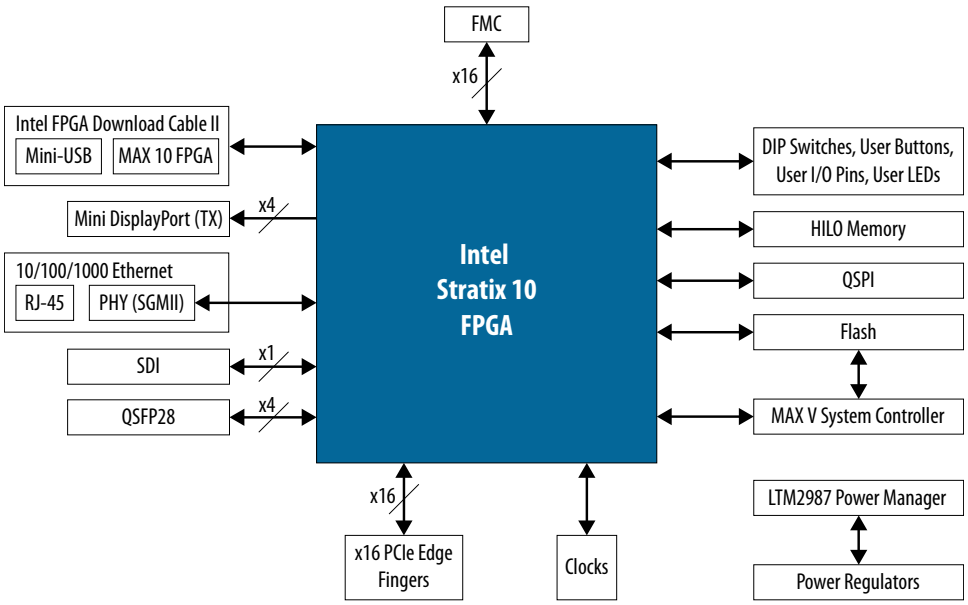
Table 1. Stratix 10 GX FPGA Development Kit Versions

Version	Ordering Code
Stratix 10 GX FPGA L-Tile	DK-DEV-1SGX-L-A
Stratix 10 GX FPGA H-Tile	DK-DEV-1SGX-H-A

Board and FPGA capabilities vary depending on the development kit version selected. For more information on the Stratix 10 L-tile and H-tile, refer to Stratix 10 FPGA product page on Intel's website.

1.1. General Development Board Description

Figure 1. Stratix 10 GX Block Diagram



1.2. Recommended Operating Conditions

- Recommended ambient operating temperature range: 0C to 45C
- Maximum ICC load current: 100 A
- Maximum ICC load transient percentage: 30 %
- FPGA maximum power supported by the supplied heatsink/fan: 200 W

1.3. Handling the Board

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Caution: This development kit should not be operated in a Vibration environment.

2. Getting Started

2.1. Installing Quartus Prime Software

The new Intel Quartus® Prime Design Suite design software includes everything needed to design for Intel FPGAs, SoCs and CPLDs from design entry and synthesis to optimization, verification and simulation. The Intel Quartus Prime Design Suite software includes an additional Spectra-Q® engine that is optimized for future devices. The Spectra-Q engine enables new levels of design productivity for next generation programmable devices with a set of faster and more scalable algorithms, a hierarchical database infrastructure and a unified compiler technology.

The Intel Quartus Prime Design Suite software is available in three editions based on specific design requirements: Pro, Standard, and Lite Edition. The Intel Stratix 10 FPGA Development Kit is supported by the Intel Quartus Prime Pro Edition.

Intel Quartus Prime Pro Edition: The Intel Quartus Prime Pro Edition is optimized to support the advanced features in Intel's next generation FPGAs and SoCs, starting with the Intel Arria® 10 device family and requires a paid license.

Included in the Intel Quartus Prime Pro Edition are the Intel Quartus Prime software, Nios® II EDS and the MegaCore IP Library. To install Intel's development tools, download the Intel Quartus Prime Pro Edition software from the Intel Quartus Prime Pro Edition page in the Download Center of Intel's website.

2.1.1. Activating Your License

Before using the Intel Quartus Prime software, you must activate your license, identify specific users and computers and obtain and install license file. If you already have a licensed version of the Standard Edition or Pro Edition, you can use that license file with this kit. If not follow these steps:

1. Log on at the My Intel Account Sign In web page and click ***Sign In.***
2. On the My Intel Home web page, click the Self-Service Licensing Center link.
3. Locate the serial number printed on the side of the development kit box below the bottom bar code. The number consists of alphanumeric characters and does not contain hyphens.
4. On the Self-Service Licensing Center web page, click the Find it with your License Activation Code link.
5. In the ***Find/Activate Products*** dialog box, enter your development kit serial number and click ***Search***.

6. When your product appears, turn on the check box next to the product name.
7. Click ***Activate Selected Products*** and click Close.
8. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the License Setup page of the ***Options*** dialog box in the Quartus Prime software to enable the software.

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Intel Quartus Prime Design Suite software. After one year, your DKE license will no longer be valid and you will not be permitted to use this version of the Intel Quartus Prime software. To continue using the Intel Quartus Prime software, you should download the free Quartus Prime Lite Edition or purchase a paid license for the Quartus Prime Pro Edition.

2.2. Development Board Package

Download the Intel Stratix 10 FPGA Development Kit package from the Intel Stratix 10 FPGA Development Kit page of the Intel website.

Unzip the Intel Stratix 10 FPGA Development Kit package.

Figure 2. Installed Development Kit Directory Structure

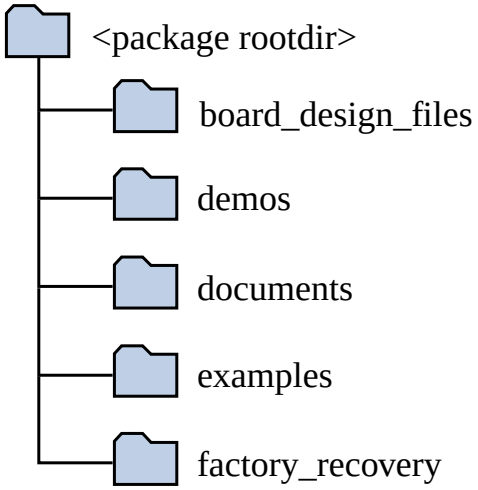


Table 2.

Directory Name	Description of Directory Contents
board_design_files	Contains schematic, layout, assembly and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications when available.
documents	Contains documentation.
examples	Contains sample design files for this board.
factory_recovery	Contains the orignal data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

2.3. Installing the USB-Blaster Driver

The development board includes integrated Intel FPGA Download Cable circuits for FPGA programming. However, for the host computer and board to communicate, you must install the On-Board Intel FPGA Download Cable II driver on the host computer.

Installation instrcutions for the On-Board Intel FPGA Download Cable II driver for your operating system are available on the Intel website.

On the Altera Programming Cable Driver Information web page of the Intel website, locate the table entry for your configuration and click the link to access the instructions.

3. Development Board Setup

This chapter describes how to apply power to the development board and provides default switch and jumper settings.

3.1. Applying Power to the Development Board

This development kit is designed to operate in two modes:

1. **As a PCIe* add-in card**

   When operating the card as a PCIe system, insert the card into an available PCIe slot and connect a 2x4 and 2x3 pin PCIe power cable from the system to power connectors at J26 and J27 of the board respectively.

   Note: When operating as a PCIe add-in card, the board will not power on unless power is supplied to J26 and J27.

2. **In bench-top mode**

   In Bench-top mode, you must supply the board with provided power 240W power supply connected to the power connector J27. The following describes the operation in bench-top mode.

This development board ships with its switches preconfigured to support the design examples in the kit.

If you suspect that your board may not be correctly configured with the default settings, follow the instructions in the Default Switch and Jumper Settings section of this chapter.

1. The development board ships with design examples stored in the flash memory device. To load the design stored in the factory portion of the flash memory, verify SW3.3 is set to ON. This is the default setting.
2. Connect the supplied power supply to an outlet and the DC Power Jack (J27) on the FPGA board.

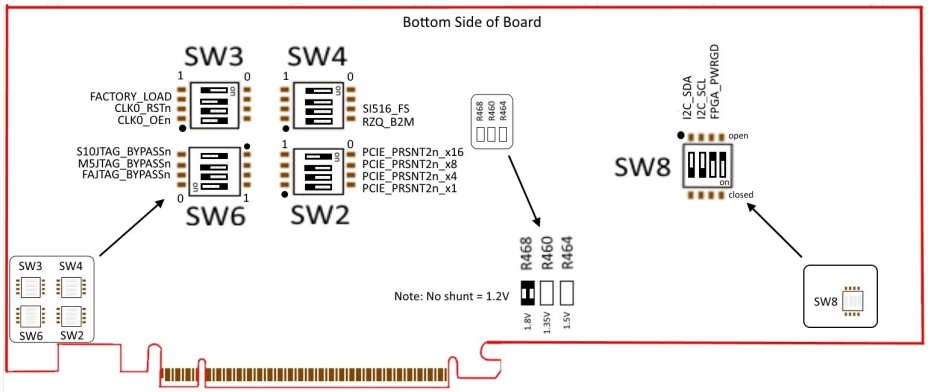
   Note: Use only the supplied power supply. Power regulation circuits on the board can be damaged by power supplies with greater voltage.
3. Set the power switch (SW7) to the ON position.

When the board powers up, the parallel flash loader (PFL) on the MAX® V reads a design from flash memory and configures the FPGA. When the configuration is complete, green LEDs illuminate signaling the device configured successfully. If the configuration fails, the red LED illuminates.

3.2. Default Switch and Jumper Settings

This topic shows you how to restore the default factory settings and explains their functions.

Figure 3. Default Switch Settings



1. Set DIP switch bank (SW2) to match the following table

Table 3. SW2 DIP PCIe Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	x1	ON for PCIe x1	OFF
2	x4	ON for PCIe x4	OFF
3	x8	ON for PCIe x8	OFF
4	x16	ON for PCIe x16	ON

2. If all of the resistors are open, the FMC VCCIO value is 1.2 V. To change that value, add resistors as shown in the folowing table.

Table 4. Default Resistor Settings for the FPGA Mezzanine (FMC) Ports (Board Bottom)

Board Reference	Board Label	Description
R460	1.35V	1.35V FMC VCCIO select
R464	1.5V	1.5V FMC VCCIO select
R468	1.8V	1.8V FMC VCCIO select *Note:* A 0 Ohm resistor is installed by default

3. Set DIP switch bank (SW6) to match the following table.

Table 5. SW6 JTAG Bypass DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	Intel Stratix 10	OFF to enable the Intel Stratix 10 in the JTAG chain. ON to bypass the Intel Stratix 10 in the JTAG chain.	OFF
2	MAX V	OFF to enable the MAX V in the JTAG chain. ON to bypass the MAX V in the JTAG chain.	OFF
3	FMC	OFF to enable the FMC Connector in the JTAG chain. ON to bypass the FMC connector in the JTAG chain.	ON

4. SW1 DIP Switch Default Settings (Board TOP)

Table 6. SW1 DIP Switch Default Settings (Board TOP)

Switch	Board Label	Function
1	MSEL2	MSEL2, MSEL1 = [0,0] QSPI AS Fast Mode MSEL2, MSEL1 = [0,1] QSPI AS Normal Mode MSEL2, MSEL1 = [1,0] AVST x16 Mode (Default) MSEL2, MSEL1 = [1,1] JTAG Only Mode
2	MSEL1	

5. Set DIP switch bank (SW6) to match the following table.

Table 7. SW3 DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	CLK0_OEn	ON to enable the Si5341A clock device OFF to disable the Si5341A clock device	ON
2	CLK0_RSTn	ON to hold the Si5341A clock device in reset OFF to allow the Si5341A clock device to function normally	OFF
3	FACTORY_LOAD	ON to load factory image from flash OFF to load user hardware1 from flash	ON

Table 8. SW4 DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	RZQ_B2M	ON for setting RZQ resistor of Bank 2M to 99.17 Ohm	OFF

continued...

Switch	Board Label	Function	Default Position
		OFF for setting RZQ resistor of Bank 2M to 240 Ohm	
2	SI516_FS	ON for setting the SDI REFCLK frequency to 148.35 MHz OFF for setting the SDI REFCLK frequency to 148.5 MHz	OFF

Table 9. SW8 DIP Switch Default Settings (Board Bottom)

Switch	Board Label	Function	Default Position
1	I2C_SDA	Connects VRM I2C to MAX V I2C chain	ON
2	I2C_SCL	Connects VRM I2C to MAX V I2C chain	ON
3	FPGA_PWRGD	Connects LT2987 Power Good to MAX V	OFF

3.3. Factory Reset

This section is a part of the Board Test System (BTS) GUI that is under development. It will be updated in a future version when new information is available.

4. Board Components

This chapter introduces all the important components on the development board. A complete set of schematics, a physical layout database and GERBER files for the development board reside in the development kit documents directory.

4.1. Board Overview

An image of the Intel Stratix 10 FPGA development board is shown below.

Figure 4. Stratix 10 FPGA Development Board Image - Front

Figure 5. Stratix 10 FPGA Development Board Image - Rear

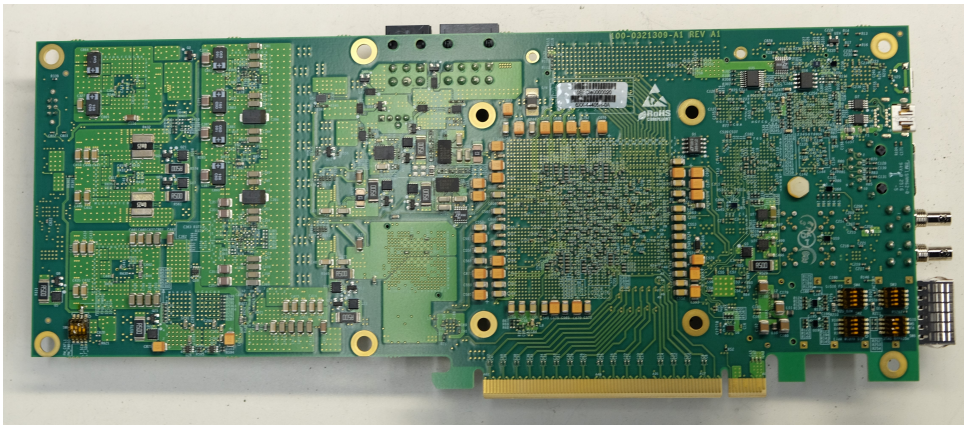


Table 10. Stratix 10 GX FPGA Development Board Components

Board Reference	Type	Description
Featured Devices		
U1	FPGA	Stratix 10 GX FPGA, 1SG280LU3F50E3VGS1. • Adaptive logic modules (ALMs): 933,120 • LEs (K): 2,753 • Registers: 3,732,480 • M20K memory blocks: 11,721 • Transceiver Count: 96 • Package Type: 2397 BGA
U11	CPLD	MAX V CPLD, 2210 LEs, 256 FBGA, 1.8V VCCINT.
Configuration and Setup Elements		
CN1	On-board Intel FPGA Download Cable II	Micro-USB 2.0 connector for programming and debugging the FPGA.
SW2	PCI Express* Control DIP Switch	Enables PCI Express link widths x1, x4, x8 and x16.
SW6	JTAG Bypass DIP Switch	Enables and disbales devices in the JTAG chain. This switch is located on the back of the board.
SW1	MSEL Configuration DIP Switch	Sets the Intel Stratix 10 MSEL pins.
SW3	Board settings DIP Switch	Controls the MAX V CPLD System Controller functions such as clock reset, clock enable, factory or user design load from flash and FACTORY signal command sent at power up. This switch is located at the bottom of the board.
S4	CPU reset push button	The default reset for the FPGA logic. This button resides on the LED daughter board.
S2	Image select push button	Toggles the configuration LEDs which selects the program image that loads from flash memory to the FPGA. This button resides on the LED daughter board.
S1	Program configuration push button	Configures the FPGA from flash memory image based on the program LEDs. This button resides on the LED daughter board.
S3	MAX V reset push button	The default reset for the MAX V CPLD System Controller. This button resides on the LED daughter board.
Status Elements		
D14, D16	JTAG LEDs	Indicates the transmit or receive activity of the System Console USB interface. The TX and RX LEDs would flicker if the link is in use and active. The LEDs are either off when not in use or on when in use but idle. These LEDs reside on the LED daughter board.
D18, D21	System Console LEDs	Indicates the transmit or receive activity of the System Console USB interface. The TX and RX LEDs would flicker if the link is in use and active. The LEDs are either off when not in use or on when in use but idle.
D1, D2, D5	Program LEDs	Illuminates to show the LED sequence that determines which flash memory image loads to the FPGA when you press the program load push button. The LEDs reside on the LED daughter card.
D8	Configuration Done LED	Illuminates when the FPGA is configured. This LED resides on the LED daughter board.
D6	Load LED	Illuminates during FPGA configuration. This LED resides on the LED daughter board.

continued...

Board Reference	Type	Description
D3	Error LED	Illuminates when the FPGA configuration fails. This LED resides on the LED daughter board.
D45	Power LED	Illuminates when the board is powered on.
D40	Temperature LED	Illuminates when an over temperature condition occurs for the FPGA device. Ensure that an adequate heatsink/fan is properly installed.
D2, D3, D4, D5, D6	Ethernet LEDs	Shows the connection speed as well as transmit or receive activity.
D9	SDI Cable LED	Illuminates to show the transmit or receive activity for the SDI interface.
D15, D17, D19, D20, D22, D23	PCI Express link LEDs	You can configure these LEDs to display the PCI Express link width (x1, x4, x8 and x16) and data rate (Gen2, Gen3). These LEDs reside on the LED daughter board.
D4, D7, D9, D10	User defined LEDs	Four bi-color LEDs (green and red) for 8 user LEDs. Illuminates when driven low. These LEDs reside on the LED daughter board.
D11, D12, D13	FMC LEDs	Illuminates for RX, TX, PRNSTn activity of the FMC daughter card (when present). These LEDs reside on the LED daughter board.
Clock Circuits		
X1	SDI Reference Clock	SW4.2 DIP switch controlled: FS=0: 148.35 MHz FS=1: 148.5 MHz
U7	Programmable Clock Generator	Si 5341A Programmable Clock Generator by the clock control GUI Default Frequencies are • Out0=155.25 MHz • Out1=644.53125 MHz • Out2= 135 MHz • Out3= Not Used • Out4=156.25 MHz • Out5= 625 MHz • Out6=Not used • Out7=125 MHz • Out8= 125 MHz • Out9=125 MHz
U9	Programmable Clock Generator	Si5338A Programmable Clock Generator by the clock control GUI. Default frequencies are: • CLK0= 100 MHz • CLK1= 100 MHz • CLK1= 133 MHz • CLK2= 50 MHz
J3, J4	Clock input MMPX connector	MMPX clock input for the SDI interface.
J1, J2	MMPX GPIO/CLK output from FPGA Bank 3I	MMPX GPIO/CLK output from FPGA Bank 3I.
J17, J18	Serial Digital Interface (SDI) transceiver connectors	Two HDBNC connectors. Drives serial data input/output to or from SDI video port.
Transceiver Interfaces		

continued...

Board Reference	Type	Description
J9	PCIe x16 gold fingers	PCIe TX/RX x16 interface from FPGA bank 1C, 1D and 1E.
J12	Mini Display Port Video Connector	Four TX channels of Display Port Video interface from FPGA Bank 1F.
J15	QSFP connector	Four TX/RX channels from FPGA Bank 1K
J17, J18	SDI HDBNC Video Connector	Single TX/RX channel from FPGA bank 1N.
J13	Intel FMC Interface	Sixteen TX/RX channels from FPGA banks 4C, 4D and 4E.
General User Input/Output		
SW1	FPGA User DIP Switch	Four user DIP switches. When switch is ON, a logic 0 is selected. This switch resides on the LED daughter board.
S5, S6, S7	General user push buttons	Three user push buttons. Driven low when pressed. These buttons reside on the LED daughter board.
D4, D7, D9, D10	User defined LEDs	Four bi-color user LEDs. Illuminates when driven low. These LEDs reside on the LED daughter board.
Memory Devices		
J11	HiLo Connector	One x72 memory interface supporting DDR3 (x72), DDR4 (x72), QDR4 (x36) and RLDRAM3 (x36). This development kit includes three plugin modules (daughtercards) that use the HiLo connector: • DDR4 memory (x72) 1333 MHz • DDR3 memory (x72) 1066 MHz • RLDRAM3 memory (x36) 1200 MHz
U12, U83	Flash Memory	ICS-1GBIT STRATA FLASH, 16-BIT DATA.
Communication Ports		
J9	PCI Express x16 edge connector	Gold-plated edge fingers for up to x16 signaling in either Gen1, Gen2 or Gen3 mode.
J13	FMC Port	FPGA mezzanine card ports
J10	Gbps Ethernet RJ-45 connector	RJ-45 connector which provides a 10/100/1000 Ethernet connection via a Marvell 88E1111 PHY and the FPGA-based Intel Triple Speed Ethernet MAC MegaCore function in SGMII mode.
J15	QSFP Interface	Provides four transceiver channels for a 40G/100G QSFP module.
CN1	Micro-USB connector	Embedded Intel Intel FPGA Download Cable II JTAG for programming the FPGA via a USB cable.
Display Ports		
J12	Mini DisplayPort Connector	Mini DisplayPort male receptacle.
J17, J18	SDI video port	Two HDBNC connectors that provide a full-duplex SDI interface.
Power Supply		
J9	PCI Express edge connector	Interfaces to a PCI Express root port such as an appropriate PC motherboard.
J27	DC input jack	Accepts a 12 V DC power supply when powering the board from the provided power brick for lab benchoperation. When operating from the PCIe slot, this input must also be

continued...

Board Reference	Type	Description
		connected to the 6-pin Aux PCIe power connector provided by the PC system along with J27, or else the board will not power on.
SW7	Power switch	Switch to power ON or OFF the board when supplied from the DC input jack.
J26	PCIe 2x4 ATX power connector	12 V ATX input. This input must be connected to the 8-pin Aux PCIe power connector provided by the PC system when the board is plugged into a PCIe slot, or else the board will not power on.

4.2. MAX V CPLD System Controller

The development board utilizes the EPM2210 System Controller, an Intel MAX V CPLD for the following purposes:

- FPGA configuration from flash memory
- Power consumption monitoring
- Temperature monitoring
- Fan control
- Control registers for clocks
- Control registers for remote update system

Table 11. MAX V CPLD System Controller Device Pin-Out

Schematic Signal Name	Pin Number	I/O Standard	Description
FMCA_PRSTn	G1	1.8V	FMC present
FPGA_AVST_CLK	J2	1.8V	Avalon stream clock
USB_MAX5_CLK	H5	1.8V	48 MHz USB clock
CLK_CONFIG	J5	1.8V	125 MHz configuration clock
FPGA_nSTATUS	J4	1.8V	Configuration nSTATUS signal
FPGA_CONF_DONE	K1	1.8V	Configuration DONE signal
USB_CFG2	K2	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG3	K5	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG4	L1	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG5	L2	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG6	K3	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG12	M1	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG7	M2	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG8	L4	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG9	L3	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG10	N1	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG0	M4	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG11	N2	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus

continued...

Schematic Signal Name	Pin Number	I/O Standard	Description
USB_CFG1	M3	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG13	N3	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
USB_CFG14	P2	1.8V	MAX V to Intel MAX 10 Intel FPGA Download Cable bus
FPGA_INIT_DONE	G4	1.8V	Initialization done signal
FPGA_AVST_VALID	F5	1.8V	Avalon stream valid signal
FPGA_AVST_READY	H1	1.8V	Avalon stream ready signal
FMCA_C2M_PWRGD	R16	1.8V	FMC card to mezzanine power good signal
M5_JTAG_TCK	P3	1.8V	Dedicated MAX V JTAG clock
M5_JTAG_TDI	L6	1.8V	Dedicated MAX V JTAG data in
M5_JTAG_TDO	M5	1.8V	Dedicated MAX V JTAG data out
M5_JTAG_TMS	N4	1.8V	Dedicated MAX V JTAG mode select
MAX_RESETn	C5	2.5V	MAX V reset signal
Si516_FS	A4	2.5V	Si516 device frequency select signal
OVERTEMP	E1	2.5V	FAN PWM control signal
CLK0_FINC	E9	2.5V	Si5341A device frequency increment signal
CLK0_FDEC	A10	2.5V	Si5341A device frequency decrement signal
MAX_CONF_DONE	D7	2.5V	Configuration done LED signal
CLK0_OEn	B12	2.5V	Si5341A device enable signal
CLK1_RSTn	C11	2.5V	Si5341A device reset signal
PGM_SEL	A7	2.5V	Program Select push button signal
PGM_CONFIG	A6	2.5V	Program Configuration push button signal
PGM_LED0	D6	2.5V	Program LED0 signal
PGM_LED1	C6	2.5V	Program LED1 signal
PGM_LED2	B7	2.5V	Program LED2 signal
FACTORY_LOAD	B5	2.5V	Load factory image DIP switch signal
MAX_ERROR	C7	2.5V	Configuration error LED
MAX_LOAD	B6	2.5V	Configuration loading LED

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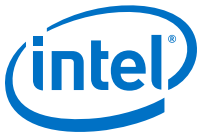
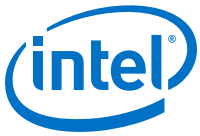


Schematic Signal Name	Pin Number	I/O Standard	Description
FPGA_PR_REQUEST	T4	1.8V	Partial reconfiguration request signal
FLASH_ADDR1	F15	1.8V	Flash address bus
FLASH_ADDR2	G16	1.8V	Flash address bus
FLASH_ADDR3	G15	1.8V	Flash address bus
FLASH_ADDR4	H16	1.8V	Flash address bus
FLASH_ADDR5	H15	1.8V	Flash address bus
FLASH_ADDR6	F16	1.8V	Flash address bus
FLASH_ADDR7	G14	1.8V	Flash address bus
FLASH_ADDR8	D16	1.8V	Flash address bus
FLASH_ADDR9	E15	1.8V	Flash address bus
FLASH_ADDR10	E16	1.8V	Flash address bus
FLASH_ADDR11	H14	1.8V	Flash address bus
FLASH_ADDR12	D15	1.8V	Flash address bus
FLASH_ADDR13	F14	1.8V	Flash address bus
FLASH_ADDR14	C14	1.8V	Flash address bus
FLASH_ADDR15	C15	1.8V	Flash address bus
FLASH_ADDR16	H3	1.8V	Flash address bus
FLASH_ADDR17	H2	1.8V	Flash address bus
FLASH_ADDR18	E13	1.8V	Flash address bus
FLASH_ADDR19	F13	1.8V	Flash address bus
FLASH_ADDR20	G13	1.8V	Flash address bus
FLASH_ADDR21	G12	1.8V	Flash address bus
FLASH_ADDR22	E12	1.8V	Flash address bus
FLASH_ADDR23	H13	1.8V	Flash address bus
FLASH_ADDR24	G5	1.8V	Flash address bus
FLASH_ADDR25	J13	1.8V	Flash address bus
FPGA_PR_DONE	J16	1.8V	Partial reconfiguration done signal
CLK_MAXV_50M	J12	1.8V	50 MHz MAX V clock
MAXV_OSC_CLK1	H12	1.8V	125 MHz MAX V clock
FLASH_DATA0	J15	1.8V	Flash data bus
FLASH_DATA1	L16	1.8V	Flash data bus
FLASH_DATA2	L14	1.8V	Flash data bus
FLASH_DATA3	K14	1.8V	Flash data bus

continued...

Schematic Signal Name	Pin Number	I/O Standard	Description
FLASH_DATA4	L13	1.8V	Flash data bus
FLASH_DATA5	L15	1.8V	Flash data bus
FLASH_DATA6	M15	1.8V	Flash data bus
FLASH_DATA7	M16	1.8V	Flash data bus
FLASH_DATA8	K16	1.8V	Flash data bus
FLASH_DATA9	K15	1.8V	Flash data bus
FLASH_DATA10	J14	1.8V	Flash data bus
FLASH_DATA11	K13	1.8V	Flash data bus
FLASH_DATA12	L12	1.8V	Flash data bus
FLASH_DATA13	N16	1.8V	Flash data bus
FLASH_DATA14	M13	1.8V	Flash data bus
FLASH_DATA15	L11	1.8V	Flash data bus
FLASH_CEn0	D14	1.8V	Flash chip enable 0
FLASH_OEn	P14	1.8V	Flash putput enable
FLASH_RDYBSYn0	F12	1.8V	Flash ready/busy 0
FLASH_RESETn	D13	1.8V	Flash reset
FLASH_CLK	N15	1.8V	Flash clock
FLASH_ADVn	N14	1.8V	Flash address valid
FLASH_CEn1	F11	1.8V	Flash chip enable 1
FPGA_PR_ERROR	K12	1.8V	Partial reconfiguration error signal
FPGA_CvP_CONFDONE	M14	1.8V	CvP configuration done signal
FLASH_RDYBSYn1	P12	1.8V	Flash ready/busy 1
FPGA_CONFIG_D0	R1	1.8V	FPGA configuration data bus
FPGA_CONFIG_D1	T2	1.8V	FPGA configuration data bus
FPGA_CONFIG_D2	N6	1.8V	FPGA configuration data bus
FPGA_CONFIG_D3	N5	1.8V	FPGA configuration data bus
FPGA_CONFIG_D4	N7	1.8V	FPGA configuration data bus
FPGA_CONFIG_D5	N8	1.8V	FPGA configuration data bus
FPGA_CONFIG_D6	M12	1.8V	FPGA configuration data bus
FPGA_CONFIG_D7	T13	1.8V	FPGA configuration data bus
FPGA_CONFIG_D8	T15	1.8V	FPGA configuration data bus
FPGA_CONFIG_D9	R13	1.8V	FPGA configuration data bus
FPGA_CONFIG_D10	P4	1.8V	FPGA configuration data bus

continued...



Schematic Signal Name	Pin Number	I/O Standard	Description
FPGA_CONFIG_D11	R3	1.8V	FPGA configuration data bus
FPGA_CONFIG_D12	T10	1.8V	FPGA configuration data bus
FPGA_CONFIG_D13	P5	1.8V	FPGA configuration data bus
FPGA_CONFIG_D14	R4	1.8V	FPGA configuration data bus
FPGA_CONFIG_D15	R5	1.8V	FPGA configuration data bus
MAX5_OEn	N10	1.8V	MAX V output enable
MAX5_CSn	T11	1.8V	MAX V chip select
MAX5_WEn	R11	1.8V	MAX V write enable
MAX5_CLK	N11	1.8V	MAX V clock
MAX5_BEn0	R10	1.8V	MAX V byte enable
MAX5_BEn1	M10	1.8V	MAX V byte enable
MAX5_BEn2	T12	1.8V	MAX V byte enable
MAX5_BEn3	P10	1.8V	MAX V byte enable
CPU_RESETn	K4	1.8V	CPU reset button
I2C_1.8V_SCL	P13	1.8V	1.8V I^2C bus
I2C_1.8V_SDA	R14	1.8V	1.8V I^2C bus
OVERTEMPn_1.8V	N13	1.8V	Over temperature signal
TSENSE_ALERTn_1.8V	T7	1.8V	Temperature sense alert signal
QSPI_SS0_MSEL0	R12	1.8V	QSPI slave select 0/ MSEL0 configuration select
MSEL1	P11	1.8V	MSEL1 configuration select
MSEL2	M11	1.8V	MSEL2 configuration select
SDI_MF2_MUTE	R7	1.8V	SDI device MF2
SDI_MF0_BYPASS	P8	1.8V	SDI device MF0
SDI_MF1_AUTO_SLEEP	R6	1.8V	SDI device MF1
SDI_TX_SD_HDn	P6	1.8V	SDI device SD/HD
FPGA_nCONFIG	E14	1.8V	nCONFIG configuration signal

4.3. FPGA Configuration

You can use the Quartus Programmer to configure the FPGA with your SRAM Object File (**.sof**).

Ensure the following:

- The Quartus Programmer and the Intel FPGA Download Cable II driver are installed on the host computer.
- The micro-USB cable is connected to the FPGA development board.
- Power to the board is ON, and no other applications that use the JTAG chain are running.

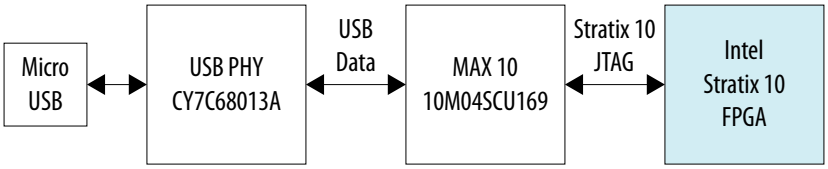
1. Start the Quartus Programmer.
2. Click **Auto Detect** to display the devices in the JTAG chain.
3. Click **Change File** and select the path to the desired **.sof**.
4. Turn on the **Program/Configure** option for the added file.
5. Click Start to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

Using the Quartus Programmer to configure a device on the board causes other JTAG-based applications such as the Board Test System and the Power Monitor to lose their connection to the board. Restart those applications after configuration is complete.

Programming the FPGA over Embedded USB-Blaster

The figure below shows the high-level conceptual block diagram for programming the Intel Stratix 10 FPGA over the embedded USB-Blaster.

Figure 6. USB-Blaster Conceptual Block Diagram



Programming the FPGA over External USB-Blaster

The figure below shows the high-level conceptual block diagram for programming the Intel Stratix 10 FPGA over an external USB-Blaster.

Figure 7. JTAG Chain Conceptual Block Diagram