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Arria II GX FPGA Development Kit

User Guide

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UG-01066-1.1

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Contents

1. About This Kit

The Altera® Arria® II GX FPGA Development Kit is a complete design environment that includes both the hardware and software you need to develop Arria II GX FPGA designs. The PCI-SIG-compliant board and the one-year license for the Quartus® II software provide everything you need to begin developing custom Arria II GX FPGA designs. The following list describes what you can accomplish with the kit:

- Develop and test PCI Express® (PCIe) designs.
- Develop and test memory subsystems consisting of DDR2 and DDR3 memories.
- Take advantage of the modular and scalable design by using the high-speed mezzanine card (HSMC) connectors to interface to over 30 different HSMCs provided by Altera partners, supporting protocols such as Serial RapidIO®, 10 Gigabit Ethernet, SONET, Common Public Radio Interface (CPRI), Open Base Station Architecture Initiative (OBSAI) and others.

Kit Features

This section briefly describes the Arria II GX FPGA Development Kit contents.

Hardware

The Arria II GX FPGA Development Kit includes the following hardware:

- Arria II GX FPGA development board—A development platform that allows you to develop and prototype hardware designs running on the Arria II GX EP2AGX125 FPGA.

  For detailed information about the board components and interfaces, refer to the *Arria II GX FPGA Development Board Reference Manual*.

- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - USB cable
  - Ethernet cable
  - HSMC loopback board—A daughtercard that allows for loopback testing all signals on the HSMC interface using the Board Test System
  - HSMC debug breakout board—A daughtercard that routes 40 CMOS signals to a 0.1-inch header and adds 20 LEDs to the remaining 40 CMOS signals

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software is a licensed set of Altera tools with full functionality. Your kit includes a one-year license for the Quartus II software (Windows platform only). This license entitles you to all the features of the subscription edition for a period of one year. After the year, you must purchase a renewal subscription to continue using the software. For more information, refer to the Altera website (www.altera.com).

Download the Quartus II Subscription Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.

The Quartus II Subscription Edition Software includes the following items:

- Quartus II Software—The Quartus II software, including the SOPC Builder system development tool, provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system.
  - Verify functionality of your design, and quickly and easily evaluate its size and speed.
  - Generate time-limited device programming files for designs that include MegaCore functions.
  - Program a device and verify your design in hardware.

  The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

  For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.
- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allows you to develop embedded software for the Nios II processor which you can include in your Altera FPGA designs.

Arria II GX FPGA Development Kit Installer

The license-free Arria II GX FPGA Development Kit installer includes all the documentation and design examples for the kit.

Download the Arria II GX FPGA Development Kit installer from the Arria II GX FPGA Development Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.

The remaining chapters in this user guide lead you through the following Arria II GX FPGA development board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the FPGA development board
- Configuring the Arria II GX FPGA
- Running the Board Test System designs

For complete information about the FPGA development board, refer to the *Arria II GX FPGA Development Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in "Kit Features" on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Board

To inspect the board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.

In typical applications with the Arria II GX FPGA development board, a heat sink is not necessary. However, under extreme conditions or for engineering sample silicon the board might require additional cooling to stay within operating temperature guidelines. You can perform power consumption and thermal modeling to determine whether your application requires additional cooling. The board has two holes near the FPGA that accommodate many different heat sinks, including the Dynatron V31G.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

CAUTION To avoid damage to the board, always have the board POWER switch (SW1) in the OFF position before inserting the DC power jack (J4).

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the Arria II GX FPGA Development Kit page.
- For additional daughter cards available for purchase, refer to the Development Board Daughtercards page.
- For the Arria II GX device documentation, refer to the Literature: Arria II GX Devices page.
- To purchase devices from the eStore, refer to the Devices page.
- For Arria II GX OrCAD symbols, refer to the Capture CIS Symbols page.
- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

This chapter explains how to install the following software:

- Quartus II Subscription Edition Software
- Arria II GX FPGA Development Kit
- USB-Blaster™ driver

Installing the Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software provides the necessary tools used for developing hardware and software for Altera FPGAs. Included in the Quartus II Subscription Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. The Quartus II software (including SOPC Builder) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this kit. To install the Altera development tools, perform the following steps:

1. Run the Quartus II Subscription Edition Software installer you acquired in "Software" on page 1–1.
2. Follow the on-screen instructions to complete the installation process.

If you have difficulty installing the Quartus II software, refer to *Altera Software Installation and Licensing Manual*.

Licensing Considerations

Purchasing this kit entitles you to a one-year license for the Quartus II Subscription Edition Software. Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, you need to obtain and install a license file. To begin, go to the Self Service Licensing Center page of the Altera website, log into or create your myAltera account, and take the following actions:

1. On the Activate Products page, enter the serial number provided with your development kit in the **License Activation Code** box.

Your serial number is printed on the development kit box below the bottom bar code. The number is 10 or 11 alphanumeric characters and does not contain hyphens. Figure 3–1 shows 3S150SPXXXX as an example serial number.

Figure 3–1. Locating Your Serial Number

2. Consult the Activate Products table, to determine how to proceed.
   a. If the administrator listed for your product is someone other than you, skip the remaining steps and contact your administrator to become a licensed user.
   b. If the administrator listed for your product is you, proceed to step 3.
   c. If the administrator listed for your product is *Stocking*, activate the product, making you the administrator, and proceed to step 3.
3. Use the Create New License page to license your product for a specific user (you) on specific computers. The Manage Computers and Manage Users pages allow you to add users and computers not already present in the licensing system.

   To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

4. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus II software to enable the software.

For complete licensing details, refer to *Altera Software Installation and Licensing Manual*.

Installing the Arria II GX FPGA Development Kit

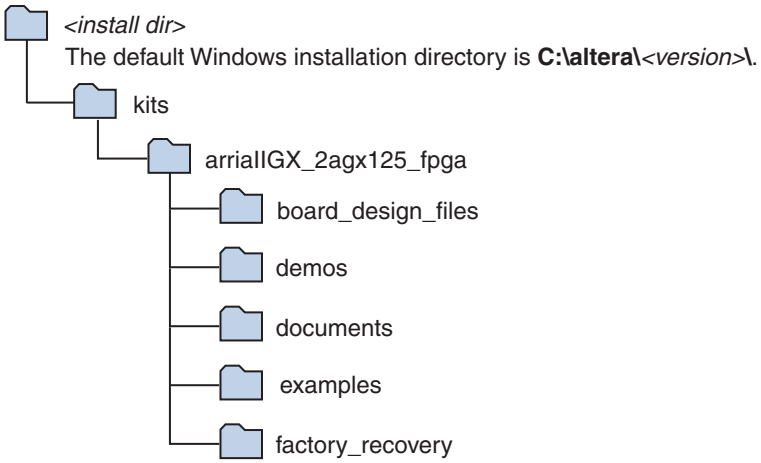
To install the Arria II GX FPGA Development Kit, perform the following steps:

1. Run the Arria II GX FPGA Development Kit installer you acquired in "Software" on page 1–1.

2. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you choose is in the same relative location to the Quartus II software installation.

The installation program creates the Arria II GX FPGA Development Kit directory structure shown in Figure 3–2.

Figure 3–2. Arria II GX FPGA Development Kit Installed Directory Structure *(1)*



Note to Figure 3–2:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Arria II GX FPGA Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster Driver

The Arria II GX FPGA development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster driver on the host computer.

Installation instructions for the USB-Blaster driver for your operating system are available on the Altera website. On the Cable & Adapter Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

4. Development Board Setup

The instructions in this chapter explain how to set up the Arria II GX FPGA development board.

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Arria II GX FPGA development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch Settings" on page 4–2 to return the board to its factory settings before proceeding.
2. The FPGA development board ships with design examples stored in the flash memory device. Verify the USER_LOAD switch (SW4.4) is set to the off position to load the design stored in the factory portion of flash memory. Figure 4–1 shows the switch location on the Arria II GX FPGA development board.
3. Set the POWER switch (SW1) to the off position.

   CAUTION: To avoid damage to the board, always have the board POWER switch (SW1) in the off position before inserting the DC power jack (J4).

4. Connect the DC adapter (+16 V, 3.75 A) to the DC power jack (J4) on the FPGA board and plug the cord into a power outlet.

   CAUTION: Use only the supplied 16-V power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

5. Set the POWER switch (SW1) to the on position. When power is supplied to the board, a blue LED (D18) illuminates indicating that the board has power.

The MAX II device on the board contains a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. The USER_LOAD switch (SW4.4) controls which design to load. When the switch is in the off position, the PFL loads the design from the factory portion of flash memory. When the switch is in the on position, the PFL loads the design from the user portion of flash memory.

The kit includes a MAX II design which contains the MAX II PFL megafunction. The design resides in the *<install dir>***\kits\arriaIIGX_2agx125_fpga\examples\max2** directory.

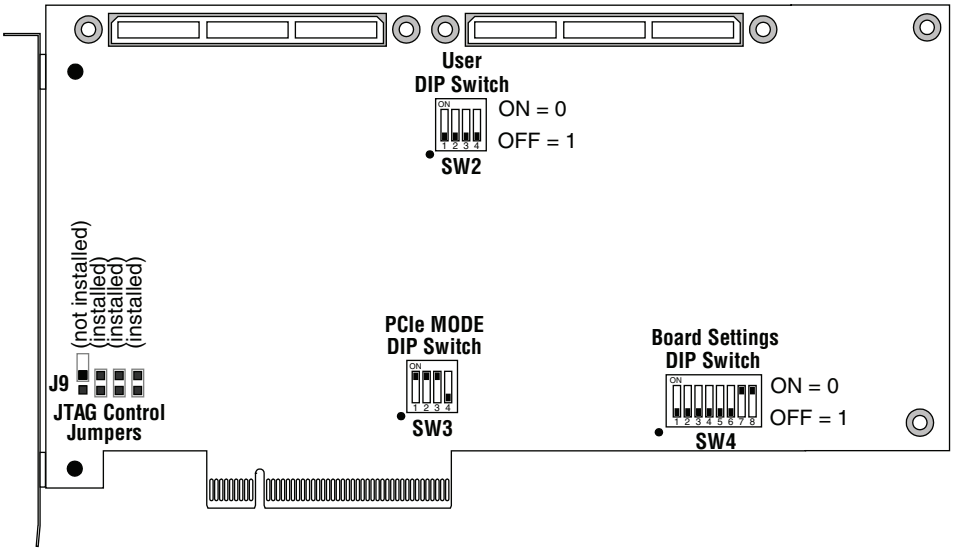
When configuration is complete, the CONF DONE LED (D14) illuminates, signaling that the Arria II GX device configured successfully.

For more information about the PFL megafunction, refer to *Parallel Flash Loader Megafunction User Guide*.

Factory Default Switch Settings

This section shows the factory switch settings for the Arria II GX FPGA development board. Figure 4–1 shows the switch locations and the default position of each switch.

Figure 4–1. Switch Locations and Default Settings on the FPGA Development Board



To restore the switches to their factory default settings, perform the following steps:

1. Set DIP switch bank (SW3) to match Table 4–1 and Figure 4–1.

Table 4–1. SW3 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	PCIe x1	Switch 1 has the following options: ■ When off, the PCIe card PCIE_PRSNT2n_x1 signal is connected to PCIe card PRSNT1 signal. ■ When on, the PCIe card PCIE_PRSNT2n_x1 signal floats.	On
2	PCIe x4	Switch 2 has the following options: ■ When off, the PCIe card PCIE_PRSNT2n_x4 signal is connected to PCIe card PRSNT1 signal. ■ When on, the PCIe card PCIE_PRSNT2n_x4 signal floats.	On
3	PCIe x8	Switch 3 has the following options: ■ When off, the PCIe card PCIE_PRSNT2n_x8 signal is connected to PCIe card PRSNT1 signal. ■ When on, the PCIe card PCIE_PRSNT2n_x8 signal floats.	On
4	—	■ —	—

2. Set DIP switch bank (SW4) to match Table 4–2 and Figure 4–1.

Table 4–2. SW4 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	DIP0	Switch 1 has the following options: ■ When on, reserved. ■ When off, reserved.	Off
2	DIP1	Switch 2 has the following options: ■ When on, reserved. ■ When off, reserved.	Off
3	DIP2	Switch 3 has the following options: ■ When on, reserved. ■ When off, reserved.	Off
4	USER LOAD	Switch 4 has the following options: ■ When on, the PFL loads the user hardware 1 design on power up. ■ When off, the PFL loads the factory design on power up.	Off
5	PWR MON	Switch 5 has the following options: ■ When on, reserved. ■ When off, reserved.	Off
6	USB DISn	Switch 6 has the following options: ■ When on, reserved. ■ When off, reserved.	Off
7	CLK EN	Switch 7 has the following options: ■ When on, all on-board oscillators are enabled. ■ When off, on-board oscillators to the FPGA are disabled.	On
8	CLK SEL	Switch 8 has the following options: ■ When on, programmable oscillator clock (U30) is selected. ■ When off, LVPECL SMA clock (J10 and J11) is selected.	On

3. Set the board jumpers to match Table 4–3 and Figure 4–1.

Table 4–3. JTAG Chain Jumper Settings (Part 1 of 2)

Board Reference	Board Label	Function	Default Shunt Position
J9 pins 1-2	MAX DIS	This jumper has the following options: ■ Installing the shunt removes the MAX II EPM2210 device from the JTAG chain. ■ Removing the shunt includes the MAX II EPM2210 device in the JTAG chain.	Not installed
J9 pins 3-4	HSMA DIS	This jumper has the following options: ■ Installing the shunt removes HSMC port A from the JTAG chain. ■ Removing the shunt includes HSMC port A in the JTAG chain.	Installed

Table 4–3. JTAG Chain Jumper Settings (Part 2 of 2)

Board Reference	Board Label	Function	Default Shunt Position
J9 pins 5-6	HSMB DIS	This jumper has the following options: ■ Installing the shunt removes HSMC port B from the JTAG chain. ■ Removing the shunt includes HSMC port B in the JTAG chain.	Installed
J9 pins 7-8	PCIe DIS	This jumper has the following options: ■ Installing the shunt removes the PCIe device from the JTAG chain. ■ Removing the shunt includes the PCIe device in the JTAG chain.	Installed

For more information about the FPGA board settings, refer to the *Arria II GX FPGA Development Board Reference Manual*.

5. Board Update Portal

The Arria II GX FPGA Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the USER_LOAD switch (SW4.4) in the off position, the Arria II GX FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware portion of flash memory, and provides links to useful information on the Altera website, including kit-specific links and design resources.

☞ After successfully updating the user hardware flash memory, you can load the user design from flash memory into the FPGA. To do so, set the USER_LOAD switch (SW4.4) to the on position and power cycle the board.

The source code for the Board Update Portal design resides in the <*install dir*>**\kits\arriaIIGX_2agx125_fpga\examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page A–4 to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.

☞ Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. With the board powered down, set the USER_LOAD switch (SW4.4) to the off position.
2. Attach the Ethernet cable from the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router, and obtains an IP address. The LCD on the board displays the IP address.
4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

5. Click Arria II GX FPGA Development Kit on the Board Update Portal web page to access the kit's home page. Visit this page occasionally for documentation updates and additional new designs.

You can also navigate directly to the Arria II GX FPGA Development Kit page of the Altera website to determine if you have the latest kit software.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Design files available from the Arria II GX FPGA Development Kit page include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Preparing Design Files for Flash Programming" on page A–2 for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" to access the Board Update Portal web page.
2. In the **Hardware File Name** field specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field, otherwise leave the **Software File Name** field blank.
3. Click **Upload**. The progress bar indicates the percent complete.
4. To configure the FPGA with the new design after the flash memory upload process is complete, set the USER_LOAD switch (SW4.4) to the on position and power cycle the board, or press the IMAGE SEL button (PB6) until the CONFIG1 LED (D12) illuminates and then press the LOAD IMAGE button (PB5). Refer to Table 6–1 on page 6–5 for information about the CONFIG LEDs.

As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "Restoring the Flash Device to the Factory Settings" on page A–4.

6. Board Test System

The kit includes a design example and application called the Board Test System to test the functionality of the Arria II GX FPGA development board. The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the application to test board components, modify functional parameters, observe performance, and measure power usage. The application is also useful as a reference for designing systems. To install the application, follow the steps in "Installing the Arria II GX FPGA Development Kit" on page 3–2.

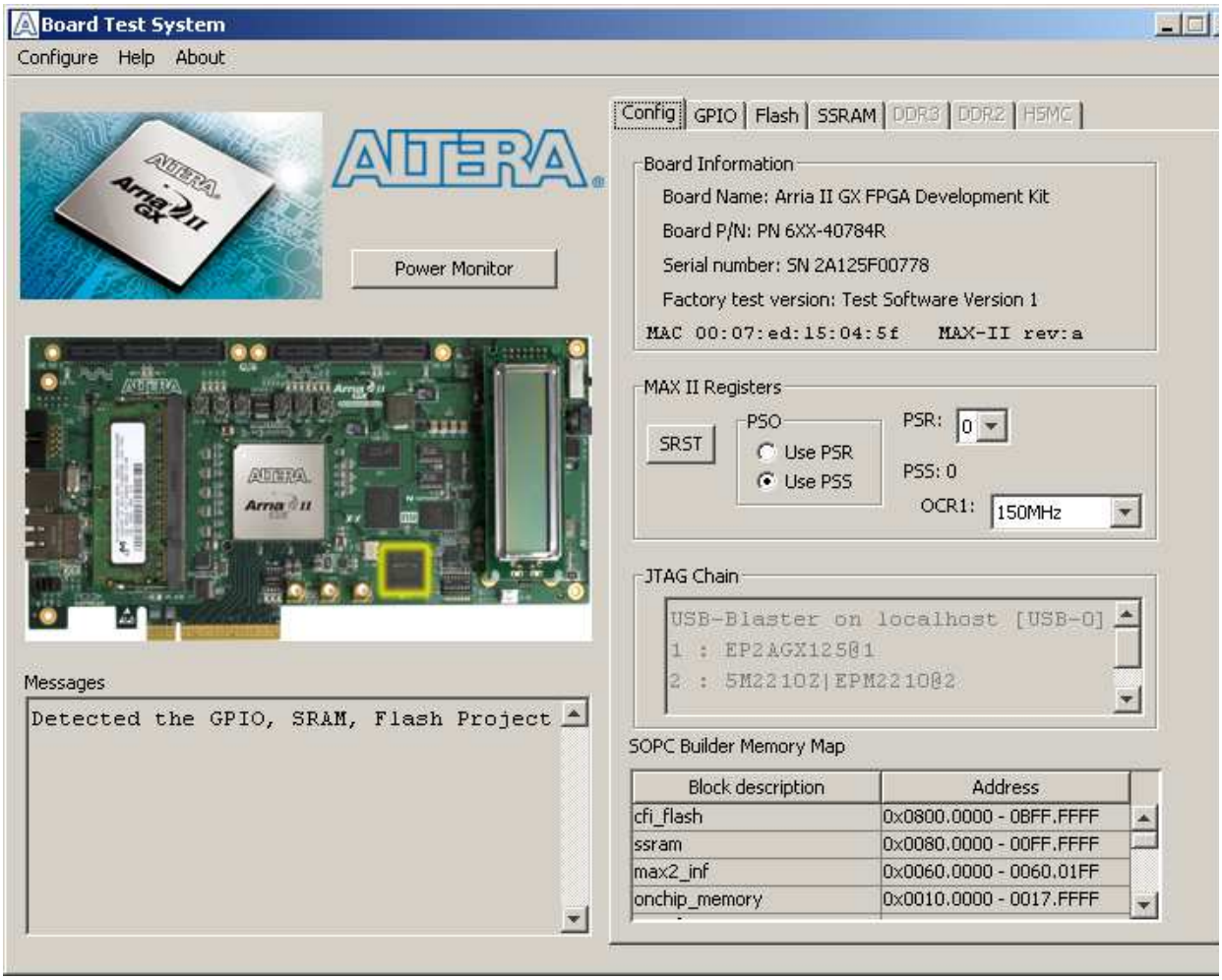
The application provides access to the following Arria II GX FPGA development board features:

- General purpose I/O (GPIO)
- SRAM
- Flash memory
- DDR2 and DDR3 memories
- HSMC connectors
- Character LCD
- Programmable oscillator

The application allows you to exercise most of the board components. While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.

The Board Test System GUI communicates over the JTAG bus to a test design running in the Arria II GX device. Figure 6–1 shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The **Power Monitor** button starts the Power Monitor application that measures and reports current power information for the board. Because the application communicates over the JTAG bus to the MAX II device, you can measure the power of any design in the FPGA, including your own designs.

The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board

With the power to the board off, perform the following steps:

1. Connect the USB cable to the board.
2. Verify the settings for the board settings DIP switch bank (SW4) match Table 4–2 on page 4–3.
3. Set the USER_LOAD switch (SW4.4) to the on position.
4. Verify the settings for the JTAG jumper block (J9) match Table 4–3 on page 4–3. These settings determine the devices to include in the JTAG chain.

   For more information about the board's DIP switch and jumper settings, refer to the *Arria II GX FPGA Development Board Reference Manual*.

5. Turn the power to the board on. The board loads the design stored in the user hardware 1 portion of flash memory into the FPGA. If your board is still in the factory configuration or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design loads the GPIO, SRAM, and flash memory tests.

   CAUTION: To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the <*install dir*>**\kits\arriaIIGX_2agx125_fpga\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

On Windows, click **Start** > **All Programs** > **Altera** > **Arria II GX FPGA Development Kit** <*version*> > **Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The Arria II GX FPGA development board's flash memory ships preconfigured with the design that corresponds to the **Config**, **GPIO**, and **SSRAM**, and **Flash** tabs.

If you power up your board with the USER_LOAD switch (SW4.4) in the off position, or if you load your own design into the FPGA with the Quartus II Programmer, you receive a message prompting you to configure your board with a valid Board Test System design. Refer to "The Configure Menu" for information about configuring your board.

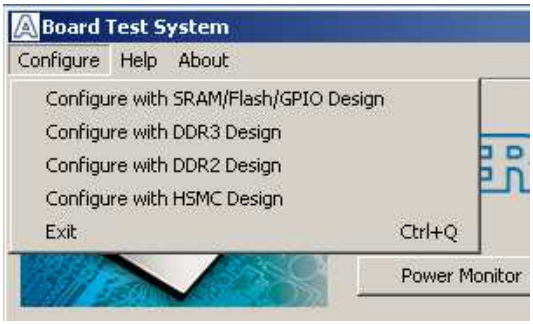
Using the Board Test System

This section describes each control in the Board Test System application.

The Configure Menu

Each test design tests different functionality and corresponds to one or more application tabs. Use the Configure menu to select the design you want to use. Figure 6–2 shows the Configure menu.

Figure 6–2. The Configure Menu



To configure the FPGA with a test system design, follow these steps:

1. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (**.sof**) to the FPGA. The download process usually takes about a minute.
3. When configuration finishes, click **Close** to complete the configuration process and run the design in the FPGA. A corresponding application tab appears in the GUI that interfaces with the design in the FPGA.

The Config Tab

The **Config** tab shows information about the board's current configuration. Figure 6–1 on page 6–2 shows the **Config** tab. The tab displays the contents of the MAX II registers, the MAX II code version, the JTAG chain, the board's MAC address, and the flash memory map.

The following sections describe the controls on the **Config** tab.

MAX II Registers

The **MAX II registers** control allow you to view and change the current MAX II register values as described in Table 6–1. Changes to the register values with the GUI take effect immediately. For example, selecting a new frequency in the **OCR1** list immediately changes the clock frequency on the board.

Table 6–1. MAX II Registers

Register Name	Read/Write Capability	Description
System Reset (SRST)	Write only	Set to 0 to initiate an FPGA reconfiguration.
Page Select Register (PSR)	Read / Write	Determines which of the up to eight (0-7) pages of flash memory to use for FPGA reconfiguration. The flash memory ships with pages 0 and 1 preconfigured.
Page Select Override (PSO)	Read / Write	When set to 0, the value in PSR determines the page of flash memory to use for FPGA reconfiguration. When set to 1, the value in PSS determines the page of flash memory to use for FPGA reconfiguration
Page Select Switch (PSS)	Read only	Holds the current value of the illuminated CONFIG LED (D11-D13) based on the following encoding: ■ 0 = CONFIG LED (D13) and corresponds to the flash memory page for the factory hardware design ■ 1 = CONFIG LED (D12) and corresponds to the flash memory page for the user hardware 1 design ■ 2 = CONFIG LED (D11) and corresponds to the flash memory page for the user hardware 2 design
Oscillator Control Register 1 (OCR1)	Read / Write	Determines the U26 oscillator output frequency based on the following options: ■ 0 = 100 MHz ■ 1 = 125 MHz ■ 2 = 150 MHz ■ 3 = 156.25 MHz
Oscillator Control Register 2 (OCR2)	Read / Write	Determines the U30 oscillator output frequency based on the following options: ■ 0 = 100 MHz ■ 1 = 125 MHz ■ 2 = 150 MHz ■ 3 = 156.25 MHz You cannot change OCR2 from the GUI.

- **PSO**—Sets the MAX II PSO register. The following options are available:
  - **Use PSR**—Allows the PSR to determine the page of flash memory to use for FPGA reconfiguration.
  - **Use PSS**—Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.