Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Cyclone III FPGA Development Kit

User Guide

101 Innovation Drive
San Jose, CA 95134
www.altera.com

UG-01027-1.4
P25-36208-03

Subscribe

Contents

Chapter 1. About This Kit
Introduction . . . 1–1
Kit Features . . . 1–1
Documentation . . . 1–2

Chapter 2. Getting Started
Introduction . . . 2–1
Before You Begin . . . 2–1
Check the Kit Contents . . . 2–1
Inspect the Board . . . 2–2
Hardware Requirements . . . 2–2
Software Requirements . . . 2–2
References . . . 2–3

Chapter 3. Software Installation
Introduction . . . 3–1
Installing the Cyclone III Development Kit . . . 3–1
Installing the Quartus II Web Edition Software . . . 3–2
Licensing Considerations . . . 3–3
Installing the USB-Blaster Driver . . . 3–3

Chapter 4. Development Board Setup
Introduction . . . 4–1
Requirements . . . 4–1
Powering Up the Board . . . 4–2
Configuring the FPGA . . . 4–4

Chapter 5. Board Update Portal
Introduction . . . 5–1
Connecting to the Board Update Portal Web Page . . . 5–1
Using the Board Update Portal to Update User Designs . . . 5–2

Chapter 6. Board Test System
Introduction . . . 6–1
Preparing the Board . . . 6–2
Running the Board Test System . . . 6–3
Using the Board Test System . . . 6–4
The Configure Menu . . . 6–4
The Config Tab . . . 6–4
MAX II Registers . . . 6–4
JTAG Chain . . . 6–4
Board Information . . . 6–5
Flash Memory Map . . . 6–5
The GPIO Tab . . . 6–5
Character LCD . . . 6–6
User DIP Switches . . . 6–6
User LEDs . . . 6–6
Push Button Switches . . . 6–6

7-Segment Display 6–6
Ethernet 6–6
The SRAM&Flash Tab 6–7
SRAM 6–7
Flash 6–8
The Graphic LCD Tab 6–9
Graphics LCD 6–9
The DDR2 Tab 6–10
Start 6–10
Stop 6–10
Performance Indicators 6–11
Error Control 6–11
Number of Addresses to Write and Read 6–11
Data Type 6–11
Read and Write Control 6–11

Chapter 7. Power Measurement
Introduction 7–1
Power Design Example 7–1
Measuring Power 7–3
A/D Measurements 7–3
Measuring V_{CC_INT} Power 7–3
Measuring I/O Power 7–3
Measuring Voltage with a DMM 7–4
Calculating Power 7–5
Changing the Design Example 7–5

Chapter 8. Design Tutorials
Introduction 8–1
My First FPGA Tutorial 8–1
My First Nios II Software Tutorial 8–1

Appendix A. Programming the Flash Device
Overview A–1
Creating a Flash File A–1
Parallel Flash Loader Instantiation A–4
Programming the Flash Device A–4
Restoring the Factory Design to the Flash Device A–6

Additional Information
Document Revision History Info–1
How to Contact Altera Info–1
Typographic Conventions Info–2

1. About This Kit

Introduction

Welcome to the Altera® Cyclone® III Development Kit, which includes a full-featured FPGA development board, hardware and software development tools, documentation, and accessories needed to begin FPGA development.

The kit provides an integrated control environment that includes a USB command controller, a multi-port SRAM/DDR SDRAM/flash memory controller, Ethernet, an on-board meter, and example designs with demonstration circuitry specified in Verilog code to help you get started quickly with your own designs.

The development board includes an Altera Cyclone III FPGA configured with a hardware reference design stored in flash memory. Hardware designers can use the development board, along with example designs included in the kit, as a platform to prototype complex embedded systems.

The development kit includes these kit features and documentation:

- Cyclone III development board
- Accessory daughter cards
- Power supply, cables, and documentation

Kit Features

This section briefly describes the Cyclone III Development Kit features.

- **Cyclone III Development Board**—a prototyping platform that allows you to develop and prototype high-speed bus interfaces as well as evaluate Cyclone III transceiver performance.

  For specific information about board components and interfaces, refer to the *Cyclone III 3C120 Development Board Reference Manual*.

- **Quartus II Web Edition Software**—The Quartus II software integrates into nearly any design environment, with interfaces to industry-standard EDA tools. The kit includes:
  - The SOPC Builder system development tool
  - Quartus II Web Edition software

- **MegaCore IP Library**—This library contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore® Plus feature to perform the following tasks:
  - Simulate behavior of a MegaCore function within your system
  - Verify functionality of your design, and quickly and easily evaluate its size and speed
  - Generate time-limited device programming files for designs that include MegaCore functions
  - Program a device and verify your design in hardware
- **Nios II Embedded Software Design Tools**—This full-featured set of tools allows you to develop embedded software on the Nios II processor running on Altera FPGAs.
- **Cyclone III Development Kit Application and Drivers**—The application and drivers allow you to execute memory read and write transactions to the board.
- **Design Examples**—The design examples are useful for a variety of hardware applications and let you quickly begin board prototyping and device verification.

You only need to purchase a license for a MegaCore function when you are completely satisfied with its functionality and performance, and want to take your design to production.

The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.

Documentation

The Cyclone III Development Kit contains the following documents:

- *Readme.txt*—Contains special instructions and refers to the kit documentation.
- *Cyclone III Development Kit User Guide* (this document)—Describes how to use the kit.
- *Cyclone III 3C120 Development Board Reference Manual*—Provides specific information about the board components and interfaces, steps for using the board, and pin-outs and signal specifications.

2. Getting Started

Introduction

This user guide familiarizes you with the contents of the kit and guides you through the Cyclone III development board setup. Using this guide, you can do the following:

- Inspect the contents of the kit
- Install the Altera Quartus II Web Edition software
- Install the Cyclone III Development Kit
- Set up, power up, and verify correct operation of the development board
- Configure the Cyclone III FPGA
- Find and use the tutorials
- Set up and run included application examples and demonstrations

For complete information about the development board, refer to the *Cyclone III 3C120 Development Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in this section. If any of the items are missing, contact Altera before you proceed.

Check the Kit Contents

The Cyclone III Development Kit contains the following items:

- Cyclone III development board with an EP3C120F780C7N Cyclone III device
- USB cable
- Accessory daughter cards:
  - Two loopback high-speed mezzanine connector (HSMC) cards
  - Debug HSMC card
  - One 16 character × 2 line Liquid Crystal Display (LCD)
  - One 2.8-in. thin-film transistor (TFT) LCD module
- 16-V DC Power supply and adapters for North America, Europe, the United Kingdom, and Japan.

To ensure that you have the most up-to-date information about this product, refer to the Cyclone III FPGA Development Kit page.

Inspect the Board

Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

CAUTION

Without proper anti-static handling, the Cyclone III development board can be damaged.

Verify that all components are on the board and appear intact.

In typical applications with the Cyclone III development board, a heatsink is not necessary. However, under extreme conditions the board may require additional cooling to stay within operating temperature guidelines. You may wish to perform power consumption and thermal modeling to determine whether your application requires additional cooling.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

Hardware Requirements

The Quartus II software has some minimum system requirements. Otherwise, the Cyclone III development kit provides all of the hardware needed to use the board.

For the Quartus II software requirements, refer to the Quartus II Web Edition Software page.

Software Requirements

This kit requires the following software:

- Windows XP operating system
- Quartus II Web Edition software

Refer to *Quartus II Installation & Licensing for Windows* for further information on the Quartus II system software requirements, especially heeding the following:

- A web browser, Microsoft Internet Explorer version 5.0 or later or Firefox version 2.0 or later. You need a web browser to register the Quartus II software and request license files. Refer to "Licensing Considerations" on page 3–3.
- Version 2.0 or later of the .NET framework.

If you receive an "Application Error" message when launching the demo application, install version 2.0 or later versions of the .NET framework. Some Windows versions do not have runtime DLL for the .NET application. You can download the .NET framework application from the following location: *www.microsoft.com/download*.

References

For other related information, refer to the following websites:

Table 2–1.

For More Information About	Refer to
Additional daughter cards available for purchase	www.altera.com/products/devkits/kit-daughter_boards.jsp
Cyclone III handbook	www.altera.com/literature/lit-cyc3.jsp
Cyclone III reference designs	http://www.altera.com/products/devkits/altera/kit-cyc3.html
eStore if you want to purchase devices	www.altera.com/buy/devices/buy-devices.html
Cyclone III Orcad symbols	www.altera.com/support/software/download/pcb/pcbpcb_index.html
Nios® II 32-bit embedded processor solutions	www.altera.com/technology/embedded/emb-index.html

3. Software Installation

Introduction

This section describes the following procedures:

- "Installing the Cyclone III Development Kit"
- "Installing the Quartus II Web Edition Software" on page 3–2
- "Installing the USB-Blaster Driver" on page 3–3

Before starting the installation, verify that you have complied with the conditions described in "Software Requirements" on page 2–2.

Installing the Cyclone III Development Kit

The license-free Cyclone III Development Kit installer includes all the documentation and design examples for the kit.

To install the Cyclone III Development Kit, follow these steps:

1. Download the Cyclone III Development Kit installer from the Cyclone III FPGA Development Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Development Kits, Daughter Cards & Programming Hardware page of the Altera website.
2. Follow the on-screen instructions to complete the installation process.

When the installation is complete, the Cyclone III Development Kit installation program creates the directory structure shown in Figure 3–1, where <*path*> is the Cyclone III Development Kit installation directory.

Figure 3–1. Cyclone III Development Kit Installed Directory Structure

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications that may change from release to release.
documents	Contains the development kit documentation.
examples	Contains the sample design files for the Cyclone III Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to put the board into the original condition.

Installing the Quartus II Web Edition Software

The Quartus II Web Edition software provides the necessary tools for developing hardware and software for Altera FPGAs. Included in the Quartus II Web Edition software are the Quartus II software, the Nios II EDS, and the MegaCore® IP Library. The Quartus II software (including SOPC Builder) and the Nios II EDS are the primary FPGA development tools for creating the reference designs in this kit.

To install the Quartus II Web Edition software, follow these steps:

1. Download the Quartus II Web Edition software from the Quartus II Web Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.
2. Follow the on-screen instructions to complete the installation process.

If you have difficulty installing the Quartus II software, refer to *Quartus II Installation & Licensing for Windows and Linux Workstations*.

The Quartus II Web Edition software includes the following items:

- Quartus II software—The Quartus II software, including the SOPC Builder system development tool, provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.

  To compare the Quartus II subscription and web editions, refer to *Altera Quartus II Software—Subscription Edition vs. Web Edition*. The kit also works with the subscription edition.

- MegaCore IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions with the OpenCore Plus feature to perform the following tasks:
  - Simulate behavior of a MegaCore function in your system
  - Verify functionality of your design, and quickly and easily evaluate its size and speed
  - Generate time-limited device programming files for designs that include MegaCore functions
  - Program a device and verify your design in hardware
  - The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

  For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.

- Nios® II Embedded Design Suite (EDS)—A full-featured tool set that allow you to develop embedded software for the Nios II processor which you can include in your Altera FPGA designs.

Licensing Considerations

The Quartus II Web Edition software is license-free and supports Cyclone III devices without any additional licensing requirement. This kit also works with the Quartus II Subscription Edition software, after you obtain the proper license file. To purchase a subscription, contact your Altera sales representative.

Installing the USB-Blaster Driver

The Cyclone III development board includes integrated USB-Blaster™ circuitry for FPGA programming. However, for the host computer and development board to communicate, you must install the USB-Blaster driver on the host computer.

To download the USB-Blaster driver, go to the Altera support site at www.altera.com/support/software/drivers/dri-index.html.
To install it, go to www.altera.com/support/software/drivers/usb-blaster/dri-usb-blaster-xp.html.

4. Development Board Setup

Introduction

The instructions in this chapter explain how to install the development board and configure the FPGA.

Requirements

Before starting the installation, verify that you have complied with the conditions described in "Hardware Requirements" on page 2–2 and have completed the following requirements:

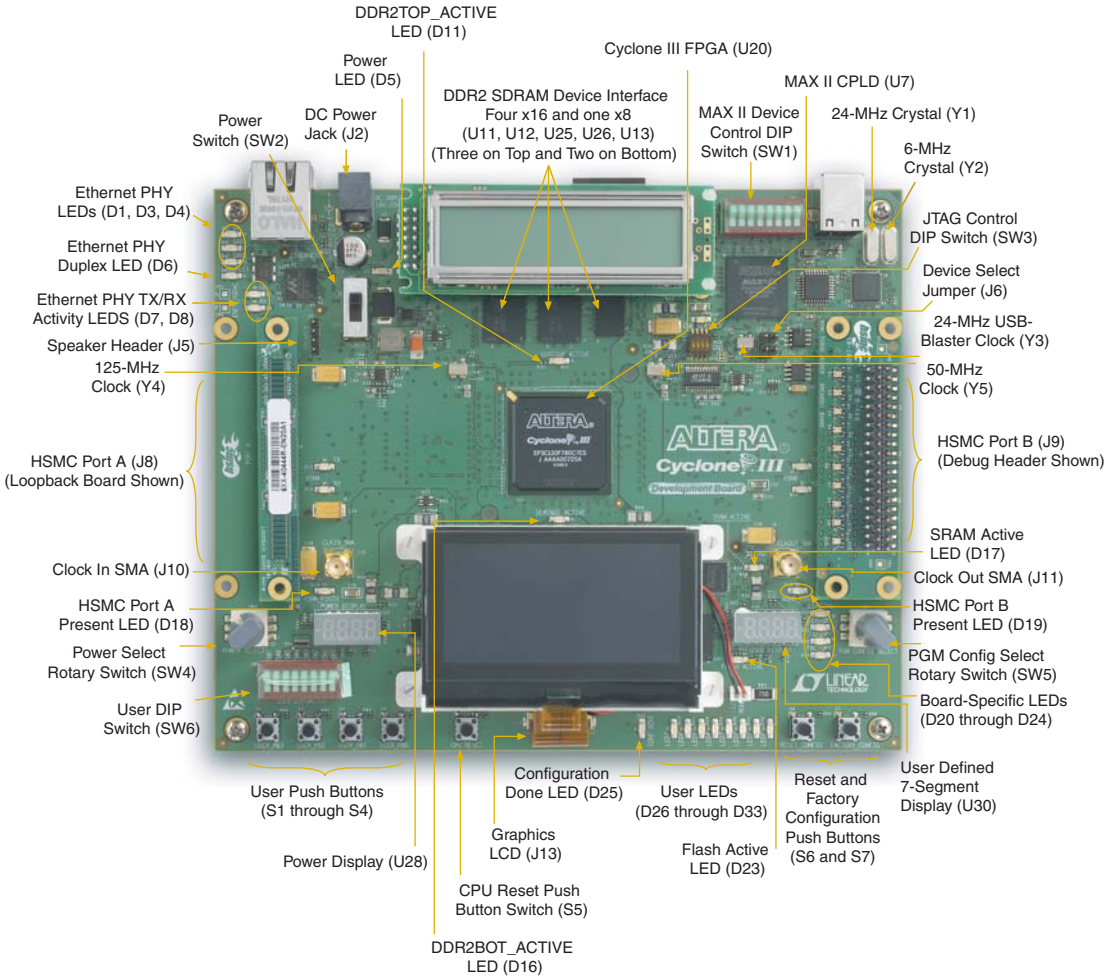
- Quartus II software installed on the host computer
- USB-Blaster driver software installed on the host computer.

The Cyclone III development board includes integrated USB-Blaster circuitry for FPGA programming. Host computer and development board cannot communicate without the USB-Blaster driver software installed. For installation information, refer to "Installing the USB-Blaster Driver" on page 3–3.

Powering Up the Board

Figure 4–1 shows the Cyclone III development board and its components.

Figure 4–1. Cyclone III Development Board Layout and Components



Before powering up, prepare the board by performing the following steps:

1. If cards are plugged into the high-speed mezzanine connector (HSMC) ports, remove them (Figure 4–1) shows a daughter card plugged into both port A and port B).
2. Ensure that the POWER switch SW2 is in the OFF (or DOWN) position.
3. Configure the 8-position SW1 DIP switch to the default settings in Table 4–1.

Table 4–1. Switch SW1 Settings (Part 1 of 2)

Switch	Name	Function		Default Position
		Position 0	Position 1	
1	mΩ/mA	mΩ	mA	0
2	V/Ω	V	W	1

Table 4–1. Switch SW1 Settings (Part 2 of 2)

Switch	Name	Function		Default Position
		Position 0	Position 1	
3	RSV0	MAX_RESERVE0		X
4	RSV1	MAX_RESERVE1		X
5	MAX0	PFL Disable	PFL Enable	1
6	MAX1	MAX_DIP1		X
7	MAX2	MAX_DIP2		X
8	MAX3	MAX_DIP3		X

Note to Table 4–1:

(1) X = don't care

4. Ensure that the 4-position SW3 mini-DIP switches and the two jumpers are set to the default positions shown in Table 4–2.

Table 4–2. Initial Switch and Jumper Settings

DEV_SEL-J6	JTAG_SEL-J7	SW3.1	SW3.2	SW3.3	SW3.4
ON	ON	ON	OFF	OFF	OFF

5. Verify that the PGM CONFIG SELECT rotary switch SW5 is set to 0.

At power up, the development board uses a preloaded configuration to demonstrate that the board is operating correctly.

Power up the development board by performing the following steps:

1. Connect the 16-V DC adapter to the development board and to a power source.

Use only the supplied 16-V power supply. Power regulation circuitry on the board could be damaged by supplies greater than 16 V.

2. Slide the POWER switch to ON. The nearby blue POWER light-emitting diode (LED) lights up.
3. Confirm that user LEDs 0-7 flash in a scrolling, side-to-side pattern. For customized configurations, the pattern depends on the application.

For information about custom configurations, refer to "Programming the Flash Device" on page A–4.

Configuring the FPGA

Before configuring the FPGA, ensure that the Quartus II software and the USB-Blaster driver software are installed on the host computer and the development board is powered on.

For USB-Blaster driver installation information, refer to "Installing the USB-Blaster Driver" on page 3–3.

To configure the Cyclone III FPGA, perform the following steps:

1. Verify that the 4-position SW3 mini-DIP switches and the two jumpers are set to the default positions shown in Table 4–2.
2. Connect the USB cable to the development board USB port.
3. Cycle the POWER switch OFF then ON.
4. Start the Quartus II software.
5. On the Tools menu, click **Programmer**. The Quartus II Programmer appears.
6. Click **Add File** and select *<path>***...****examples****cycloneIII_3c120_dev_my_first_fpga****cycloneIII_3c120_dev_my_first_fpga.sof**.
7. Turn on **Program/Configure** to select the added file.
8. Click **Start** to download the selected file to the FPGA. The FPGA is configured when the progress bar reaches 100%.
9. Confirm that user LEDs 0-3 flash in a slow binary counting pattern.

5. Board Update Portal

Introduction

The Cyclone III FPGA Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the PGM CONFIG SELECT rotary switch (SW5) in position 0, the Cyclone III FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the FPGA design 1 and design 6 (HW1 and SW1) portion of flash memory, and provides links to useful information on the Altera website, including links to kit-specific and design resources.

After successfully updating the FPGA design 1 and design 6 (HW1 and SW1)flash memory, you can load the user design from flash memory into the FPGA. To do so, set the PGM CONFIG SELECT rotary switch (SW5) to position 1 and power cycle the board.

The source code for the Board Update Portal design resides in the <*install dir*>**\kits\cycloneIII_3c120_dev\examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Factory Design to the Flash Device" on page A–6 to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.

Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform the following steps:

1. With the board powered down, set the PGM CONFIG SELECT rotary switch (SW5) to position 0.
2. Attach the Ethernet cable from the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router, and obtains an IP address. The LCD on the board displays the IP address.
4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

5. Click **Cyclone III FPGA Development Kit** on the Board Update Portal web page to access the kit's home page. Visit this page occasionally for documentation updates and additional new designs.

You can also navigate directly to the Cyclone III FPGA Development Kit page of the Altera website to determine if you have the latest kit software.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the FPGA design 1 and design 6 (HW1 and SW1)portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Design files available from the Cyclone III FPGA Development Kit page of the Altera website include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Creating a Flash File" on page A–1 for information about preparing your own design for upload.

To upload a design over the network into the FPGA design 1 and design 6 (HW1 and SW1) of flash memory on your board, perform the following steps:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" to access the Board Update Portal web page.
2. In the **Hardware File Name** field specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field, otherwise leave the **Software File Name** field blank.
3. Click **Upload**. The file takes about 20 seconds to upload.
4. To configure the FPGA with the new design after the flash memory upload process completes, set the PGM CONFIG SELECT rotary switch (SW5) to the 1 position and power cycle the board, or press the RESET_CONFIG push-button (S6).

As long as you do not overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the FPGA design 1 and design 6 (HW1 and SW1)portion of flash memory. If you overwrite the factory image, you can restore it by following the instructions in "Restoring the Factory Design to the Flash Device" on page A–6.

6. Board Test System

Introduction

The kit includes a design example and application called the Board Test System to test the functionality of the Cyclone III FPGA development board. The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the application to test board components, modify functional parameters, observe performance, and measure power usage. The application is also useful as a reference for designing systems. To install the application, follow the steps in "Installing the Cyclone III Development Kit" on page 3–1.

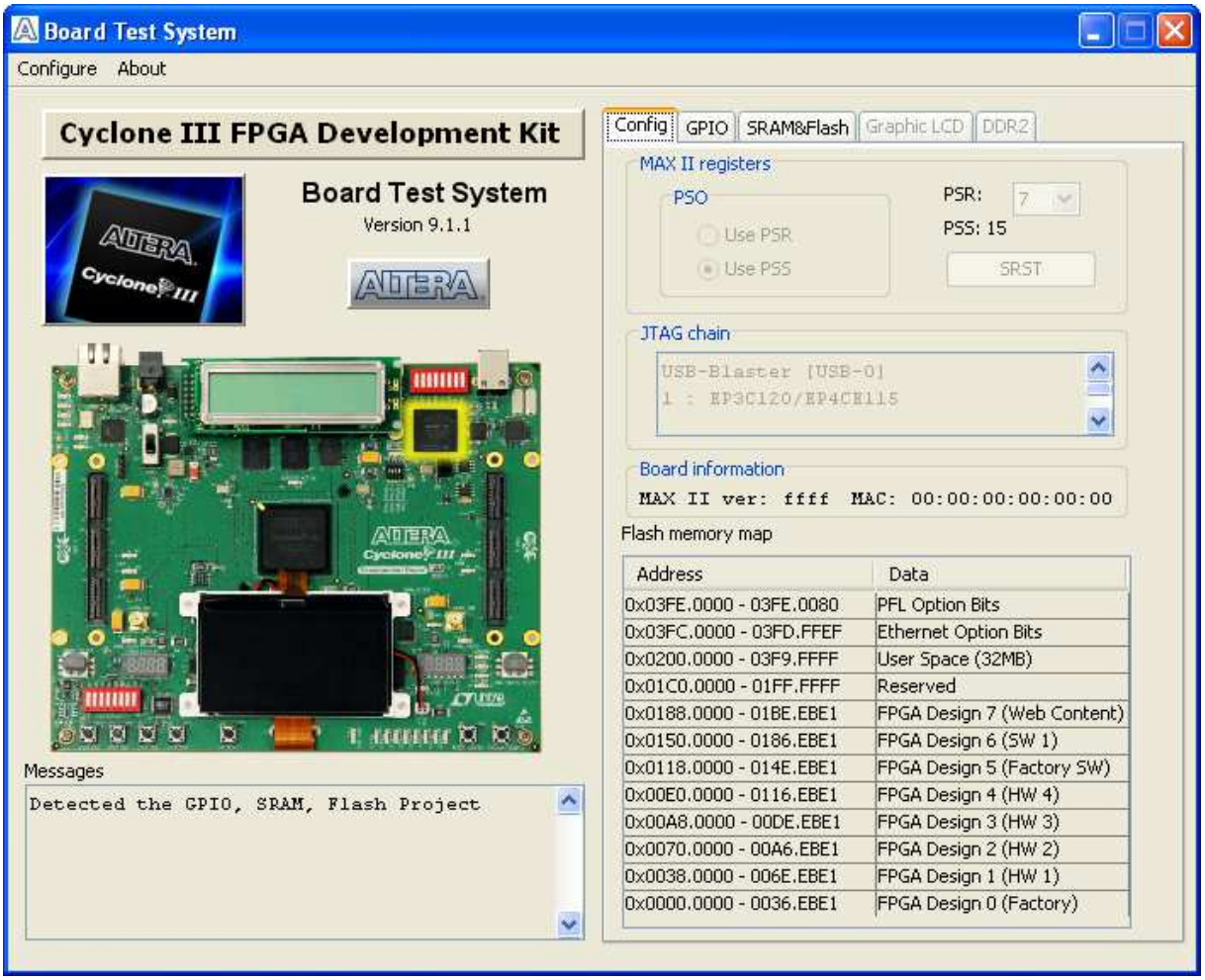
The application provides access to the following Cyclone III FPGA development board features:

- General purpose I/O (GPIO)
- SRAM
- Flash memory
- DDR2 memory
- Graphic LCD

The application allows you to exercise most of the board components. While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.

A GUI runs on the PC which communicates over the JTAG bus to a test design running in the Cyclone III device. Figure 6–1 shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

Preparing the Board

With the power to the board off, perform the following steps:

1. Connect the USB cable to the board.
2. Verify the settings for the board settings DIP switch bank (SW3) match the settings in Table 4–2 on page 4–3.

3. Set the PGM CONFIG SELECT rotary switch (SW5) to position 1.
4. Turn the power to the board on. The board loads the design stored in the user hardware 1 portion of flash memory into the FPGA. If your board is still in the factory configuration or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design that loads tests accessing the GPIO, SRAM, and flash memory.

CAUTION

To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the <*install dir*>**\kits\cycloneIII_3c120_dev\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

On Windows, click **Start** > **All Programs** > **Altera** > **Cyclone III FPGA Development Kit** <*version*> > **Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The Cyclone III FPGA development board's flash memory ships preconfigured with the design that corresponds to the **Config**, **GPIO**, **SRAM&Flash** tabs.

If you power up your board with the PGM CONFIG SELECT rotary switch (SW5) in a position other than position 1, or if you load your own design into the FPGA with the Quartus II Programmer, you receive a message prompting you to configure your board with a valid Board Test System design. Refer to "The Configure Menu" for information about configuring your board.

Using the Board Test System

This section describes each control in the Board Test System application.

The Configure Menu

Each test design tests different functionality and corresponds to one or more application tabs. Use the Configure menu to select the design you want to use. Figure 6–2 shows the Configure menu.

Figure 6–2. The Configure Menu

1. To configure the FPGA with a test system design, perform the following steps:On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click **Configure** to download the corresponding SRAM/Flash/GPIO design object file (**.sof**) to the FPGA. The download process usually takes about a minute.
3. When configuration finishes, the design begins running in the FPGA. The corresponding GUI application tab that interfaces with the design is enabled.

The Config Tab

The **Config** tab shows information about the board's current configuration. Figure 6–1 on page 6–2 shows the **Config** tab. The tab displays the contents of the JTAG chain, the flash memory map, and other details stored on the board.

The following sections describe the controls on the **Config** tab.

MAX II Registers

The **MAX II registers** control allow you to view the current MAX II register values. The values are set when you load the test system design into the FPGA and is not configurable.

JTAG Chain

The **JTAG chain** control shows all the devices currently in the JTAG chain. The Cyclone III device is always the first device in the chain.

Connecting a jumper shunt on J6 and an external USB-Blaster on J14 includes the MAX II device in the JTAG chain.

Board Information

The **Board information** controls display static information about your board.

Flash Memory Map

The **Flash memory map** control shows the memory map of the flash memory device on your board.

The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. You can write to the LCD, read user DIP switch settings, turn LEDs on or off, detect push button presses, write to the 7-segment display, and run an Ethernet application (the Simple Socket Server Test) on your board. Figure 6–3 shows the **GPIO** tab.

Figure 6–3. The GPIO Tab