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Cyclone III LS FPGA Development Kit

User Guide

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1. About This Kit

Introduction

The Altera® Cyclone® III LS FPGA Development Kit is a complete design environment that includes both the hardware and software you need to develop Cyclone III LS FPGA designs. The board and the one-year license for the Quartus® II software provide everything you need to begin developing custom Cyclone III LS FPGA designs. The following list describes what you can accomplish with the development kit:

- Develop and test memory subsystems consisting of DDR2 memory
- Take advantage of the modular and scalable design by using the high-speed mezzanine card (HSMC) connectors to interface to over 20 different HSMCs provided by Altera partners

Kit Features

This section briefly describes the Cyclone III LS FPGA Development Kit contents.

Hardware

- Cyclone III LS FPGA development board—A development platform that allows you to develop and prototype hardware designs running on the Cyclone III LS EP3CLS200 FPGA.
- For detailed information about the board components and interfaces, refer to the *Cyclone III LS FPGA Development Board Reference Manual*.
- Power supply and cables—The development kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - USB cable
  - Ethernet cable

Software

- Altera Complete Design Suite DVD—A DVD that includes the following items:
  - Quartus II Software—The Quartus II software, including the SOPC Builder system development tool, provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.

The kit includes a development kit edition (DKE) license for the Quartus II software (Windows platform only). This license entitles you to all the features of the subscription edition for a period of one year. After the year, you must purchase a renewal subscription to continue using the software. For more information, refer to the Altera website (www.altera.com).

- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system
  - Verify functionality of your design, and quickly and easily evaluate its size and speed
  - Generate time-limited device programming files for designs that include MegaCore functions
  - Program a device and verify your design in hardware

The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.

- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allow you to develop embedded software for the Nios II processor which you can include in your Altera FPGA designs.

- Cyclone III LS FPGA Development Kit CD-ROM—A CD-ROM that includes all the documentation and design examples for the kit.

Use the following links to check the Altera website to ensure you have the latest software versions:

- For the Altera Complete Design Suite, refer to the Quartus II Subscription Edition Download page.
- For the Cyclone III LS FPGA Development Kit, refer to the Cyclone III LS FPGA Development Kit page.

2. Getting Started

Introduction

This user guide leads you through the following Cyclone III LS FPGA development board setup steps:

- Inspecting the contents of the kit
- Installing the Altera Complete Design Suite DVD software
- Setting up, powering up, and verifying correct operation of the development board
- Configuring the Cyclone III LS FPGA
- Running the Board Test System designs

For complete information about the development board, refer to the *Cyclone III LS FPGA Development Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in this section. If any of the items are missing, contact Altera before you proceed.

Inspect the Board

To inspect the board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.

In typical applications with the Cyclone III LS FPGA development board, a heat sink is not necessary. However, under extreme conditions or for engineering sample silicon the board might require additional cooling to stay within operating temperature guidelines. You can perform power consumption and thermal modeling to determine whether your application requires additional cooling.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

References

Use the following links to check the Altera website for the following other related information:

- For the latest board design files and reference designs, refer to the Cyclone III LS FPGA Development Kit page.
- For additional daughter cards available for purchase, refer to the Development Board Daughtercards page.
- For the Cyclone III LS device documentation, refer to the Literature: Cyclone III Devices page.
- To purchase devices from the eStore, refer to the Devices page.
- For Cyclone III LS OrCAD symbols, refer to the Capture CIS Symbols page.
- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

Introduction

This section explains how to install the following software:

- Altera Complete Design Suite
- Cyclone III LS FPGA Development Kit
- USB-Blaster™ driver

Installing the Altera Complete Design Suite

The Altera Complete Design Suite provides the necessary tools used for developing hardware and software for Altera FPGAs. Included on the Altera Complete Design Suite DVD are the Quartus II software and the Nios II EDS. The Quartus II software (including SOPC Builder) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this development kit. To install the Altera software tools, perform the following steps:

1. Insert the Altera Complete Design Suite DVD into your computer.
2. Follow the installer instructions to complete the installation process.

If you have difficulty installing the Quartus II software, refer to the *Quartus II Installation & Licensing for Windows and Linux Workstations*.

Licensing Considerations

Before using the Quartus II software, you must request a license file from the Altera Licensing page on the Altera website and install it on your computer. When you request a license file, Altera emails you a **license.dat** file that enables the software.

To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you'll use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

To obtain a license, perform the following steps.

1. Go to the Get My Altera License page on the Altera website.
2. Under **Development Kit Licenses Request**, click **Licenses for RoHS-Compliant Kits**.
3. Follow the on-screen instructions to request your license. Altera sends you a license file through email.
4. To install your license, refer to *Specifying the License File* in *Quartus II Installation & Licensing for Windows and Linux Workstations*.

Installing the Cyclone III LS FPGA Development Kit

To install the Cyclone III LS FPGA Development Kit, perform the following steps:

1. Insert the Cyclone III LS FPGA Development Kit CD-ROM into your computer.

   The CD-ROM should start an auto-install process. If it does not, browse to the CD-ROM drive and double-click on the **setup.exe** file.

2. Follow the on-screen instructions to complete the installation process.

The installation program creates the directory structure for the Cyclone III LS FPGA Development Kit files shown in Figure 3–1.

Figure 3–1. Cyclone III LS FPGA Development Kit Installed Directory Structure

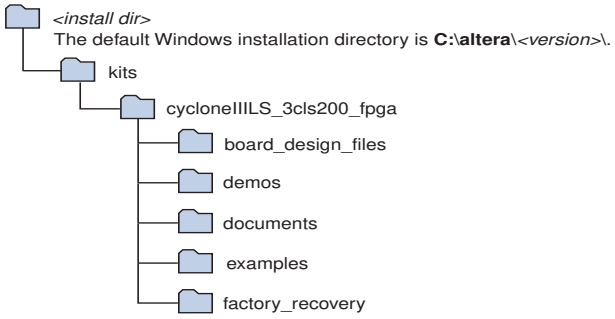


Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications.
documents	Contains the development kit documentation.
examples	Contains the sample design files for the Cyclone III LS FPGA Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster Driver

The Cyclone III LS FPGA development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster driver on the host computer.

Installation instructions for the USB-Blaster driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

4. Development Board Setup

Introduction

The instructions in this chapter explain how to set up the Cyclone III LS FPGA development board.

Setting Up the Board

To set up and power up the board, perform the following steps:

1. The Cyclone III LS FPGA development board ships with its board switches preconfigured to support the example designs in the development kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch Settings" on page 4–2 to return the board to its factory settings before proceeding.
2. The development board ships with example designs stored in the flash memory device. Verify the PGM/USER LOAD switch (SW2.6) is set to the on position to load the design stored in the factory portion of flash memory. Figure 4–1 shows the switch location on the Cyclone III LS FPGA development board.
3. Connect the DC adapter (+16 V, 3.75 A) to the DC power jack (J5) on the FPGA board and plug the cord into a power outlet.

   CAUTION: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

4. Set the POWER switch (SW1) to the on position. When power is supplied to the board, a blue LED (D3) illuminates indicating that the board has power.

The MAX II device on the board contains a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads one of two designs from flash memory and configures the FPGA. The PGM/USER LOAD switch (SW2.6) controls which design to load. When the switch is in the on position, the PFL loads the design from the factory portion of flash memory. When the switch is in the off position, the PFL loads the design from the user portion of flash memory.

The development kit includes the MAX II configuration design in the <*install dir*>**\kits\cycloneIIILS_3cls200_fpga\examples\max2** directory.

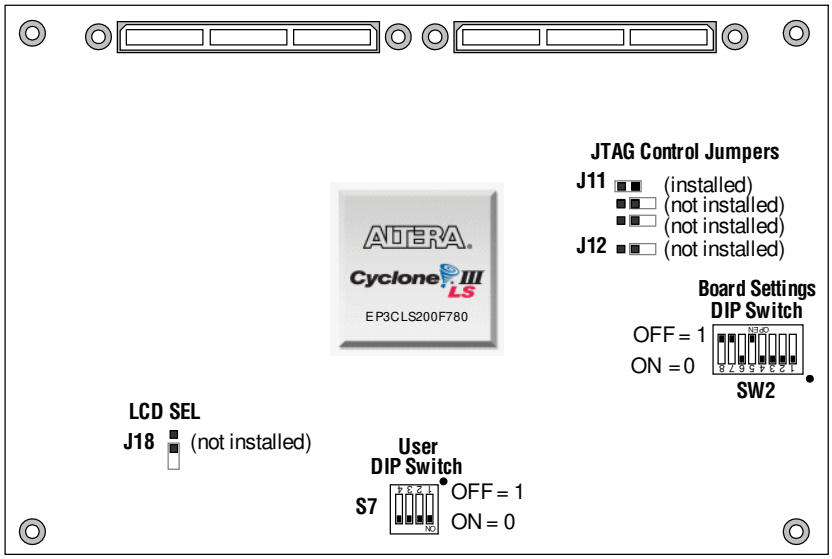
When configuration is complete, the CONF DONE LED (D14) illuminates, signaling that the Cyclone III LS device configured successfully. If the loaded design has the Quartus II software INIT_DONE option on, the FPGA INIT DONE LED (D14) illuminates when the device enters user mode.

For more information about the PFL megafunction, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.

Factory Default Switch Settings

This section shows the factory switch settings for the Cyclone III LS FPGA development board. Figure 4–1 shows the switch bank locations and the default position of each switch.

Figure 4–1. Switch Locations and Default Settings on the FPGA Development Board



To restore the switches to their factory default settings, perform the following steps:

1. Set DIP switch bank (S7) to match Table 4–1 and Figure 4–1.

Table 4–1. S7 Dip Switch Settings

Switch	Position
1	On
2	On
3	On
4	On

2. Set DIP switch bank (SW2) to match Table 4–2 and Figure 4–1.

Table 4–2. SW2 Dip Switch Settings

Switch	Position
1	On
2	On
3	On
4	On
5	Off
6	On
7	Off
8	Off

3. Set the board jumpers to match Table 4–3 and Figure 4–1.

Table 4–3. Jumper Settings

Board Reference	Shunt Position
J11 pins 1-2	Installed
J11 pins 3-4	Not Installed
J11 pins 5-6	Not Installed
J12	Not Installed
J18	Not Installed

For more information about the FPGA board settings, refer to the *Cyclone III LS FPGA Development Board Reference Manual*.

5. Board Update Portal

Introduction

The Cyclone III LS FPGA Development Kit ships with the Board Update Portal example design stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the PGM/USER LOAD switch (SW2.6) in the on position, the Cyclone III LS FPGA configures with the Board Update Portal example design. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user portion of flash memory, and provides links to useful information on the Altera website, including links to kit-specific and design resources.

☞ After successfully updating the flash memory user design, you can load the user design from flash memory into the FPGA. To do so, set the PGM/USER LOAD switch (SW2.6) to the off position and power cycle the board.

The source code for the Board Update Portal design resides in the <*install dir*>**\kits\cycloneIIILS_3cls200_fpga\examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page A–4 to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.

☞ Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform the following steps:

1. With the board powered down, set the PGM/USER LOAD switch (SW2.6) to the on position.
2. Attach the Ethernet cable from the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router, and obtains an IP address. The LCD on the board displays the IP address.
4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

5. Click **Cyclone III LS FPGA Development Kit** on the Board Update Portal web page and verify that you have the latest version of the development kit software (the software version also appears on the CD-ROM).

   If you download new software, double-click the downloaded **.exe** file to begin the installation process.

6. Visit the Board Update Portal web page occasionally for documentation updates and additional new designs not included on the CD-ROM.

If the Board Update Portal does not connect, refer to the Cyclone III LS FPGA Development Kit page on the Altera website to determine if you have the latest kit software.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Design files available from the Cyclone III LS FPGA Development Kit page on the Altera website include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Preparing Design Files for Flash Programming" on page A–2 for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" to access the Board Update Portal web page.
2. In the **Hardware File Name** field specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field, otherwise leave the **Software File Name** field blank.
3. Click **Upload**. The progress bar indicates the percent complete.
4. To configure the FPGA with the new design after the flash memory upload process is complete, set the PGM/USER LOAD switch (SW2.6) to the off position and power cycle the board, or press the PGM_SELECT button (S9) until the PROGRAM LED1 LED (D30) illuminates and then press the PGM CONFIG button (S8). Refer to Table 6–1 on page 6–5 for information about the PROGRAM LEDs.

As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "Restoring the Flash Device to the Factory Settings" on page A–4.

6. Board Test System

Introduction

The kit includes an example design and application called the Board Test System to test the functionality of the Cyclone III LS FPGA development board. The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the application to test board components, modify functional parameters, observe performance, and measure power usage. The application is also useful as a reference for designing systems. To install the application, follow the steps in "Installing the Cyclone III LS FPGA Development Kit" on page 3–2.

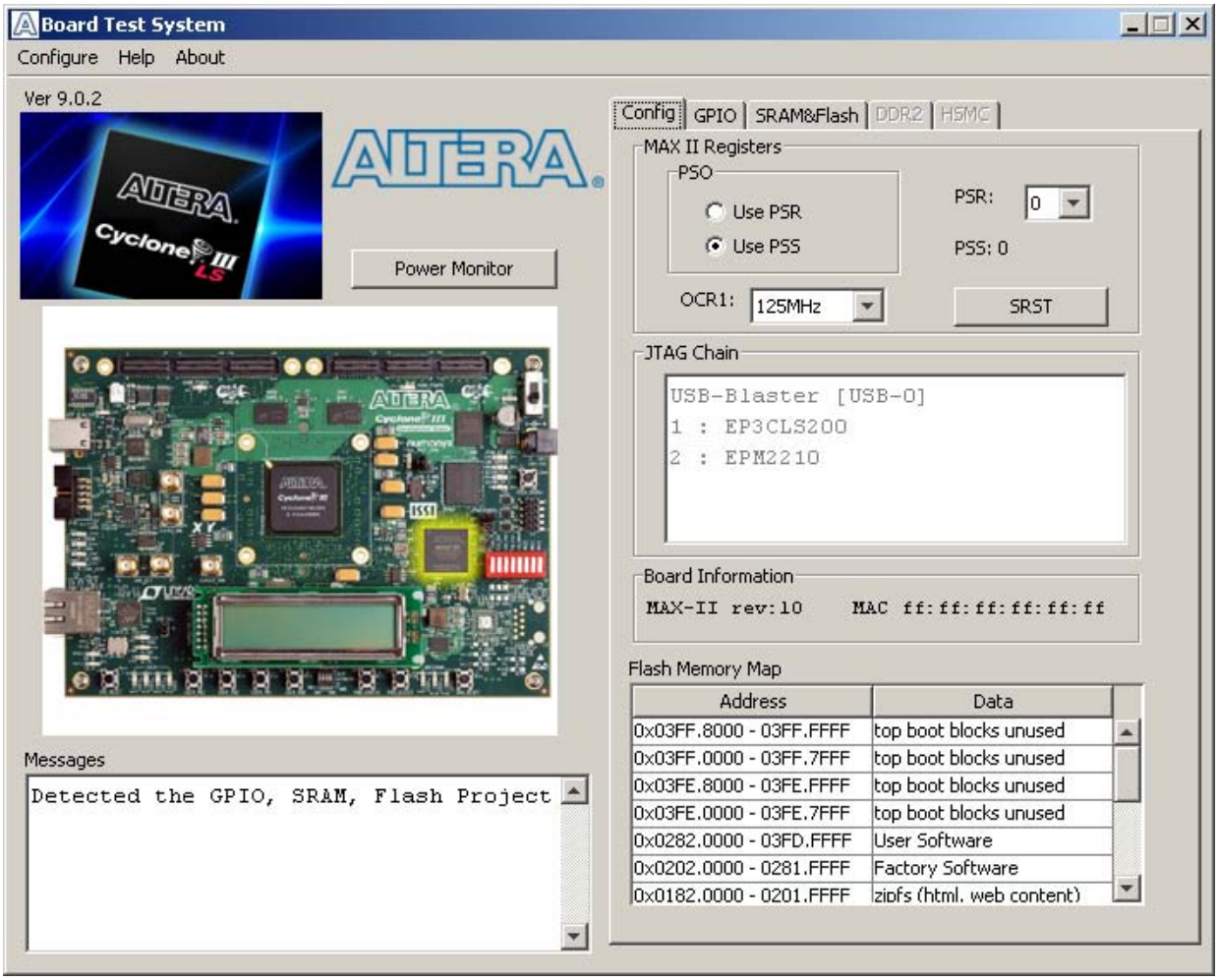
The application provides access to the following Cyclone III LS FPGA development board features:

- General purpose I/O (GPIO)
- SRAM
- Flash memory
- DDR2 memory
- HSMC connectors
- Programmable oscillator

The application allows you to exercise most of the board components. While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.

A GUI runs on the PC which communicates over the JTAG bus to a test design running in the Cyclone III LS device. Figure 6–1 shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The **Power Monitor** button starts the Power Monitor application that measures and reports current power information for the board. Because the application communicates over the JTAG bus to the MAX II device, you can measure the power of any design in the FPGA, including your own designs.

☞ The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board

With the power to the board off, perform the following steps:

1. Connect the USB cable to the board.
2. Verify the settings for the board settings DIP switch bank (SW2) match Table 4–2 on page 4–2.
3. Set the PGM/USER LOAD switch (SW2.6) to the off position.
4. Verify the settings for the JTAG jumper blocks (J11 and J12) match Table 4–3 on page 4–3. These settings determine the devices to include in the JTAG chain.

   For more information about the board's DIP switch and jumper settings, refer to the *Cyclone III LS FPGA Development Board Reference Manual*.

5. Turn the power to the board on. The board loads the design stored in the user portion of flash memory into the FPGA. If your board is still in the factory configuration or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design that tests the GPIO, SRAM, and flash memory loads.

CAUTION

To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the <*install dir*>**\kits\cycloneIIILS_3cls200_fpga\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

On Windows, click **Start** > **All Programs** > **Altera** > **Cyclone III LS FPGA Development Kit** <*version*> > **Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The Cyclone III LS FPGA development board's flash memory ships preconfigured with the design that corresponds to the **Config**, **GPIO**, and **SRAM&Flash** tabs.

If you power up your board with the PGM/USER LOAD switch (SW2.6) in the on position, or if you load your own design into the FPGA with the Quartus II Programmer, you receive a message prompting you to configure your board with a valid Board Test System design. Refer to "The Configure Menu" for information about configuring your board.

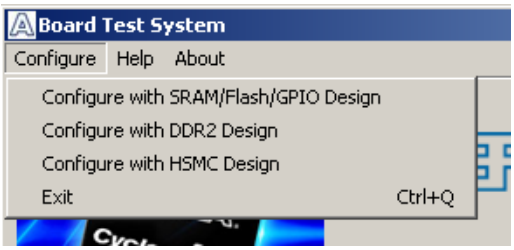
Using the Board Test System

This section describes each control in the Board Test System application.

The Configure Menu

Each test design tests different functionality and corresponds to one or more application tabs. Use the Configure menu to select the design you want to use. Figure 6–2 shows the Configure menu.

Figure 6–2. The Configure Menu



To configure the FPGA with a test system design, perform the following steps:

1. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (**.sof**) to the FPGA. The download process usually takes about a minute.
3. When configuration finishes, click **Close** to complete the configuration process and run the design in the FPGA. A corresponding application tab appears in the GUI that interfaces with the design in the FPGA.

The Config Tab

The **Config** tab shows information about the board's current configuration. Figure 6–1 on page 6–2 shows the **Config** tab. The tab displays the contents of the MAX II registers, the MAX II code version, the JTAG chain, the board's MAC address, and the flash memory map.

The following sections describe the controls on the **Config** tab.

MAX-II Registers

These controls allow you to view and change the current MAX II register values as described in Table 6–1. Changes to the register values with the GUI take effect immediately. For example, selecting a new frequency in the **OCR1** list immediately changes the clock frequency on the board.

Table 6–1. MAX II Registers

Register Name	Read/Write Capability	Description
System Reset (SRST)	Write only	Set to 0 to initiate an FPGA reconfiguration.
Page Select Register (PSR)	Read / Write	Determines which of the two pages of flash memory to use for FPGA reconfiguration. The flash memory ships with pages 0 and 1 preconfigured.
Page Select Override (PSO)	Read / Write	When set to 0, the value in PSR determines the page of flash memory to use for FPGA reconfiguration. When set to 1, the value in PSS determines the page of flash memory to use for FPGA reconfiguration.
Page Select Switch (PSS)	Read only	Holds the current value of the illuminated PROGRAM LED (D29-D31) based on the following encoding: ■ 0 = PROGRAM LED0 LED (D31) and corresponds to the flash memory page for the factory hardware design ■ 1 = PROGRAM LED1 LED (D30) and corresponds to the flash memory page for the user hardware 1 design ■ 2 = PROGRAM LED2 LED (D29) and corresponds to the flash memory page for the user hardware 2 design
Oscillator Control Register 1 (OCR1)	Read / Write	Determines the U17 oscillator output frequency based on the following options: ■ 0 = 100 MHz ■ 1 = 125 MHz ■ 2 = 150 MHz ■ 3 = 156.25 MHz

- **PSO**—Sets the MAX II PSO register. The following options are available:
  - **Use PSR**—Allows the PSR to determine the page of flash memory to use for FPGA reconfiguration.
  - **Use PSS**—Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.
- **PSR**—Sets the MAX II PSR register. The numerical values in the list corresponds to the page of flash memory to load during FPGA reconfiguration. Refer to Table 6–1 for more information.
- **PSS**—Displays the MAX II PSS register value. Refer to Table 6–1 for the list of available options.
- **OCR1**—Sets the MAX II OCR1 register. Refer to Table 6–1 for the list of available options.
- **SRST**—Resets the system and reloads the FPGA with a design from flash memory based on the other MAX II register values. Refer to Table 6–1 for more information.

Because the **Config** tab requires that a specific design is running in the FPGA, writing a 0 to SRST or changing the PSO value can cause the Board Test System to stop running.

JTAG Chain

This control shows all the devices currently in the JTAG chain. The Cyclone III LS device is always the first device in the chain.

Installing the shunt jumper on jumper J11 pins 1-2 includes the MAX II device in the JTAG chain. Installing the shunt jumper on jumper J12 or setting the anti-tamper DIP switch SW2.3 to the off position breaks the JTAG chain.

For information about the anti-tamper design example, refer to *<install dir>*\kits\cycloneIIILS_3cls200_fpga\examples\max2\at_example\readme_at_example.txt.

Board Information

- **MAX-II rev**—Indicates the version of MAX II code currently running on the board. The MAX II code resides in the *<install dir>*\kits\cycloneIIILS_3cls200_fpga\examples directory. Newer revisions of this code might be available on the Cyclone III LS FPGA Development Kit page of the Altera website.
- **MAC**—Indicates the MAC address of the board.

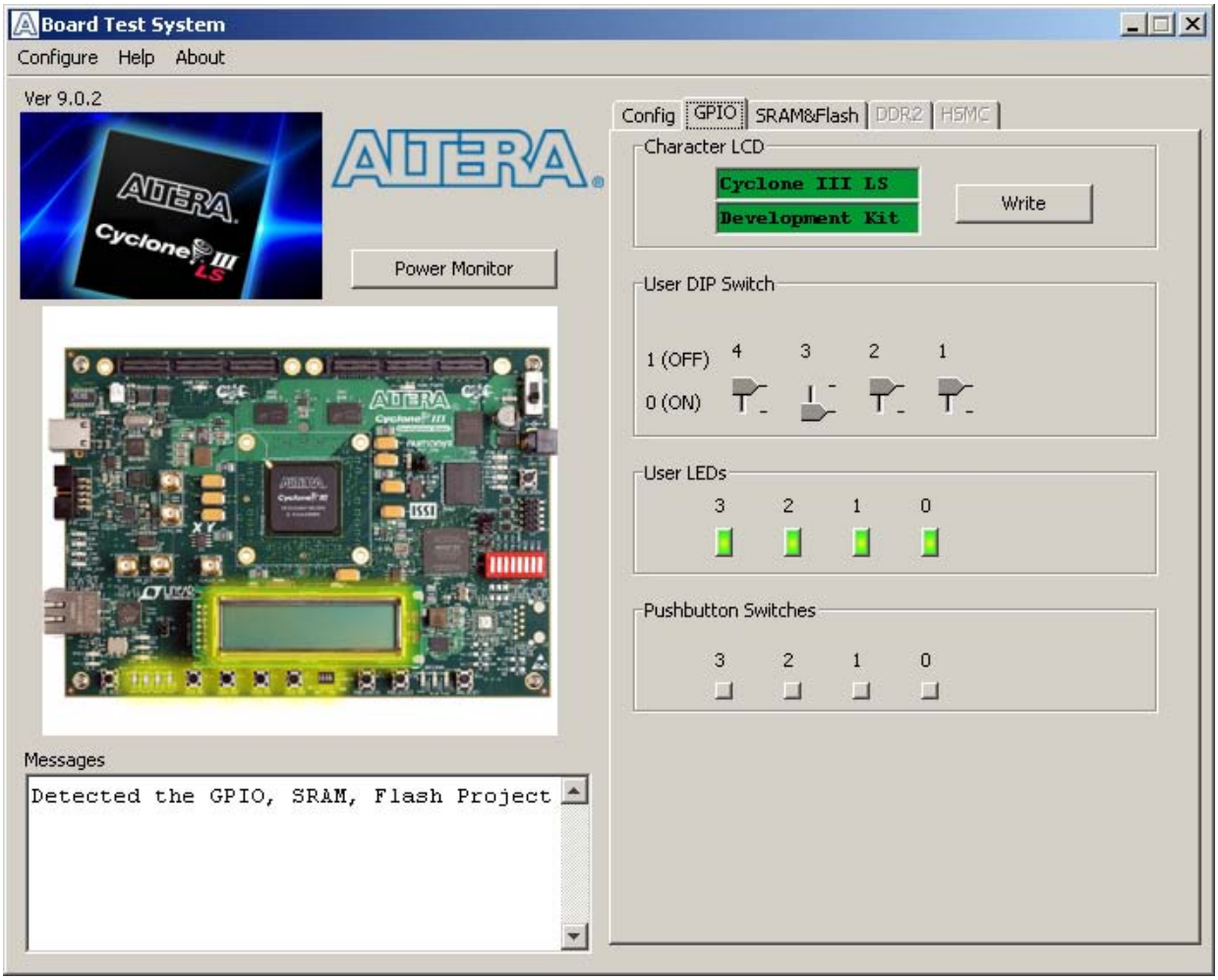
Flash Memory Map

This control shows the memory map of the flash memory device on your board.

The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. You can write to the LCD, read DIP switch settings, turn LEDs on or off, and detect push button presses. Figure 6–3 shows the **GPIO** tab.

Figure 6–3. The GPIO Tab



The following sections describe the controls on the **GPIO** tab.

Character LCD

This control allows you to display text strings on the LCD on your board. Type text in the text boxes and then click **Write**.

☞ If you exceed the 16 character display limit on either line, a warning message appears.

User Dip Switch

This read-only control displays the current positions of the switches in the user DIP switch bank (S7). Change the switches on the board to see the graphical display change accordingly.

User LEDs

This control displays the current state of the user LEDs. Click on the graphical representation of the LEDs to turn the board LEDs on and off.