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Stratix IV GT 100G Development Kit

User Guide

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UG-01091-1.1

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Contents

1. About This Kit

The Altera® Stratix® IV GT 100G Development Kit is a complete design environment that includes both the hardware and software you need to develop Stratix IV GT FPGA designs. The following list describes what you can accomplish with the kit:

- Test signal quality of the FPGA transceiver I/Os (up to 11.3 Gbps)
- Develop and test optical networking interfaces such as CFP, quad small-form-factor pluggable (QSFP), and small form-factor Pluggable (SFP+) interface
- Develop embedded designs utilizing the Nios® II processor and the SSRAM memory
- Develop and test network designs utilizing the Gigabit Ethernet PHY and the FPGA transceivers
- Develop FPGA designs for high-performance applications
- Measure the FPGA's power consumption

Kit Features

This section briefly describes the Stratix IV GT 100G Development Kit contents.

Hardware

The Stratix IV GT 100G Development Kit includes the following hardware:

- Stratix IV GT 100G development board—A development platform that allows you to develop and prototype hardware designs running on the Stratix IV GT EP4S100G5F45I1N FPGA.

  For detailed information about the board components and interfaces, refer to the *Stratix IV GT 100G Development Board Reference Manual*.

- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - USB cable
  - Ethernet cable
  - CFP Loopback board with both passive and active retimed loopback features
  - QSFP loopback module
  - Two SFP+ loopback modules
  - Two Interlaken loopback boards

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software is a licensed set of Altera tools with full functionality. Your kit includes a development kit edition (DKE) license for the Quartus II software (Windows platform only). This license entitles you to all the features of the subscription edition for a period of one year. After the year, you must purchase a renewal subscription to continue using the software. For more information, refer to the Altera website (www.altera.com).

Download the Quartus II Subscription Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.

The Quartus II Subscription Edition Software includes the following items:

- Quartus II Software—The Quartus II software, including the SOPC Builder system development tool, provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system
  - Verify functionality of your design, and quickly and easily evaluate its size and speed
  - Generate time-limited device programming files for designs that include MegaCore functions
  - Program a device and verify your design in hardware

  The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

  For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.
- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allow you to develop embedded software for the Nios II processor which you can include in your Altera FPGA designs.

Stratix IV GT 100G Development Kit Installer

The license-free Stratix IV GT 100G Development Kit installer includes all the documentation and design examples for the kit.

Download the Stratix IV GT 100G Development Kit installer from the Stratix IV GT 100G Development Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.

2. Getting Started

The remaining chapters in this user guide lead you through the following Stratix IV GT 100G development board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the 100G development board
- Configuring the Stratix IV GT FPGA
- Running the Board Test System designs

For complete information about the 100G development board, refer to the *Stratix IV GT 100G Development Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in "Kit Features" on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Board

To inspect board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the Stratix IV GT 100G Development Kit page.
- For the Stratix IV GT device documentation, refer to the Literature: Stratix IV Devices page.
- To purchase devices from the eStore, refer to the Devices page.
- For Stratix IV GT OrCAD symbols, refer to the Capture CIS Symbols page.
- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

This chapter explains how to install the following software:

- Quartus II Subscription Edition Software
- Stratix IV GT 100G Development Kit
- USB-Blaster™ driver

Installing the Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software provides the necessary tools for developing hardware and software for Altera FPGAs. Included in the Quartus II Subscription Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. The Quartus II software (including SOPC Builder) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this kit. To install the Altera development tools, perform the following steps:

1. Run the Quartus II Subscription Edition Software installer you acquired in "Software" on page 1–2.
2. Follow the on-screen instructions to complete the installation process.

If you have difficulty installing the Quartus II software, refer to *Altera Software Installation and Licensing*.

Licensing Considerations

Purchasing this kit entitles you to a one-year DKE license for the Quartus II Subscription Edition Software. Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, you need to obtain and install a license file. To begin, go to the Self Service Licensing Center page of the Altera website, log into or create your myAltera account, and take the following actions:

1. On the Activate Products page, enter the serial number provided with your development kit in the **License Activation Code** box.

   Your serial number is printed on the development kit box below the bottom bar code. The number is 10 or 11 alphanumeric characters and does not contain hyphens. Figure 3–1 shows the correct serial number as 3S150SPXXXX.

Figure 3–1. Locating Your Serial Number

2. Consult the Activate Products table, and to determine how to proceed, follow one of these steps:
   - If the administrator listed for your product is someone other than you, skip the remaining steps and contact your administrator to become a licensed user.
   - If the administrator listed for your product is you, proceed to step 3.
   - If the administrator listed for your product is *Stocking*, activate the product, making you the administrator, and proceed to step 3.
3. Use the Create New License page to license your product for a specific user (you) on specific computers. The Manage Computers and Manage Users pages allow you to add users and computers not already present in the licensing system.

   To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

4. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus II software to enable the software.

For complete licensing details, refer to *Altera Software Installation and Licensing*.

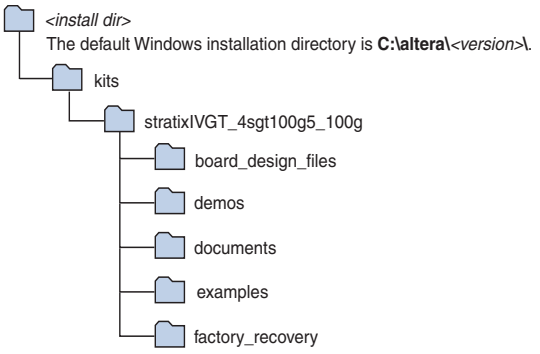
Installing the Stratix IV GT 100G Development Kit

To install the Stratix IV GT 100G Development Kit, perform the following steps:

1. Run the Stratix IV GT 100G Development Kit installer you acquired in "Software" on page 1–2.
2. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you specify is in the same relative location to your Quartus II software as the default locations.

The installation program creates the Stratix IV GT 100G Development Kit directory structure shown in Figure 3–2.

Figure 3–2. Stratix IV GT 100G Development Kit Installed Directory Structure *(1)*



Note to Figure 3–2:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Stratix IV GT 100G Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster Driver

The Stratix IV GT 100G development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster driver on the host computer.

Installation instructions for the USB-Blaster driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

4. Development Board Setup

This chapter explains how to set up the Stratix IV GT 100G development board.

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Stratix IV GT 100G development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be configured with the default settings, follow the instructions in "Factory Default Switch Settings" on page 4–2 to return the board to its factory settings before proceeding.
2. Press FACTORY (S12) to load the Board Update Portal design from flash memory.
3. Connect the DC adapter (18.5 V, 120 W) to the DC power jack (J1) on the FPGA board and plug the cord into a power outlet.

   CAUTION: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

4. Set the POWER switch (SW1) to the on position. When power is supplied to the board, a blue LED (D7) illuminates indicating that the board has power.

The MAX II device on the board contains (among other things) a parallel flash loader (PFL) megafunction. Pressing FACTORY (S12) configures the FPGA with the Board Update Portal from flash. Pressing PGM_SEL (S10) until POF 1 LED illuminates, and then pressing LOAD (S11) button configures the user hardware portion of flash memory.

The kit includes a MAX II design which contains the MAX II PFL megafunction. The design resides in the *<install dir>***kits\stratixIVGT_4sgt100g5_100g\examples\max2** directory.

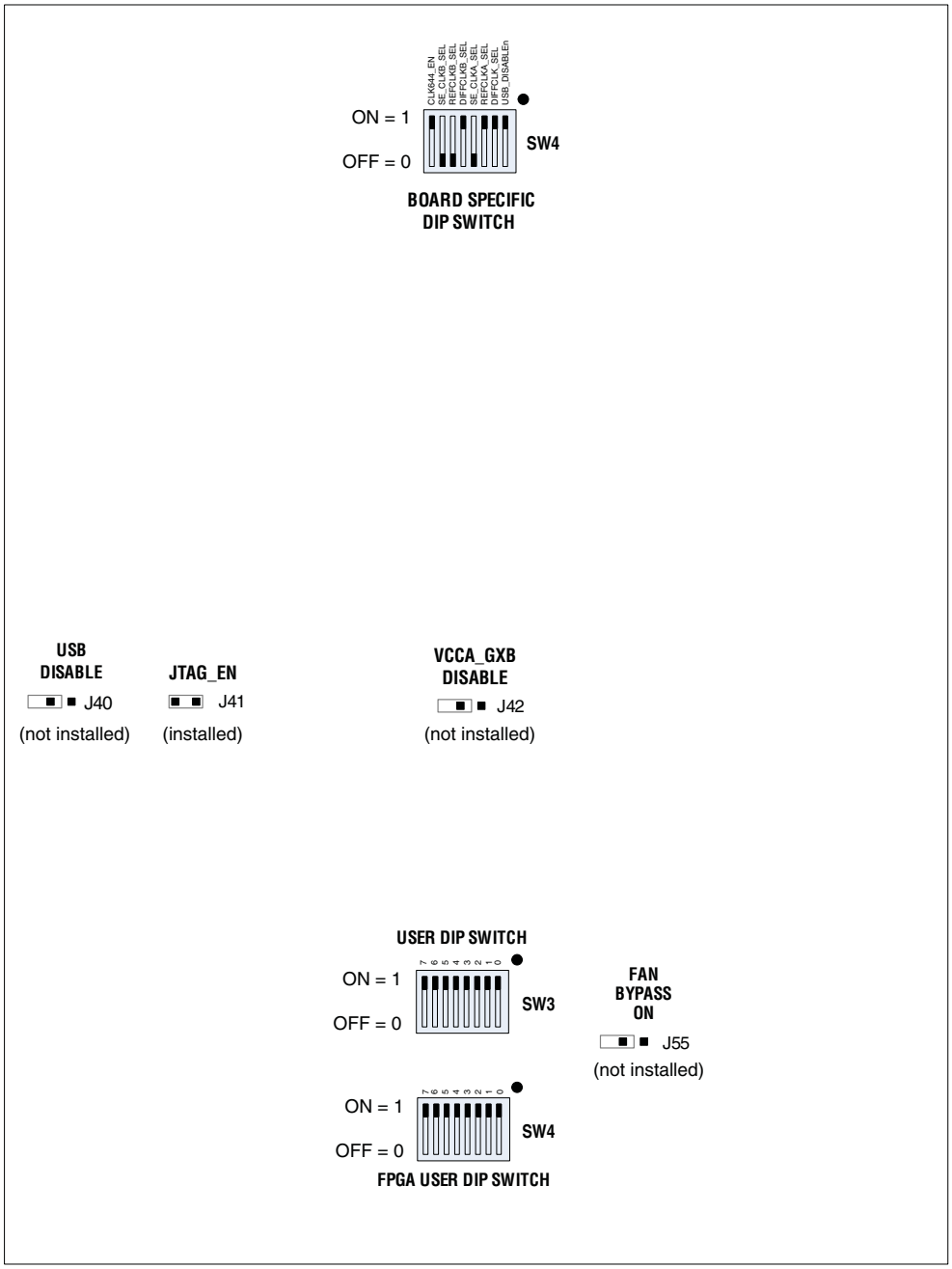
When configuration is complete, the MAX_CONF (D37) illuminates, signaling that you configured the Stratix IV GT device successfully.

For more information about the PFL megafunction, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.

Factory Default Switch Settings

This section shows the factory switch settings for the Stratix IV GT 100G development board. Figure 4–1 shows the switch locations and the default position of each switch on the top side of the board.

Figure 4–1. Switch Locations and Default Settings on the Board Top



To restore the switches to their factory default settings, perform the following steps:

1. Set DIP switch bank (SW2) to match Table 4–1 and Figure 4–1.

2. Set the User DIP Switch bank (SW3) and FPGA User DIP Switch bank (SW4) to the 1 position, as shown in Figure 4–1.

Table 4–1. SW2 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	USB_DISABLEn	Switch 1 has the following options: ■ When on, a logic 1 is selected. Enables the Embedded USB Blaster. ■ When off, a logic 0 is selected. Disables the Embedded USB Blaster.	On
2	DIFFCLKA_SEL	Switch 2 has the following options: ■ When on, a logic 1 is selected. The PLL for the single ended clock goes to the global clock inputs of the A tree structure. ■ When off, a logic 0 is selected. The SMA input for the single ended clock goes to the global clock inputs of the A tree structure.	On
3	REFCLKA_SEL	Switch 3 has the following options: ■ When on, a logic 1 is selected. The PLL goes to the transceivers on the A clock tree structure. ■ When off, a logic 0 is selected. The SMA input goes to the transceivers on the A clock tree structure.	On
4	SE_CLKA_SEL	Switch 4 has the following options: ■ When on, a logic 1 is selected. The SMA for the single ended clock goes to the global clock inputs of the A tree structure. ■ When off, a logic 0 is selected. The PLL for the single ended clock goes to the global clock inputs of the A tree structure.	Off
5	DIFFCLKB_SEL	Switch 5 has the following options: ■ When on, a logic 1 is selected. The PLL for the single ended clock goes to the global clock inputs of the B tree structure. ■ When on, a logic 1 is selected. The PLL for the single ended clock goes to the global clock inputs of the B tree structure.	On
6	REFCLKB_SEL	Switch 6 has the following options: ■ When off, a logic 0 is selected. The PLL goes to the transceivers on the B clock tree structure. ■ When on, a logic 1 is selected. The SMA goes to the transceivers on the B clock tree structure.	Off
7	SE_CLKB_SEL	Switch 7 has the following options: ■ When on, a logic 1 is selected. The SMA for the single ended clock goes to the global clock inputs of the B tree structure. ■ When off, a logic 0 is selected. The PLL for the single ended clock goes to the global clock inputs of the B tree structure.	Off
8	CLK644_EN	Switch 8 has the following options: ■ When on, a logic 1 is selected. Enables the 644.53125MHz clock. ■ When off, a logic 0 is selected. Disables the 644.53125MHz clock.	On

3. Set the board jumpers to match Table 4–2, as shown in Figure 4–1.

Table 4–2. Jumper Settings

Board Reference	Name	Default Shunt Position
J40	USB DISABLE	Not Installed
J41	JTAG_EN	Installed
J42	VCCA_GXB DISABLE	Not Installed
J55	FAN BYPASS ON	Not Installed

For more information about the FPGA board settings, refer to the *Stratix IV GT 100G Development Board Reference Manual*.

5. Board Update Portal

The Stratix IV GT 100G Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

Pressing FACTORY (S12) configures the FPGA with the Board Update Portal design example from flash memory. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware portion of flash memory, and provides links to useful information on the Altera website, including kit-specific links and design resources.

After successfully updating the user hardware flash memory, you can load the user design from flash memory into the FPGA. To do so, press PGM_SEL (S10) until the POF 1 LED illuminates, and then press LOAD (S11) to configure the user hardware portion of flash memory.

The source code for the Board Update Portal design resides in the *<install dir>***kits\stratixIVGT_4sgt100g5_100g\examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page A–4 to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.

Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform the following steps:

1. With the board powered down, attach the Ethernet cable from the board to your LAN.
2. Power up the board. The board connects to the LAN's gateway router, and obtains an IP address. The LCD on the board displays the IP address.
3. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.
4. Click Stratix IV GT 100G Development Kit on the Board Update Portal web page to access the kit's home page. Visit this page occasionally for documentation updates and additional new designs.

You can also navigate directly to the Stratix IV GT 100G Development Kit page of the Altera website to determine if you have the latest kit software.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user hardware portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Design files available from the Stratix IV GT 100G Development Kit page of the Altera website include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Preparing Design Files for Flash Programming" on page A–2 for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" to access the Board Update Portal web page.
2. In the **Hardware File Name** field specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field, otherwise leave the **Software File Name** field blank.
3. Click **Upload**.
4. To configure the FPGA with the new design after the flash memory upload process is complete, press PGM_SEL (S10) until the POF 1 LED illuminates, and then press LOAD (S11) to configure the user hardware portion of flash memory.

As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user hardware portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "Restoring the Flash Device to the Factory Settings" on page A–4.

6. Board Test System

The kit includes a design example and application called the Board Test System to test the functionality of the Stratix IV GT 100G development board. The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the application to test board components, modify functional parameters, observe performance, and measure power usage. The application is also useful as a reference for designing systems. To install the application, follow the steps in "Installing the Stratix IV GT 100G Development Kit" on page 3–2.

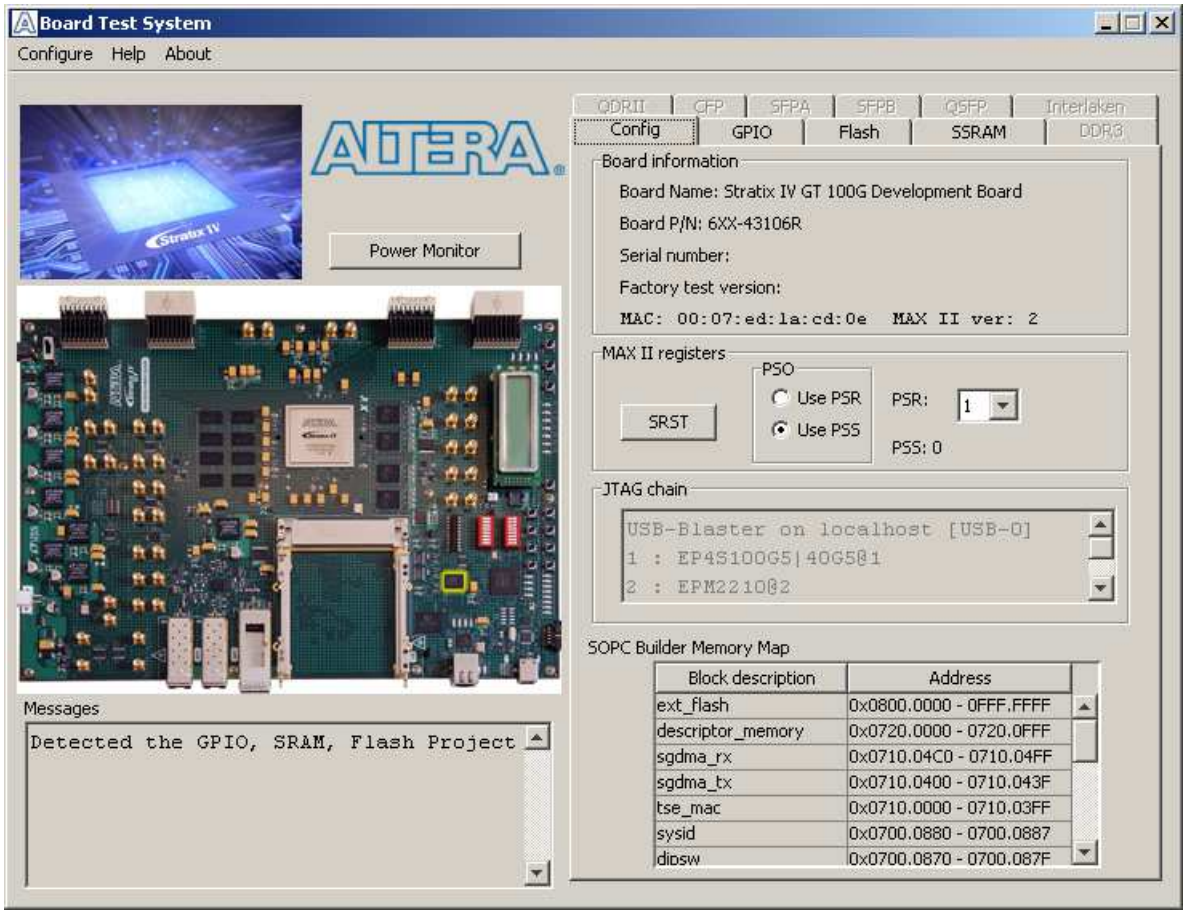
The application provides access to the following Stratix IV GT 100G development board features:

- General purpose I/O (GPIO)
- SRAM
- Flash memory
- Interlaken interfaces
- CFP loopback card
- QSFP optical networking module
- SFP+ optical networking modules
- QDR II SRAM interfaces
- DDR3 SDRAM interfaces

The application allows you to exercise most of the board components. While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.

A GUI runs on the PC which communicates over the JTAG bus to a test design running in the Stratix IV GT device. Figure 6–1 shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The **Power Monitor** button starts the Power Monitor application that measures and reports current power information for the board. Because the application communicates over the JTAG bus to the MAX II device, you can measure the power of any design in the FPGA, including your own designs.

The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II Programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board

With the power to the board off, perform the following steps:

1. Connect the USB cable to the board.
2. Verify the settings for the board settings DIP switches SW2, SW3, and SW4 match Figure 4–1 on page 4–2.

   For more information about the board's DIP switch and jumper settings, refer to the *Stratix IV GT 100G Development Board Reference Manual*.

3. Turn the power to the board on.
4. Press PGM_SEL (S10) until the POF 1 LED illuminates, and then press LOAD (S11) to configure the user hardware portion of flash memory.

   CAUTION: To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the *<install dir>***kits\stratixIVGT_4sgt100g5_100g\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

On Windows, click **Start** > **All Programs** > **Altera** > **Stratix IV GT 100G Development Kit** *<version>* > **Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The Stratix IV GT 100G development board's flash memory ships preconfigured with the design that corresponds to the test tabs.