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Stratix IV E FPGA Development Kit

User Guide

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UG-01067-2.1

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Contents

Appendix A. Programming the Flash Memory Device

Additional Information

1. About This Kit

The Altera® Stratix® IV E FPGA Development Kit is a complete design environment that includes both the hardware and software you need to develop Stratix IV E FPGA designs. The board and the one-year license for the Quartus® II software provide everything you need to begin developing custom Stratix IV E FPGA designs. The following list describes what you can accomplish with the kit:

- Develop and test memory subsystems consisting of DDR3, RLDRAM II, and QDR II+ memories.
- Build designs capable of migrating to Altera's low-cost HardCopy® IV ASICs.
- Take advantage of the modular and scalable design by using the high-speed mezzanine card (HSMC) connectors to interface to over 30 different HSMCs provided by Altera partners, supporting protocols such as Serial RapidIO®, 10 Gigabit Ethernet, SONET, Common Public Radio Interface (CPRI), Open Base Station Architecture Initiative (OBSAI) and others.
- Develop FPGAs design for cost-sensitive applications.
- Measure the FPGA's low power consumption.

Kit Features

This section briefly describes the Stratix IV E FPGA Development Kit contents.

Hardware

The Stratix IV E FPGA Development Kit includes the following hardware:

- Stratix IV E FPGA development board—A development platform that allows you to develop and prototype hardware designs running on the Stratix IV E EP4SE530 FPGA.

  For detailed information about the board components and interfaces, refer to the *Stratix IV E FPGA Development Board Reference Manual*.

- HSMC loopback board—A daughtercard that allows for loopback testing all signals on the HSMC interface using the Board Test System.
- HSMC debug breakout board—A daughtercard that routes 40 CMOS signals to a 0.1" header and adds 20 LEDs to the remaining 40 CMOS signals.
- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - USB cable
  - Ethernet cable

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software is a licensed set of Altera tools with full functionality. Your kit includes a one-year Development Kit license for the Quartus II software (Windows platform only). This license entitles you to all the features of the subscription edition for a period of one year.

After the year, your Development Kit license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software.

Download the Quartus II Subscription Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.

The Quartus II Subscription Edition Software includes the following items:

- Quartus II Software—The Quartus II software, including the Qsys and SOPC Builder system development tool, provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system.
  - Verify functionality of your design, and quickly and easily evaluate its size and speed.
  - Generate time-limited device programming files for designs that include MegaCore functions.
  - Program a device and verify your design in hardware.

  The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

  For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.
- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allow you to develop embedded software for the Nios II processor which you can include in your Altera FPGA designs.

Stratix IV E FPGA Development Kit Installer

The license-free Stratix IV E FPGA Development Kit installer includes all the documentation and design examples for the kit.

Download the Stratix IV E FPGA Development Kit installer from the Stratix IV E FPGA Development Kit page of the Altera website. Alternatively, you can request a Development Kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.

2. Getting Started

The remaining chapters in this user guide lead you through the following Stratix IV E FPGA development board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the FPGA development board
- Configuring the Stratix IV E FPGA
- Running the Board Test System designs

For complete information about the FPGA development board, refer to the *Stratix IV E FPGA Development Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in "Kit Features" on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Board

To inspect the board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.

In typical applications with the Stratix IV E FPGA development board, a heat sink is not necessary. However, under extreme conditions or for engineering sample silicon the board might require additional cooling to stay within operating temperature guidelines. You can perform power consumption and thermal modeling to determine whether your application requires additional cooling. For information about measuring board and FPGA temperature in real time, refer to "The Power Monitor" on page 6–21.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the Stratix IV E FPGA Development Kit page.
- For additional daughter cards available for purchase, refer to the Development Board Daughtercards page.
- For the Stratix IV E device documentation, refer to the Literature: Stratix IV Devices page.
- To purchase devices from the eStore, refer to the Devices page.
- For Stratix IV E OrCAD symbols, refer to the Capture CIS Symbols page.
- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

This chapter explains how to install the following software:

- Quartus II Subscription Edition Software
- Stratix IV E FPGA Development Kit
- USB-Blaster™ driver

Installing the Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software provides the necessary tools used for developing hardware and software for Altera FPGAs. Included in the Quartus II Subscription Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. The Quartus II software (including Qsys and SOPC Builder) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this kit. To install the Altera development tools, perform the following steps:

1. Run the Quartus II Subscription Edition Software installer you acquired in "Software" on page 1–2.
2. Follow the on-screen instructions to complete the installation process.

If you have difficulty installing the Quartus II software, refer to *Altera Software Installation and Licensing Manual*.

Licensing Considerations

Purchasing this kit entitles you to a one-year Development Kit license for the Quartus II Subscription Edition Software.

After the year, your Development Kit license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software.

Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the Subscription Edition, you can use that license file with this kit. If not, you need to obtain and install a license file. To begin, go to the Self Service Licensing Center page of the Altera website, log into or create your myAltera account, and take the following actions:

1. On the Activate Products page, enter the serial number provided with your development kit in the **License Activation Code** box.

Your serial number is printed on the development kit box below the bottom bar code. The number is 10 or 11 alphanumeric characters and does not contain hyphens. Figure 3–1 shows *3S150SPXXXX* as an example serial number.

Figure 3–1. Locating Your Serial Number

2. Consult the Activate Products table, to determine how to proceed.
   a. If the administrator listed for your product is someone other than you, skip the remaining steps and contact your administrator to become a licensed user.
   b. If the administrator listed for your product is you, proceed to step 3.
   c. If the administrator listed for your product is *Stocking*, activate the product, making you the administrator, and proceed to step 3.
3. Use the Create New License page to license your product for a specific user (you) on specific computers. The Manage Computers and Manage Users pages allow you to add users and computers not already present in the licensing system.

   To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

4. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus_II software to enable the software.

For complete licensing details, refer to *Altera Software Installation and Licensing Manual*.

Installing the Stratix IV E FPGA Development Kit

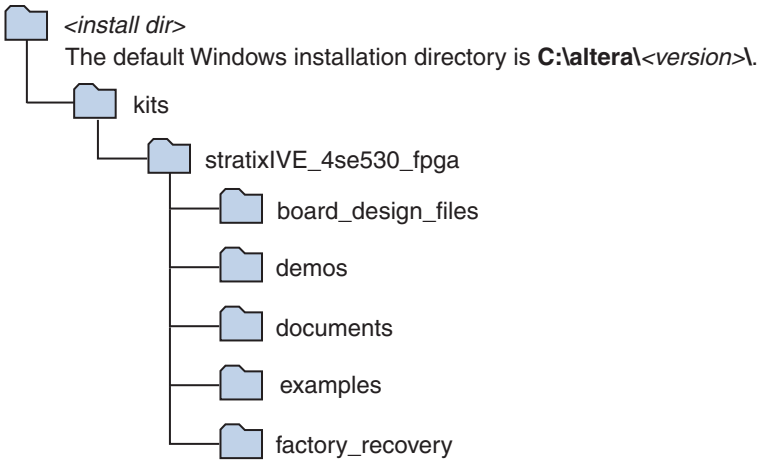
To install the Stratix IV E FPGA Development Kit, perform the following steps:

1. Run the Stratix IV E FPGA Development Kit installer you acquired in "Software" on page 1–2.

2. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you choose is in the same relative location to your Quartus II software as the default locations.

The installation program creates the Stratix IV E FPGA Development Kit directory structure shown in Figure 3–2.

Figure 3–2. Stratix IV E FPGA Development Kit Installed Directory Structure *(1)*



Note to Figure 3–2:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications, if present; not all kits include demos.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Stratix IV E FPGA Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster Driver

The Stratix IV E FPGA development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster driver on the host computer.

Installation instructions for the USB-Blaster driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

4. Development Board Setup

The instructions in this chapter explain how to set up the Stratix IV E FPGA development board.

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Stratix IV E FPGA development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch Settings" on page 4–2 to return the board to its factory settings before proceeding.
2. The FPGA development board ships with design examples stored in the flash memory device. Verify the PGM CONFIG SELECT rotary switch (SW5) is set to the 0 position to load the design stored in the factory portion of flash memory. Figure 4–1 shows the switch location on the Stratix IV E FPGA development board.
3. Connect the DC adapter (+16 V, 3.75 A) to the DC power jack (J22) on the FPGA board and plug the cord into a power outlet.

   CAUTION: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

4. Set the POWER switch (SW3) to the on position. When power is supplied to the board, a blue LED (D21) illuminates indicating that the board has power.

The MAX II device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. The PGM CONFIG SELECT rotary switch (SW5) controls which design to load. When the switch is in the 0 position, the PFL loads the design from the factory portion of flash memory. When the switch is in the 1 position, the PFL loads the design from the user hardware portion of flash memory.

The kit includes a MAX II design which contains the MAX II PFL megafunction. The design resides in the *<install dir>***kits****stratixIVE_4se530_fpga****examples****max2** directory.

When configuration is complete, the CONF DONE LED (D22) illuminates, signaling that the Stratix IV E device configured successfully.

For more information about the PFL megafunction, refer to *Parallel Flash Loader Megafunction User Guide*.

Factory Default Switch Settings

This section shows the factory switch settings for the Stratix IV E FPGA development board. Figure 4–1 shows the switch locations and the default position of each switch on the top side of the board.

Figure 4–1. Switch Locations and Default Settings on the Board Top

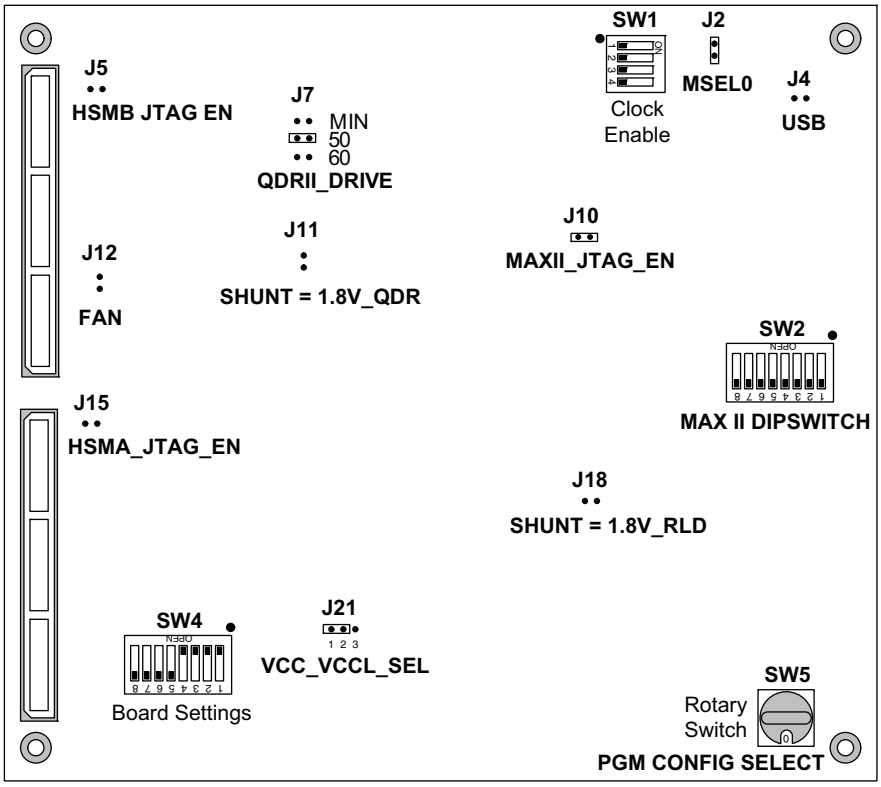
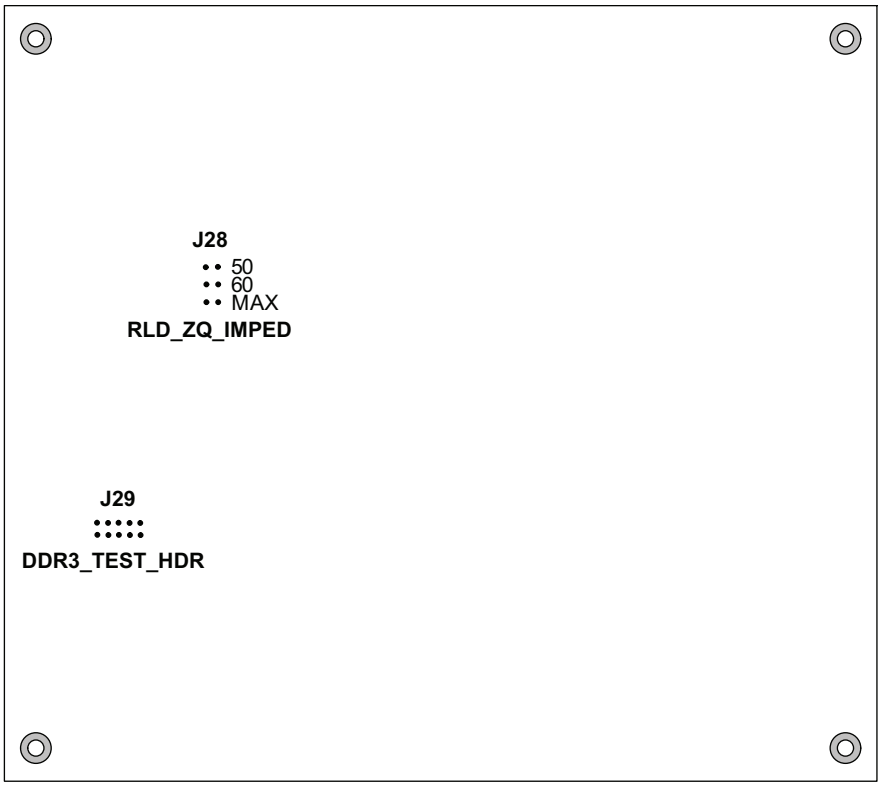


Figure 4–2 shows the switch locations and the default position of each switch on the bottom side of the board.

Figure 4–2. Switch Locations and Default Settings on the Board Bottom



To restore the switches to their factory default settings, perform the following steps:

1. Set the PGM CONFIG SELECT rotary switch (SW5) to the 0 position, as shown in Figure 4–1.
2. Set DIP switch bank (SW1) to match Table 4–1 and Figure 4–1.

Table 4–1. SW1 Dip Switch Settings (Part 1 of 2)

Switch	Board Label	Function	Default Position
1	CLK50_EN	Switch 1 has the following options: ■ When on, the 50 MHz clock is disabled. ■ When off, the 50 MHz clock is enabled.	Off
2	CLK66_EN	Switch 2 has the following options: ■ When on, the 66 MHz clock is disabled. ■ When off, the 66 MHz clock is enabled.	Off

Table 4–1. SW1 Dip Switch Settings (Part 2 of 2)

Switch	Board Label	Function	Default Position
3	CLK100_EN	Switch 3 has the following options: ■ When on, the 100 MHz clock is disabled. ■ When off, the 100 MHz clock is enabled.	Off
4	CLK125_EN	Switch 4 has the following options: ■ When on, the 125 MHz clock is disabled. ■ When off, the 125 MHz clock is enabled.	Off

3. Set DIP switch bank (SW2) to match Table 4–2 and Figure 4–1.

Table 4–2. SW2 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	DIP0	Switch 1 is a MAX II user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Closed
2	DIP1	Switch 2 is a MAX II user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Closed
3	DIP2	Switch 3 is a MAX II user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Closed
4	DIP3	Switch 4 is a MAX II user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Closed
5	DIP4	Switch 5 is a MAX II user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Closed
6	DIP5	Switch 6 is a MAX II user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Closed
7	DIP6	Switch 7 is a MAX II user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Closed
8	CLK66_SEL	Switch 8 has the following options: ■ When closed, the 66 MHz clock is selected. ■ When open, the SMA input clock is selected.	Closed

4. Set DIP switch bank (SW4) to match Table 4–3 and Figure 4–1.

Table 4–3. SW4 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	USER_DIPSW0	Switch 1 is a user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Open
2	USER_DIPSW1	Switch 2 is a user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Open
3	USER_DIPSW2	Switch 3 is a user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Open
4	USER_DIPSW3	Switch 4 is a user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Open
5	USER_DIPSW4	Switch 5 is a user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Closed
6	USER_DIPSW5	Switch 6 is a user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Closed
7	USER_DIPSW6	Switch 7 is a user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Closed
8	USER_DIPSW7	Switch 8 is a user-defined switch and has the following options: ■ When closed, a logic 0 is selected. ■ When open, a logic 1 is selected.	Closed

5. Set the board jumpers to match Table 4–4, Figure 4–1, and Figure 4–2.

CAUTION Installing shunts in certain configurations might cause damage to devices on your board. Pay specific attention to the Function column details.

Table 4–4. Jumper Settings (Part 1 of 2)

Board Reference	Board Label	Function	Default Shunt Position
J2	MSEL0	This jumper has the following options: ■ Installing the shunt sets MSEL0 to logic 0. ■ Removing the shunt sets MSEL0 to logic 1.	Installed
J4	USB DISABLE	This jumper has the following options: ■ Installing the shunt disables the onboard USB-Blaster. ■ Removing the shunt enables the onboard USB-Blaster.	Not installed
J5	HSMB_JTAG_EN	This jumper has the following options: ■ Installing the shunt includes HSMC port B in the JTAG chain. ■ Removing the shunt removes HSMC port B from the JTAG chain.	Not installed
J7	QDRII DRIVE	This jumper has the following options: ■ Installing the shunt on pins 1 and 2 sets the QDR II output impedance to the minimum value possible. ■ Installing the shunt on pins 3 and 4 sets the QDR II output impedance to 50 Ω ■ Installing the shunt on pins 5 and 6 sets the QDR II output impedance to 60 Ω Always keep one and only one shunt installed. Other configurations might cause damage to the device.	Installed on pins 3 and 4
J10	MAXII_JTAG_EN	This jumper has the following options: ■ Installing the shunt includes the MAX II EMP2210 device in the JTAG chain. ■ Removing the shunt removes the MAX II device from the JTAG chain.	Installed
J11	SHUNT=1.8V QDR	This jumper has the following options: ■ Installing the shunt sets QDR II VDDQ to 1.8 V. ■ Removing the shunt sets QDR II VDDQ to 1.5 V.	Not installed
J15	HSMA_JTAG_EN	This jumper has the following options: ■ Installing the shunt includes HSMC port A in the JTAG chain. ■ Removing the shunt removes HSMC port A from the JTAG chain.	Not installed
J18	SHUNT=1.8V RLD	This jumper has the following options: ■ Installing the shunt sets RLDRAM II VDDQ to 1.8 V. ■ Removing the shunt sets RLDRAM II VDDQ to 1.5 V.	Not installed

Table 4–4. Jumper Settings (Part 2 of 2)

Board Reference	Board Label	Function	Default Shunt Position
J21	VCC_VCCL_SEL	This jumper has the following options: ■ Installing the shunt on pins 1 and 2 sets VCC and VCCL to 0.9 V. ■ Installing the shunt on pins 2 and 3 sets VCC and VCCL to 1.1 V. ■ Removing the shunt sets VCC and VCCL to 0.6 V. Always keep a shunt installed on pins 1 and 2 only. The current version of the Stratix IV E device requires 0.9 V.	Installed on pins 1 and 2
J28	RLD_ZQ_IMPED	To use the RLDRAM II impedance drive jumpers, set the mode register. When the mode register is not set, the RLDRAM II output impedance is 50 Ω The RLDRAM II impedance drive jumpers have the following options: ■ Installing the shunt on pins 1 and 2 sets the RLDRAM II output impedance to the maximum value possible. ■ Installing the shunt on pins 3 and 4 sets the RLDRAM II output impedance to 50 Ω ■ Installing the shunt on pins 5 and 6 sets the RLDRAM II output impedance to 60 Ω Installing more than one shunt might cause damage to the device.	Not installed

For more information about the FPGA board settings, refer to the *Stratix IV E FPGA Development Board Reference Manual*.

5. Board Update Portal

The Stratix IV E FPGA Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the PGM CONFIG SELECT rotary switch (SW5) in the 0 position, the Stratix IV E FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware portion of flash memory, and provides links to useful information on the Altera website, including kit-specific links and design resources.

☞ After successfully updating the user hardware flash memory, you can load the user design from flash memory into the FPGA. To do so, set the PGM CONFIG SELECT rotary switch (SW5) to the 1 position and power cycle the board.

The source code for the Board Update Portal design resides in the <*install dir*>**\kits\stratixIVE_4se530_fpga\examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page A–4 to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.

☞ Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform the following steps:

1. With the board powered down, set the PGM CONFIG SELECT rotary switch (SW5) to the 0 position.
2. Attach the Ethernet cable from the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router, and obtains an IP address. The LCD on the board displays the IP address.
4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.