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Arria V GX FPGA Development Kit

User Guide

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UG-01112-1.0

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Contents

Appendix A. Programming the Flash Memory Device

Additional Information

1. About This Kit

The Altera® Arria® V GX FPGA Development Kit is a complete design environment that includes both the hardware and software you need to develop Arria V GX FPGA designs.

Kit Features

This section briefly describes the Arria V GX FPGA Development Kit contents.

Hardware

The Arria V GX FPGA Development Kit includes the following hardware:

- Arria V GX FPGA development board—A development platform that allows you to develop and prototype hardware designs running on the Arria V GX 5AGXFB3H4F40C5NES FPGA.

  For detailed information about the board components and interfaces, refer to the *Arria V GX FPGA Development Board Reference Manual*.

- HSMC loopback daughtercard
- HSMC debug daughtercard
- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - USB cable
  - Ethernet cable
  - Samtec high-speed Bull's Eye kit with 22-position connector, four SMA cables and tool

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Software

Your kit includes a license for the Development Kit Edition (DKE) of the Quartus II software (Windows platform only). For one year, this license entitles you to most of the features of the Subscription Edition (excluding the IP Base Suite).

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software. For more information, refer to the Design Software page of the Altera website.

The Quartus II Development Kit Edition (DKE) software includes the following items:

- Quartus II Software—The Quartus II software, including the Qsys system integration tool, provides a comprehensive environment for network on a chip (NoC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system.
  - Verify functionality of your design, and quickly and easily evaluate its size and speed.
  - Generate time-limited device programming files for designs that include MegaCore functions.
  - Program a device and verify your design in hardware.

  The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

  For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.
- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allows you to develop embedded software for the Nios II processor which you can include in your Altera FPGA designs.

Arria V GX FPGA Development Kit Installer

The license-free Arria V GX FPGA Development Kit installer includes all the documentation and design examples for the kit.

For information on installing the Development Kit Installer, refer to "Software Installation" on page 3–1.

The remaining chapters in this user guide lead you through the following Arria V GX FPGA development board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the FPGA development board
- Configuring the Arria V GX FPGAs
- Running the Board Test System designs

For complete information about the FPGA development board, refer to the *Arria V GX FPGA Development Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the boards to verify that you received all of the items listed in "Kit Features" on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Boards

To inspect each board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components on the board appear in place and intact.

In typical applications with the Arria V GX FPGA development board, a heat sink is not necessary. However, under extreme conditions or for engineering sample silicon the board might require additional cooling to stay within operating temperature guidelines. The board has two holes near the FPGAs that accommodate many different heat sinks, including the Dynatron CHR-152. You can perform power consumption and thermal modeling to determine whether your application requires additional cooling. For information about measuring board and FPGA power in real time, refer to "The Power Monitor" on page 6–24.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the Arria V GX FPGA Development Kit page.
- For additional daughter cards available for purchase, refer to the Development Board Daughtercards page.
- For the Arria V GX device documentation, refer to the Documentation: Arria V Devices page.
- To purchase devices from the eStore, refer to the Devices page.
- For Arria V GX OrCAD symbols, refer to the Capture CIS Symbols page.
- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

This chapter explains how to install the following software:

- Quartus II Subscription Edition Software
- Arria V GX FPGA Development Kit
- USB-Blaster™ II driver

Installing the Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software provides the necessary tools used for developing hardware and software for Altera devices. Included in the Quartus II Subscription Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. The Quartus II software (including SOPC Builder) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this kit. To install the Altera development tools, perform the following steps:

1. Download the Quartus II Subscription Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.
2. Follow the on-screen instructions to complete the installation process.

If you have difficulty installing the Quartus II software, refer to *Altera Software Installation and Licensing Manual*.

Licensing Considerations

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus II software.

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software.

Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, you need to obtain and install a license file. To begin, go to the Self Service Licensing Center page of the Altera website, log into or create your myAltera account, and take the following actions:

1. On the Activate Products page, enter the serial number provided with your development kit in the **License Activation Code** box.

Your serial number is printed on the development kit box below the bottom bar code. The number is 10 or 11 alphanumeric characters and does not contain hyphens. Figure 3–1 shows *3S150SPXXXX* as an example serial number.

Figure 3–1. Locating Your Serial Number

2. Consult the Activate Products table, to determine how to proceed.
   a. If the administrator listed for your product is someone other than you, skip the remaining steps and contact your administrator to become a licensed user.
   b. If the administrator listed for your product is you, proceed to step 3.
   c. If the administrator listed for your product is *Stocking*, activate the product, making you the administrator, and proceed to step 3.
3. Use the Create New License page to license your product for a specific user (you) on specific computers. The Manage Computers and Manage Users pages allow you to add users and computers not already present in the licensing system.

   To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

4. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus_II software to enable the software.

For complete licensing details, refer to *Altera Software Installation and Licensing Manual*.

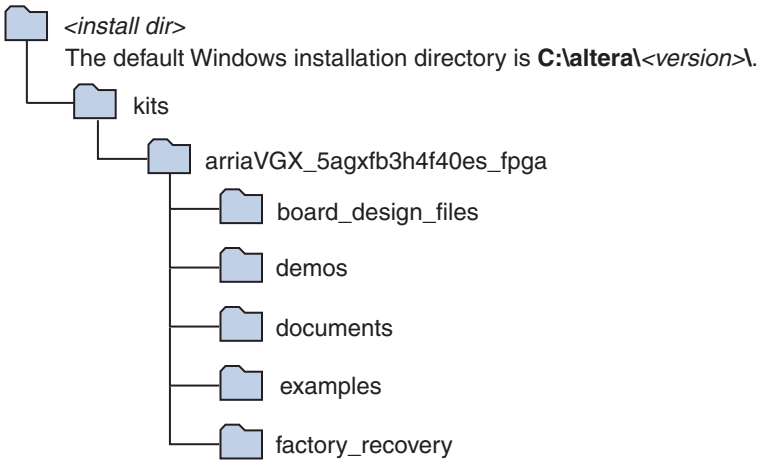
Installing the Arria V GX FPGA Development Kit

To install the Arria V GX FPGA Development Kit, perform the following steps:

1. Download the Arria V GX FPGA Development Kit installer from the Arria V GX FPGA Development Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.
2. Run the Arria V GX FPGA Development Kit installer.
3. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you choose is in the same relative location to the Quartus II software installation.

The installation program creates the Arria V GX FPGA Development Kit directory structure shown in Figure 3–2.

Figure 3–2. Arria V GX FPGA Development Kit Installed Directory Structure *(1)*



Note to Figure 3–2:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications, if present.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Arria V GX FPGA Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster II Driver

The Arria V GX FPGA development board includes integrated On-Board USB-Blaster II circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster II driver on the host computer.

Installation instructions for the USB-Blaster II driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

For USB-Blaster II configuration details, refer to the On-Board USB-Blaster II page.

4. Development Board Setup

The instructions in this chapter explain how to set up the Arria V GX FPGA development board.

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Arria V GX FPGA development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch and Jumper Settings" on page 4–2 to return the board to its factory settings before proceeding.
2. The development board ships with design examples stored in the flash memory device. Verify the Load Selector (SW5.3) is in the on (factory) position to load the design stored in the factory portion of flash memory. Figure 4–1/Figure 4–2 shows the switch locations on the Arria V GX FPGA development board.
3. Connect the +19 V, 6.32 A to the DC Power Jack (J6) on the FPGA board and plug the cord into a power outlet.

   CAUTION: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage, and a lower-rated power supply may not be able to provide enough power for the board.

4. Set the POWER switch (SW1) to the on position. When power is supplied to the board, blue LED (D1) illuminates indicating that the board has power.

The MAX II device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. The Load Selector (SW5.3) controls which design to load. When the switch is in the on (factory) position, the PFL loads the design from the factory portion of flash memory.

The kit includes a MAX II design which contains the MAX II PFL megafunction. The design resides in the *<install dir>*\kits\arriaVGX_5agxfb3hf40es_fpga\examples\max2 directory.

When configuration is complete, the Config Done LED (D16) illuminates, signaling that the Arria V GX device configured successfully.

For more information about the PFL megafunction, refer to *Parallel Flash Loader Megafunction User Guide*.

Factory Default Switch and Jumper Settings

This section shows the factory switch and jumper settings for the Arria V GX FPGA development board. Figure 4–1 shows the switch and jumper locations and the default position of each switch and jumper on the top side of the board.

Figure 4–1. Switch Locations and Default Settings on the Board Top

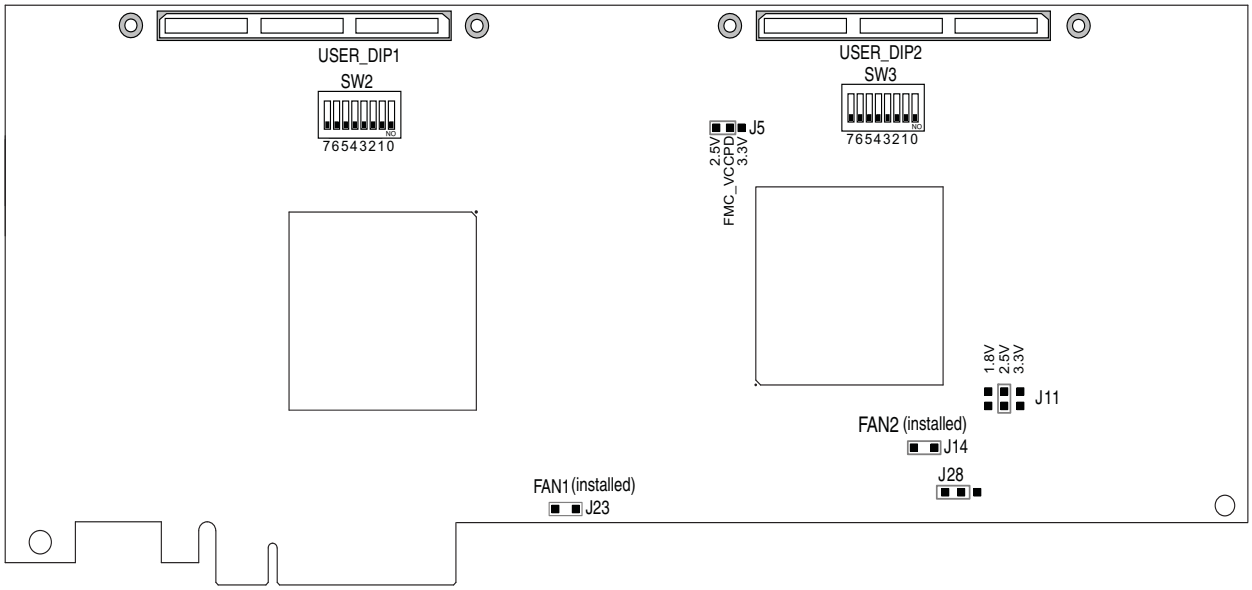
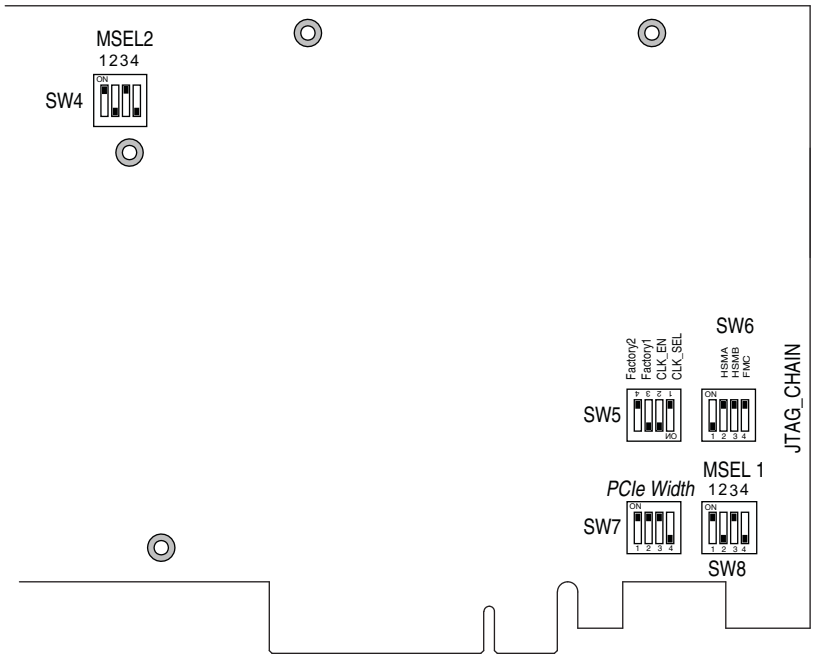


Figure 4–2 shows the switch locations and the default position of each switch on the bottom side of the board.

Figure 4–2. Switch Locations and Default Settings on the Board Bottom



To restore the switches to their factory default settings, perform the following steps:

1. Set DIP switch bank (SW4) to match Table 4–1 and Figure 4–2.

Table 4–1. SW4 FPGA2 MSEL Dip Switch Settings *(1)*

Switch	Board Label	Function	Default Position
1	FPGA2_MSEL[1]	Switch 1 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	ON
2	FPGA2_MSEL[2]	Switch 2 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF
3	—	—	ON
4	FPGA2_MSEL[4]	Switch 4 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF

Note to: Table 4–1

(1) Ensure that all MSEL setting are in a defined configuration scheme as shown in Volume 2: Device Interfaces and Integration of the *Arria V Device Handbook*.

2. Set DIP switch bank (SW5) to match Table 4–2 and Figure 4–2.

Table 4–2. SW5 Board Settings Dip Switch

Switch	Board Label	Function	Default Position
1	CLK_SEL	Switch 1 has the following options: ■ ON, (logical 0) = SMA input clock select. ■ OFF, (logical 1) = programmable oscillator clock select.	OFF
2	CLK_EN	Switch 2 has the following options: ■ ON, (logical 0) = on-board oscillator disable. ■ OFF, (logical 1) = on-board oscillator enable.	ON
3	Factory1	Switch 3 has the following options: ■ ON, (logical 0) = load the factory design for Arria V FPGA 1 from flash at power up. ■ OFF, (logical 1) = load the user design for Arria V FPGA 1 from flash at power up.	ON
4	Factory2	Switch 4 is for factory test only.	OFF

3. Set DIP switch bank (SW6) to match Table 4–3 and Figure 4–2.

Table 4–3. SW6 JTAG Dip Switch Settings

Switch	Board Label	Function	Default Position
1	—	—	OFF
2	HSMA_JTAG_EN	Switch 2 has the following options: ■ ON, (logical 0) = HCMC Port A not in JTAG chain. ■ OFF, (logical 1) = Include HCMC Port A in the JTAG chain.	ON
3	HSMB_JTAG_EN	Switch 3 has the following options: ■ ON, (logical 0) = HCMC Port B not in JTAG chain. ■ OFF, (logical 1) = Include HCMC Port B in the JTAG chain.	ON
4	FMC_JTAG_EN	Switch 4 has the following options: ■ ON, (logical 0) = FMC connector not in JTAG chain. ■ OFF, (logical 1) = Include FMC connector in the JTAG chain.	ON

4. Set DIP switch bank (SW7) to match Table 4–4 and Figure 4–2.

Table 4–4. SW7 PCIe DIP Switch Settings

Switch	Board Label	Function	Default Position
1	PCIE_PRSNT2n_x1	Switch 1 has the following options: ■ ON (0) = x1 presence detect is enabled. ■ OFF (1) = x1 presence detect is disabled.	ON
2	PCIE_PRSNT2n_x4	Switch 2 has the following options: ■ ON (0) = x4 presence detect is enabled. ■ OFF (1) = x4 presence detect is disabled.	ON
3	PCIE_PRSNT2n_x8	Switch 3 has the following options: ■ ON (0) = x8 presence detect is enabled. ■ OFF (1) = x8 presence detect is disabled.	ON
4	—	—	OFF

5. Set DIP switch bank (SW8) to match Table 4–5 and Figure 4–2.

Table 4–5. SW8 FPGA1 MSEL Dip Switch Settings *(1)*

Switch	Board Label	Function	Default Position
1	FPGA1_MSEL[1]	Switch 1 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	ON
2	FPGA1_MSEL[2]	Switch 2 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF
3	—	—	ON
4	FPGA1_MSEL[4]	Switch 4 has the following options: ■ When ON, a logic 0 is selected. ■ When OFF, a logic 1 is selected.	OFF

Note to: Table 4–5

(1) Ensure that all MSEL setting are in a defined configuration scheme as shown in Volume 2: Device Interfaces and Integration of the *Arria V Device Handbook*.

6. Set the board jumpers to match Table 4–6, Figure 4–1 and Figure 4–2.

Table 4–6. Jumper Settings (Part 1 of 2)

Board Reference	Board Label	Function	Default Position
J5	FMC_VCCPD	This jumper has the following options: ■ Installing the shunt on pins 1-2 provides 2.5 V on FMC_VCCPD. ■ Installing the shunt on pins 2-3 provides 3.3 V on FMC_VCCPD.	Pins 1-2
J11	FMC_VCCIO_SEL	This jumper has the following options: ■ No shunt = 1.5V ■ Shunt on pins 1-2 = 1.8V ■ Shunt on pins 3-4 = 2.5V ■ Shunt on pins 5-6 = 3.3V Note: When setting this jumper to 3.3 V, make sure the FMC_VCCPD is on the correct setting (J5 shunt on pins 2-3).	Pins 3-4
J14	FAN2	Powers the fan for FPGA 2	Installed

Table 4–6. Jumper Settings (Part 2 of 2)

Board Reference	Board Label	Function	Default Position
J28	FMC_VCCIO_SRC	This jumper has the following options: ■ Installing the shunt on pins 1-2 powers bank 4B when there is no FMC card installed or the FMC card does not provide a voltage for this rail. The voltage on this depends on the voltage selected on J11. ■ Installing the shunt on pins 2-3 powers bank 4B when an FMC card is installed and provides the power needed for this bank. The max voltage on this is 3.3 V. Do not install an FMC with a higher rated card. Note: FMC is not available for rev. A boards.	Pins 1-2
J23	FAN1	Powers the fan for FPGA 1	Installed

For more information about the FPGA board settings, refer to the *Arria V GX FPGA Development Board Reference Manual*.

5. Board Update Portal

The Arria V GX FPGA Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the Load Selector (SW5.3) in the on (factory) position, the Arria V GX FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware 1 and hardware 2 portion of flash memory, and provides links to useful information on the Altera website, including kit-specific links and design resources.

After successfully updating the user hardware 1 and/or hardware 2 flash memory, you can load the user design from flash memory into the FPGA. To do so, set the Load Selector (SW5.3) to the off (user) position and power cycle the board. (The design stored in user hardware 1 is used to configure FPGA 1 when the board is power cycled.) To configure FPGA 1 with the design stored in user hardware 2, push and release the PGM1 (S2) push button the required number of times until PGM2 LED lights and then push PGM_CONF (S3) to configure the FPGA.

The source code for the Board Update Portal design resides in the <*install dir*>**\kits\arriaVGX_5agxfb3hf40es_fpga\examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page A–3 to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.

Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. With the board powered down, set the Load Selector (SW5.3) to the on (factory) position.
2. Attach the Ethernet cable from the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router, and obtains an IP address. The LCD on the board displays the IP address.

4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

   You can click *Arria V GX FPGA Development Kit* on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

You can also navigate directly to the Arria V GX FPGA Development Kit page to determine if you have the latest kit software.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user hardware 1 and user hardware 2 portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Design files available from the Arria V GX FPGA Development Kit page include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Preparing Design Files for Flash Programming" on page A–2 for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" to access the Board Update Portal web page.
2. In the **Hardware File Name** field specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field, otherwise leave the **Software File Name** field blank.
3. Click **Upload**. The progress bar indicates the percent complete. The file takes about 20 seconds to upload.
4. To configure the FPGA with the new design after the flash memory upload process is complete, set the Load Selector (SW5.3) to the off (user) position and power cycle the board (SW1).

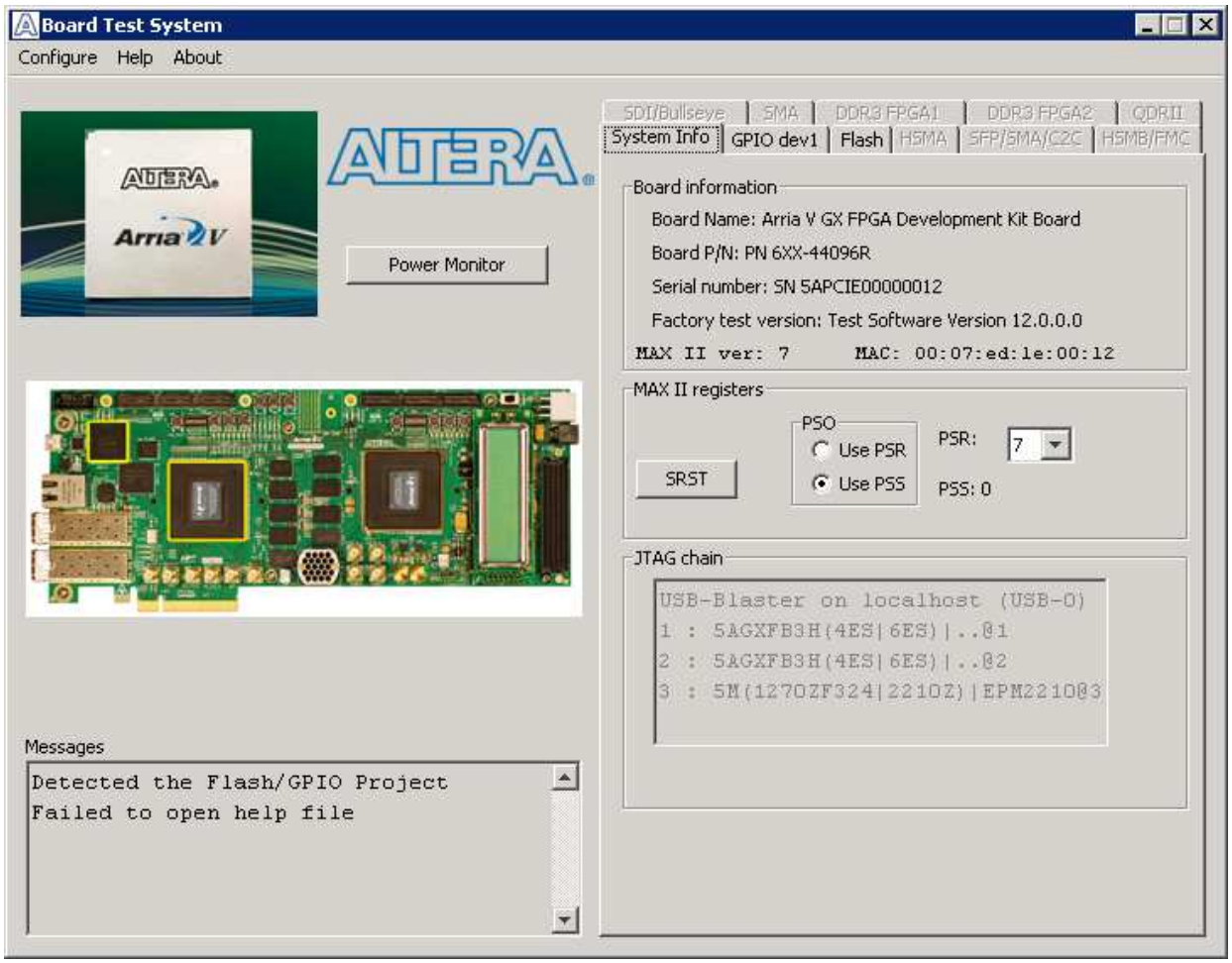
As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user hardware 1 and/or user hardware 2 portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "Restoring the Flash Device to the Factory Settings" on page A–3.

6. Board Test System

The kit includes a design example and an application called the Board Test System to test the functionality of the Arria V GX FPGA development board and supported daughtercards. The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the application to test board components, modify functional parameters, observe performance, and measure power usage. (While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.) The application is also useful as a reference for designing systems. To install the application, follow the steps in "Installing the Arria V GX FPGA Development Kit" on page 3–3.

The Board Test System GUI communicates over the JTAG bus to a test design running in the Arria V GX device. Figure 6–1 shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The **Power Monitor** button starts the Power Monitor application that measures and reports current power information for the board. Because the application communicates over the JTAG bus to the MAX II device, you can measure the power of any design in the FPGA, including your own designs.

To use the Power Monitor GUI, the MAX II device needs to be programmed with the default factory MAX II design.

The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board

With the power to the board off, follow these steps:

1. Connect the USB cable to the board.
2. Ensure that the Ethernet patch cord is plugged into the RJ45 connector.
3. Ensure that the development board switches and jumpers are set to the default positions as shown in the "Factory Default Switch and Jumper Settings" section starting on page 4–2.
4. Set the Load Selector (SW5.3) to the off (user) position.

   For more information about the board's DIP switch and jumper settings, refer to the *Arria V GX FPGA Development Board Reference Manual*.

5. Turn on the power to the board. The board loads the design stored in the user hardware 1 portion of flash memory into the FPGA. If your board is still in the factory configuration, or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design loads the GPIO, Ethernet, and flash memory tests.

   CAUTION

   To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the <*install dir*>**\kits\arriaVGX_5agxfb3hf40es_fpga\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

☞ On Windows, click **Start** > **All Programs** > **Altera** > **Arria V GX FPGA Development Kit** <*version*> > **Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The Arria V GX FPGA development board's flash memory ships preconfigured with the design that corresponds to the GPIO tab.

☞ If you power up your board with your own design programmed into the FPGA with the Quartus II Programmer, you receive a message prompting you to configure your board with a valid Board Test System design. Refer to "The Configure Menu" for information about configuring your board.

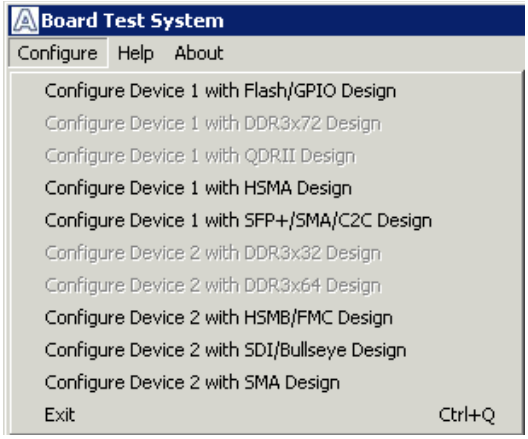
Using the Board Test System

This section describes each control in the Board Test System application.

The Configure Menu

Use the Configure menu (Figure 6–2) to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 6–2. The Configure Menu



To configure the FPGA with a test system design, perform the following steps:

1. Make sure there are no conflicts between the Quartus II software version and the Board Test System GUI version.