Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Cyclone V E FPGA Development Kit

User Guide

101 Innovation Drive
San Jose, CA 95134
www.altera.com

UG-01129-1.2

Feedback Subscribe

Contents

Chapter 1. About This Kit

Kit Features . . . 1–1
Hardware . . . 1–1
Software . . . 1–1
Quartus II Web Edition Software . . . 1–1
Cyclone V E FPGA Development Kit Installer . . . 1–2

Chapter 2. Getting Started

Before You Begin . . . 2–1
Inspect the Board . . . 2–1
References . . . 2–2

Chapter 3. Software Installation

Installing the Quartus II Web Edition Software . . . 3–1
Licensing Considerations . . . 3–1
Installing the Development Kit . . . 3–1
Installing the USB-Blaster II Driver . . . 3–2

Chapter 4. Development Board Setup

Setting Up the Board . . . 4–1
Factory Default Switch Settings . . . 4–2

Chapter 5. Board Update Portal

Connecting to the Board Update Portal Web Page . . . 5–1
Using the Board Update Portal to Update User Designs . . . 5–2

Chapter 6. Board Test System

Preparing the Board . . . 6–2
Running the Board Test System . . . 6–2
Using the Board Test System . . . 6–3
The System Info Tab . . . 6–3
Board Information . . . 6–3
MAX V Registers . . . 6–4
JTAG Chain . . . 6–4
Qsys Memory Map . . . 6–5
The GPIO Tab . . . 6–6
Character LCD . . . 6–6
User DIP Switches . . . 6–6
User LEDs . . . 6–7
Push Button Switches . . . 6–7
The Flash Tab . . . 6–7
Read . . . 6–8
Write . . . 6–8
Random Test . . . 6–8
CFI Query . . . 6–8
Increment Test . . . 6–8
Reset . . . 6–8
Erase . . . 6–8

Data Display/Entry Boxes 6–8
Flash Memory Map 6–8
The SSRAM Tab 6–9
Read 6–9
Write 6–9
Random Test 6–10
Increment Test 6–10
The Power Monitor 6–10
General Information 6–11
Power Information 6–11
Power Graph 6–11
Graph Settings 6–11
Reset 6–11
The Clock Control 6–12
Serial Port Registers 6–13
fXTAL 6–13
Target Frequency 6–13
Clear 6–13
Set New Frequency 6–13
Configuring the FPGA Using the Quartus II Programmer 6–13

Appendix A. Programming the Flash Memory Device

CFI Flash Memory Map A–1
Preparing Design Files for Flash Programming A–2
Creating Flash Files Using the Nios II EDS A–2
Programming Flash Memory Using the Board Update Portal A–2
Programming Flash Memory Using the Nios II EDS A–3
Restoring the Flash Device to the Factory Settings A–4
Restoring the MAX V CPLD to the Factory Settings A–5

Additional Information

Document Revision History Info–1
How to Contact Altera Info–1
Typographic Conventions Info–1

1. About This Kit

The Altera® Cyclone® V E FPGA Development Kit is a complete design environment that includes both the hardware and software you need to develop Cyclone V E FPGA designs.

Kit Features

This section briefly describes the Cyclone V E FPGA Development Kit contents.

For a complete list of this kit's contents and capabilities, refer to the Cyclone V E FPGA Development Kit page.

Hardware

The Cyclone V E FPGA Development Kit includes the following hardware:

- Cyclone V E FPGA development board—A development platform that allows you to develop and prototype hardware designs running on the Cyclone V E FPGA.

  For detailed information about the board components and interfaces, refer to the *Cyclone V E FPGA Development Board Reference Manual*.

- Debug Header Breakout Board HSMC.
- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom.
  - USB cable.
  - Ethernet cable.

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Web Edition Software

The Quartus II Web Edition Software is a licensed set of Altera tools with full functionality.

Download the Quartus II Web Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.

To compare the Quartus II subscription and web editions, refer to *Altera Quartus II Software — Subscription Edition vs. Web Edition*. The kit also works in conjunction with the subscription edition.

Cyclone V E FPGA Development Kit Installer

The license-free Cyclone V E FPGA Development Kit installer includes all the documentation and design examples for the kit.

For information on installing the Development Kit Installer, refer to "Installing the Development Kit" on page 3–1.

The remaining chapters in this user guide lead you through the following Cyclone V E FPGA development board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the FPGA development board
- Configuring the Cyclone V E FPGA
- Running the Board Test System designs

For complete information about the FPGA development board, refer to the *Cyclone V E FPGA Development Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in "Kit Features" on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Board

Perform these steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components on the board appears in place and intact.

In typical applications with the Cyclone V E FPGA development board, a heat sink is not necessary. However, under extreme conditions, the board might require additional cooling to stay within operating temperature guidelines. The board has two holes near the FPGA that accommodate many different heat sinks, including the Dynatron V31G. You can perform power consumption and thermal modeling to determine whether your application requires additional cooling. For information about measuring board and FPGA power in real time, refer to "The Power Monitor" on page 6–10.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the Cyclone V E FPGA Development Kit page.
- For additional daughter cards available for purchase, refer to the Development Board Daughtercards page.
- For the Cyclone V E device documentation, refer to the Documentation: Cyclone V Devices page.
- To purchase devices from the eStore, refer to the Devices page.
- For Cyclone V E OrCAD symbols, refer to the Capture CIS Symbols page.
- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

This chapter explains how to install the following software:

- Quartus II Web Edition Software
- Cyclone V E FPGA Development Kit software
- On-Board USB-Blaster™ II driver

Installing the Quartus II Web Edition Software

Perform these steps:

1. Run the Quartus II Web Edition Software installer you acquired in "Software" on page 1–1.
2. Follow the on-screen instructions to complete the installation process, choosing an installation directory that is relative to the Quartus II software installation directory.

For a list of the Web Edition capabilities and features, refer to the Detailed Comparison sheet.

If you have difficulty installing the Quartus II software, refer to the *Altera Software Installation and Licensing Manual*.

Licensing Considerations

The Quartus II Web Edition Software is license-free and supports Cyclone V E devices without any additional licensing requirement. This kit also works in conjunction with the Quartus II Subscription Edition Software, once you obtain the proper license file. To purchase a subscription, contact your Altera sales representative.

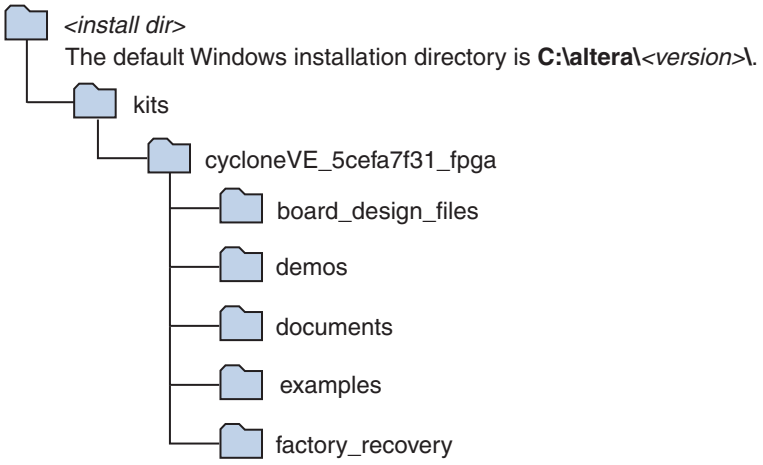
Installing the Development Kit

To install the development kit, perform these steps:

1. Download the Cyclone V E FPGA Development Kit installer from the Cyclone V E FPGA Development Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.
2. Run the Cyclone V E FPGA Development Kit installer and follow the directions. Choose an installation directory that is relative to the Quartus II software installation directory.

The installation program creates the directory structure shown in Figure 3–1.

Figure 3–1. Cyclone V E FPGA Development Kit Installed Directory Structure (1)



Note to Figure 3–1:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications, if available.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Cyclone V E FPGA Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster II Driver

The Cyclone V E FPGA development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the On-Board USB-Blaster II driver on the host computer.

Installation instructions for the On-Board USB-Blaster II driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

4. Development Board Setup

The instructions in this chapter explain how to set up the Cyclone V E FPGA development board.

Setting Up the Board

To prepare and apply power to the board, perform these steps:

1. The FPGA development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch Settings" on page 4–2 to return the board to its factory settings before proceeding.
2. The FPGA development board ships with design examples stored in the flash memory device. Verify the DIP switch SW4.3 is set to the OFF (1) position to load the design stored in the factory portion of flash memory.
3. Connect the 65 W, 15 VDC @ 4.3 A power supply to the DC Power Jack (J17) on the FPGA board and plug the cord into a power outlet.

   CAUTION: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage, and a lower-rated power supply may not be able to provide enough power for the board.

4. Set the POWER switch (SW5) to the on position. When power is supplied to the board, the blue LED (D35) illuminates indicating that the board has power.

The MAX V device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. The DIP switch SW4.3 controls which design to load. When the switch is in the OFF (1) position, the PFL loads the design from the factory portion of flash memory.

The kit includes a MAX V design which contains the MAX V PFL megafunction. The design resides in the <*install dir*>**\kits\cycloneVE_5cefa7f31_fpga\examples\max5** directory.

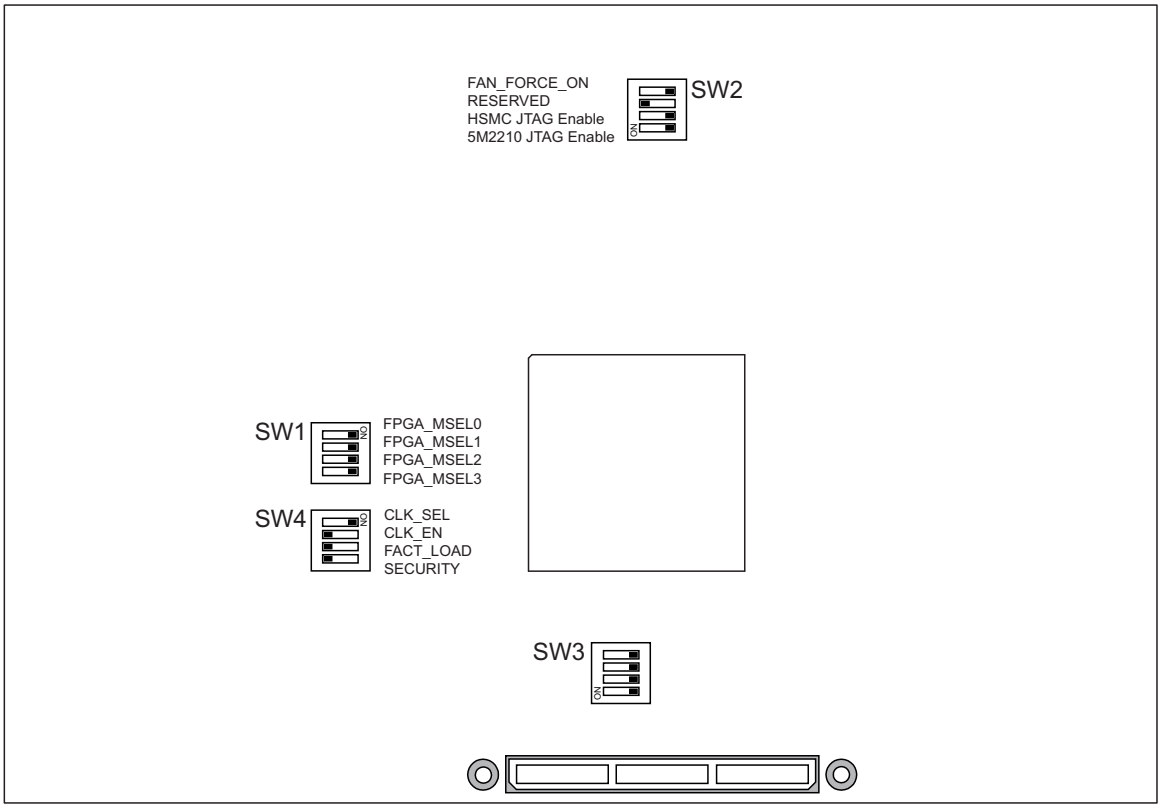
When configuration is complete, the Config Done LED (D19) illuminates, signaling that the Cyclone V E device configured successfully.

For more information about the PFL megafunction, refer to the *Parallel Flash Loader Megafunction User Guide*.

Factory Default Switch Settings

This section shows the factory switch settings (Figure 4–1) for the Cyclone V E FPGA development board.

Figure 4–1. Switch Locations and Default Settings



To restore the switches to their factory default settings, perform these steps:

1. Set the DIP switch bank (SW1) to match Table 4–1 and Figure 4–1.

Table 4–1. SW1 DIP Switch Settings

Switch	Board Label	Function	Default Position
1	FPGA_MSEL0	■ ON (0) = logic 0 is selected. ■ OFF (1) = logic 1 is selected.	ON
2	FPGA_MSEL1	■ ON (0) = logic 0 is selected. ■ OFF (1) = logic 1 is selected.	ON
3	FPGA_MSEL2	■ ON (0) = logic 0 is selected. ■ OFF (1) = logic 1 is selected.	ON
4	FPGA_MSEL3	■ ON (0) = logic 0 is selected. ■ OFF (1) = logic 1 is selected.	ON

2. Set the DIP switch bank (SW2) to match Table 4–2 and Figure 4–1.

Table 4–2. SW2 JTAG DIP Switch Settings

Switch	Board Label	Function	Default Position
1	FAN_FORCE_ON	■ ON (0) = Fan is turned on. (Fan not included.) ■ OFF (1) = Fan is turned off.	OFF
2	RESERVED	—	—
3	HSMA_JTAG_EN	■ ON (0) = Do not Include the HSMC port in the JTAG chain. ■ OFF (1) = Include the HSMC port in the JTAG chain.	ON
4	5M2210_JTAG_EN	■ ON (0) = Do not Include MAX V system controller in the JTAG chain. ■ OFF (1) = Include MAX V system controller in the JTAG chain	OFF

3. Set the DIP switch bank (SW4) to match Table 4–3 and Figure 4–1.

Table 4–3. SW4 DIP Switch Settings

Switch	Board Label	Function	Default Position
1	CLK_SEL	■ ON (0) = Select programmable oscillator clock. ■ OFF (1) = Select SMA input clock.	ON
2	CLK_EN	■ ON (0) = On-board oscillator is disabled. ■ OFF (1) = On-board oscillator is enabled.	OFF
3	FACT_LOAD	■ ON (0) = Load the user design from flash at power up. ■ OFF (1) = Load the factory design from flash at power up.	OFF
4	SECURITY	■ ON (0) = Embedded On-Board USB Blaster II sends FACTORY command at power up. ■ OFF (1) = Embedded On-Board USB Blaster II does not send FACTORY command at power up.	OFF

For more information about the FPGA board settings, refer to the *Cyclone V E FPGA Development Board Reference Manual*.

5. Board Update Portal

The Cyclone V E FPGA Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the DIP switch SW4.3 in the OFF (1) position, the Cyclone V E FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware 1 portion of flash memory and provides useful kit-specific links and design resources.

After successfully updating the user hardware 1 flash memory, you can load the user design from flash memory into the FPGA. To do so, set the DIP switch SW4.3 to the ON (0) position and power cycle the board.

The source code for the Board Update Portal design resides in the <*install dir*>**\kits\cycloneVE_5cefa7f31_fpga\examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page A–4 to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page

Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port (J8) on a DHCP enabled network.
- A separate working Ethernet port (J8) connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. With the board powered down, set the DIP switch SW4.3 to the OFF (1) position.
2. Attach the Ethernet cable from the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router and obtains an IP address. The LCD on the board displays the IP address.
4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

   You can click *Cyclone V E FPGA Development Kit* on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user hardware 1 portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Design files available from the Cyclone V E FPGA Development Kit page include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Preparing Design Files for Flash Programming" on page A–2 for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform these steps:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" to access the Board Update Portal web page.
2. In the **Hardware File Name** field, specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field; otherwise, leave the **Software File Name** field blank.
3. Click **Upload**. The progress bar indicates the percent complete.
4. To configure the FPGA with the new design after the flash memory upload process is complete, set the DIP switch SW4.3 to the ON (0) position and power cycle the board.

As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user hardware 1 portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "Restoring the Flash Device to the Factory Settings" on page A–4.

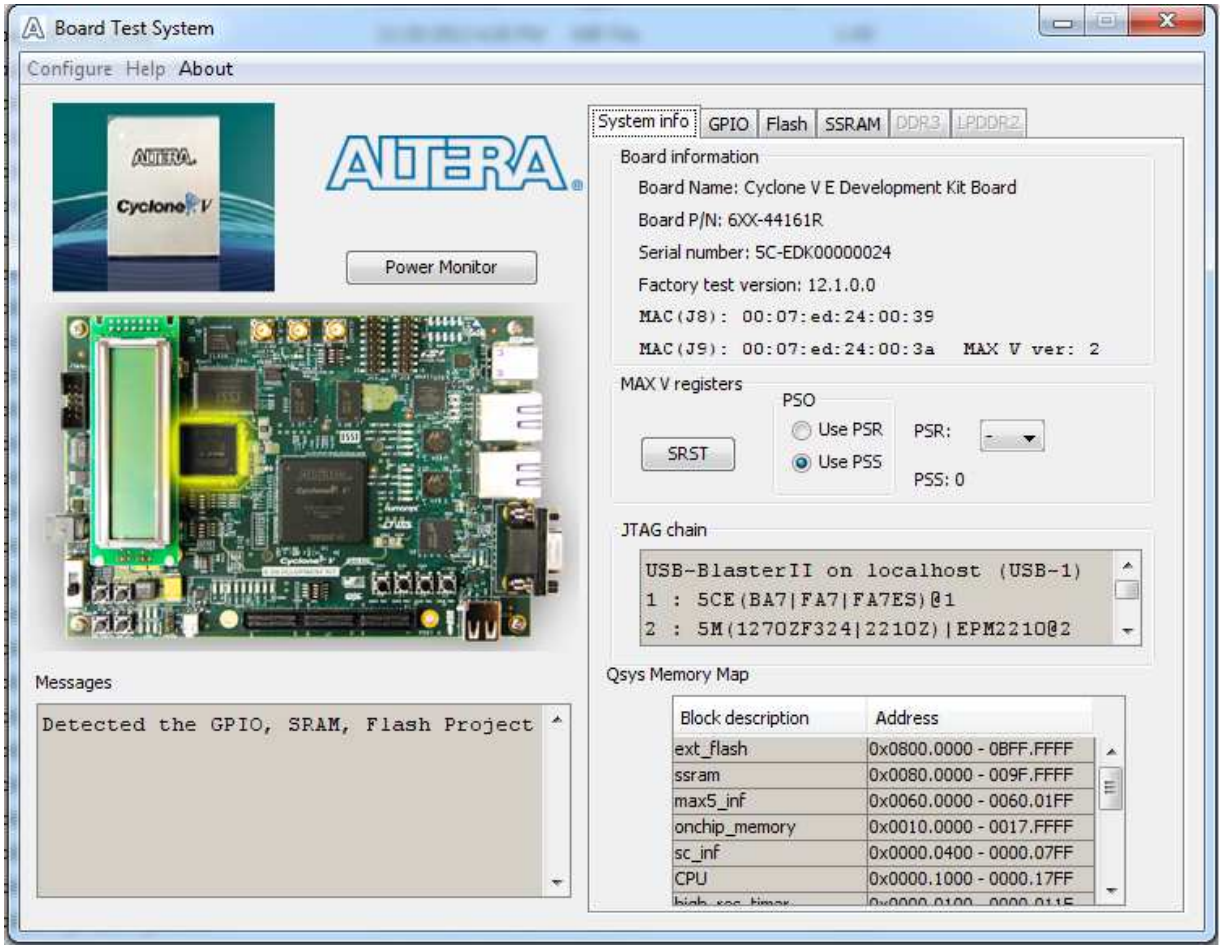
6. Board Test System

The kit includes an application called the Board Test System (BTS). The BTS provides an easy-to-use interface to alter functional settings and observe the results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage. While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality you are testing. (You can also use the BTS as a reference source for designing systems.)

To install the BTS, follow the steps in "Installing the Development Kit" on page 3–1.

The Board Test System GUI communicates over the JTAG bus to a test design running in the Cyclone V E device. Figure 6–1 shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The **Power Monitor** button starts the Power Monitor application that measures and reports current power information for the board. Because the application communicates over the JTAG bus to the MAX V device, you can measure the power of any design in the FPGA, including your own designs.

The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board

With the power to the board off, follow these steps:

1. Connect the USB cable to the board.
2. Ensure that the Ethernet patch cord is plugged into the RJ45 connector (J8).
3. Ensure that the development board switches and jumpers are set to the default positions as shown in the "Factory Default Switch Settings" section starting on page 4–2.
4. Set the DIP switch SW4.3 to the ON (0) position.

   For more information about the board's DIP switch and jumper settings, refer to the *Cyclone V E FPGA Development Board Reference Manual*.

5. Turn on the power to the board. The board loads the design stored in the user hardware 1 portion of flash memory into the FPGA. If your board is still in the factory configuration, or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design loads the GPIO, SRAM, and flash memory tests.

   CAUTION: To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the <*install dir*>**\kits\cycloneVE_5cefa7f31_fpga\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

On Windows, click **Start** > **All Programs** > **Altera** > **Cyclone V E FPGA Development Kit** <*version*> > **Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The Cyclone V E FPGA development board's flash memory ships preconfigured with the design that corresponds to the GPIO, Flash and SSRAM tabs.

☞ If you power up your board with the DIP switch SW4.3 in a position other than the ON (0) position, or if you load your own design into the FPGA with the Quartus II Programmer, you receive a message prompting you to configure your board with a valid Board Test System design.

Using the Board Test System

This section describes each control in the Board Test System application.

The System Info Tab

The **System Info** tab shows board's current configuration. Figure 6–1 on page 6–1 shows the **System Info** tab. The tab displays the contents of the MAX V registers, the JTAG chain, the board's MAC addresses, the flash memory map, and other details stored on the board.

The following sections describe the controls on the **System Info** tab.

Board Information

The **Board information** controls display static information about your board.

- **Board Name**—Indicates the official name of the board.
- **Part P/N**—Indicates the part number of the board.
- **Serial number**—Indicates the serial number of the board.
- **Factory test version**—Indicates the version of the Board Test System currently running on the board.
- **MAC (J8)**—Indicates the MAC addresses for Ethernet port (J8).
- **MAC (J9)**—Indicates the MAC addresses for Ethernet port (J9).
- **MAX V ver**—Indicates the version of MAX V code currently running on the board. The MAX V code resides in the *<install dir>***kits\cycloneVE_5cefa7f31_fpga\examples** directory. Newer revisions of this code might be available on the Cyclone V E FPGA Development Kit page of the Altera website.

MAX V Registers

The **MAX V registers** control allows you to view and change the current MAX V register values as described in Table 6–1. Changes to the register values with the GUI take effect immediately. For example, writing a 0 to SRST resets the board.

Table 6–1. MAX V Registers

Register Name	Read/Write Capability	Description
System Reset (SRST)	Write only	Set to 0 to initiate an FPGA reconfiguration.
Page Select Register (PSR)	Read / Write	Determines which of the up to three (0-2) pages of flash memory to use for FPGA reconfiguration. The flash memory ships with pages 0 and 1 preconfigured.
Page Select Override (PSO)	Read / Write	When set to 0, the value in PSR determines the page of flash memory to use for FPGA reconfiguration. When set to 1, the value in PSS determines the page of flash memory to use for FPGA reconfiguration.
Page Select Switch (PSS)	Read only	Holds the current value of the illuminated PGM LED (D25-D27) based on the following encoding: ■ 0 = PGM LED (D25) and corresponds to the flash memory page for the factory hardware design ■ 1 = PGM LED (D26) and corresponds to the flash memory page for the user hardware 1 design ■ 2 = PGM LED (D27) and corresponds to the flash memory page for the user hardware 2 design

- **PSO**—Sets the MAX V PSO register. The following options are available:
  - **Use PSR**—Allows the PSR to determine the page of flash memory to use for FPGA reconfiguration.
  - **Use PSS**—Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.
- **PSR**—Sets the MAX V PSR register. The numerical values in the list corresponds to the page of flash memory to load during FPGA reconfiguration. Refer to Table 6–1 for more information.
- **PSS**—Displays the MAX V PSS register value. Refer to Table 6–1 for the list of available options.
- **SRST**—Resets the system and reloads the FPGA with a design from flash memory based on the other MAX V register values. Refer to Table 6–1 for more information.

Because the **System Info** tab requires that a specific design is running in the FPGA at a specific clock speed, writing a 0 to SRST or changing the PSO value can cause the Board Test System to stop running.

JTAG Chain

The **JTAG chain** control shows all the devices currently in the JTAG chain. The Cyclone V E device is always the first device in the chain. The JTAG chain is normally mastered by the On-board USB-Blaster II.

If you plug in an external USB-Blaster cable to the JTAG header (J4), the On-Board USB-Blaster II is disabled.

JTAG DIP switch bank (SW2) selects which interfaces are in the chain. Refer to Table 4–2 on page 4–3 for detailed settings.

For details on the JTAG chain, refer to the *Cyclone V E FPGA Development Board Reference Manual.* For USB-Blaster II configuration details, refer to the On-Board USB-Blaster II page.

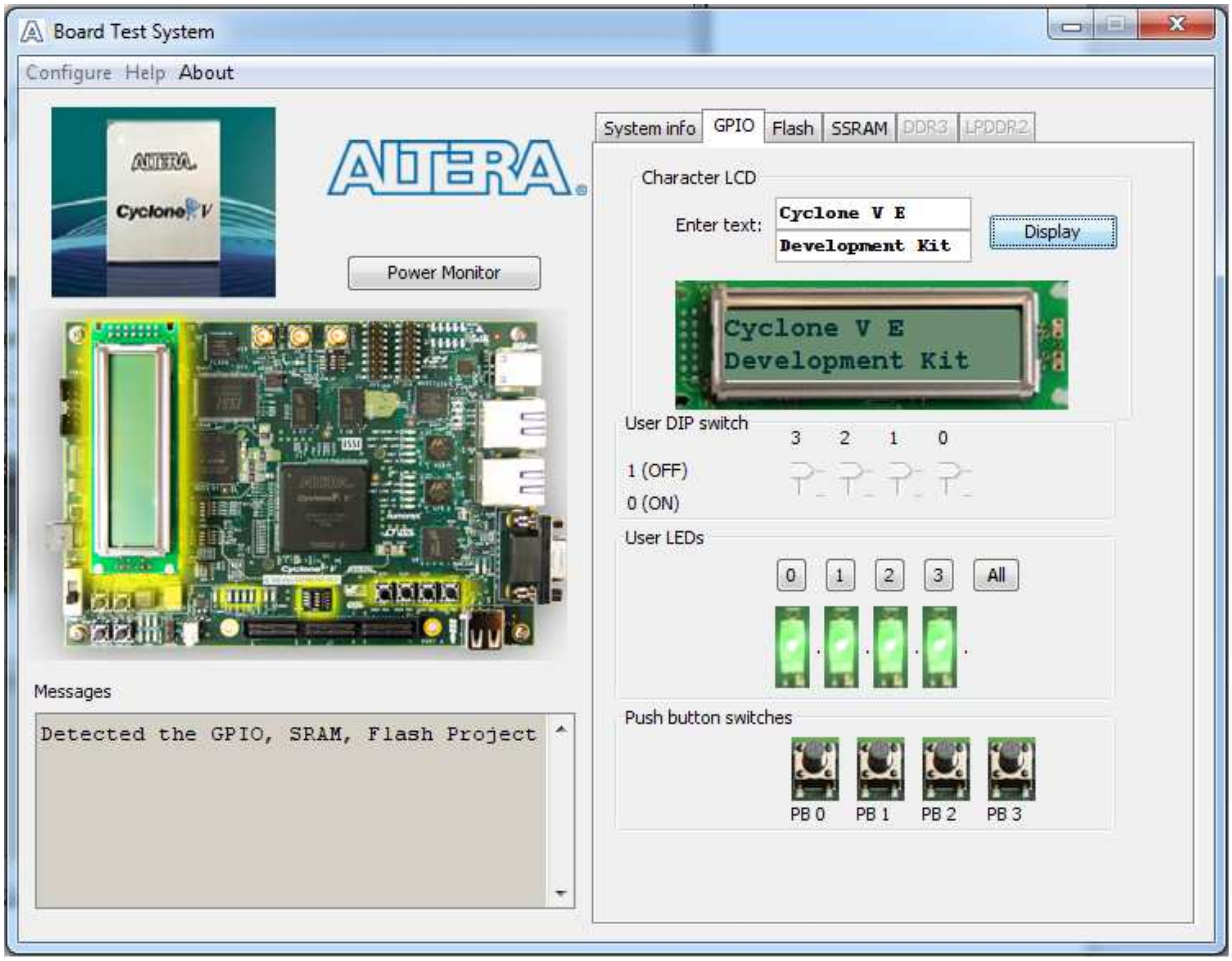
Qsys Memory Map

The **Qsys memory map** control shows the memory map of the Qsys system on your board.

The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. You can write to the character LCD, read DIP switch settings, turn LEDs on or off, and detect push button presses. Figure 6–2 shows the **GPIO** tab.

Figure 6–2. The GPIO Tab



The following sections describe the controls on the **GPIO** tab.

Character LCD

The **Character LCD** controls allow you to display text strings on the character LCD on your board. Type text in the text boxes and then click **Display**.

If you exceed the 16 character display limit on either line, a warning message appears.

User DIP Switches

The read-only **User DIP switches** control displays the current positions of the switches in the user DIP switch bank. Change the switches on the board to see the graphical display change accordingly.

User LEDs

The **User LEDs** control displays the current state of the user LEDs. Click the graphical representation of the LEDs to turn the board LEDs on and off. You can click **ALL** to turn on and off all of the user LEDs at once.

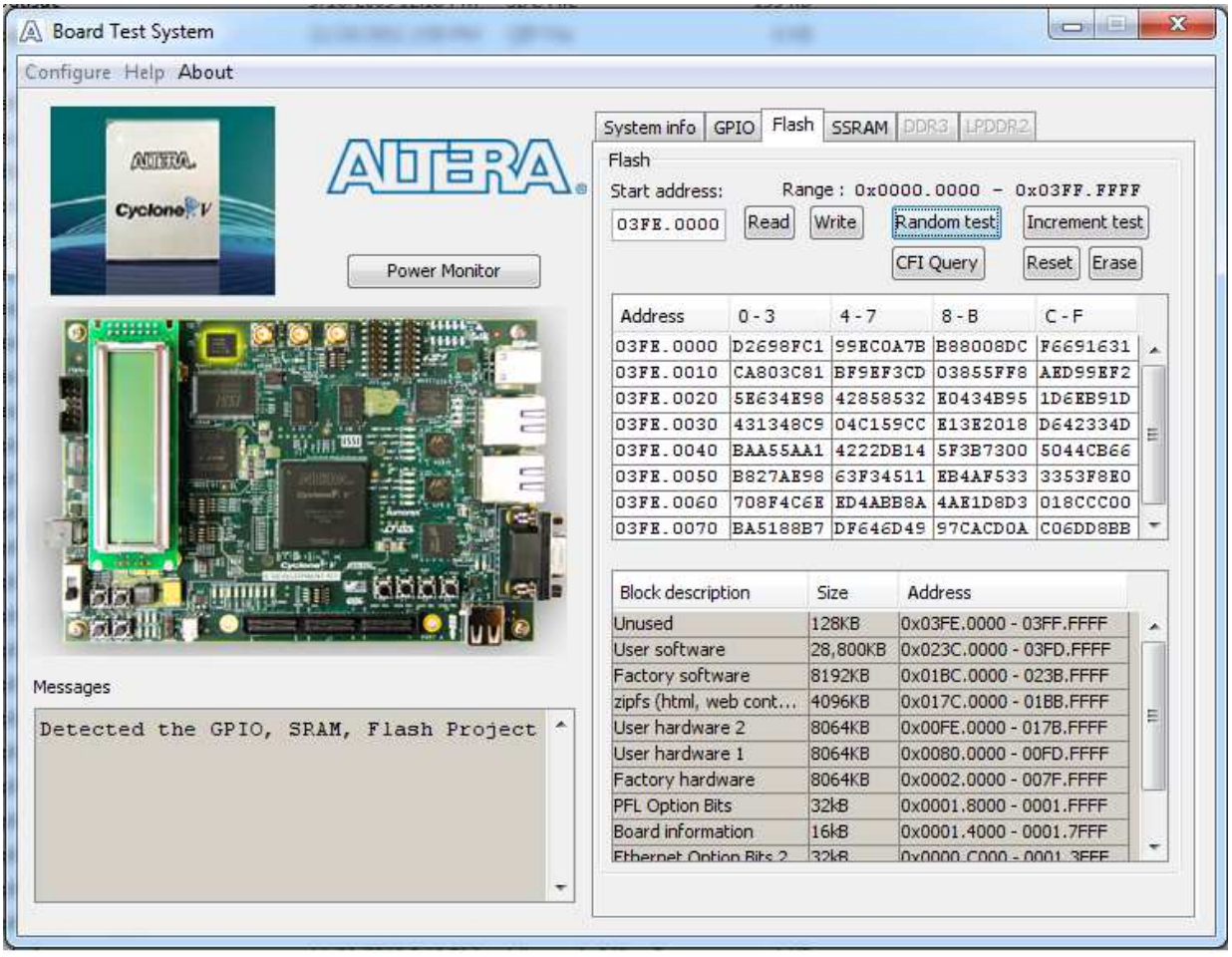
Push Button Switches

The read-only **Push Button switches** control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

The Flash Tab

The **Flash** tab allows you to read and write flash memory on your board. Figure 6–3 shows the **Flash** tab.

Figure 6–3. The Flash Tab



The following sections describe the controls on the **Flash** tab.

Read

The **Read** control reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table.

If you enter an address outside of the flash memory address space, a warning message identifies the valid flash memory address range.

Write

The **Write** control writes the flash memory on your board. To update the flash memory contents, change values in the table and click **Write**. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.

Random Test

Starts a random data pattern test to flash memory, which is limited to a scratch page in the upper 128K block.

CFI Query

The **CFI Query** control updates the memory table, displaying the CFI ROM table contents from the flash device.

Increment Test

Starts an incrementing data pattern test to flash memory, which is limited to a scratch page in the upper 128K block.

Reset

The **Reset** control executes the flash device's reset command and updates the memory table displayed on the **Flash** tab.

Erase

Erases flash memory, which is limited to a scratch page in the upper 128K block.

Data Display/Entry Boxes

There are 8 rows and 4 columns. Each column contain 8 hexadecimal numbers. After entering the numbers in each cell, press Enter on your keyboard. Then click **Write** and **Read** button.

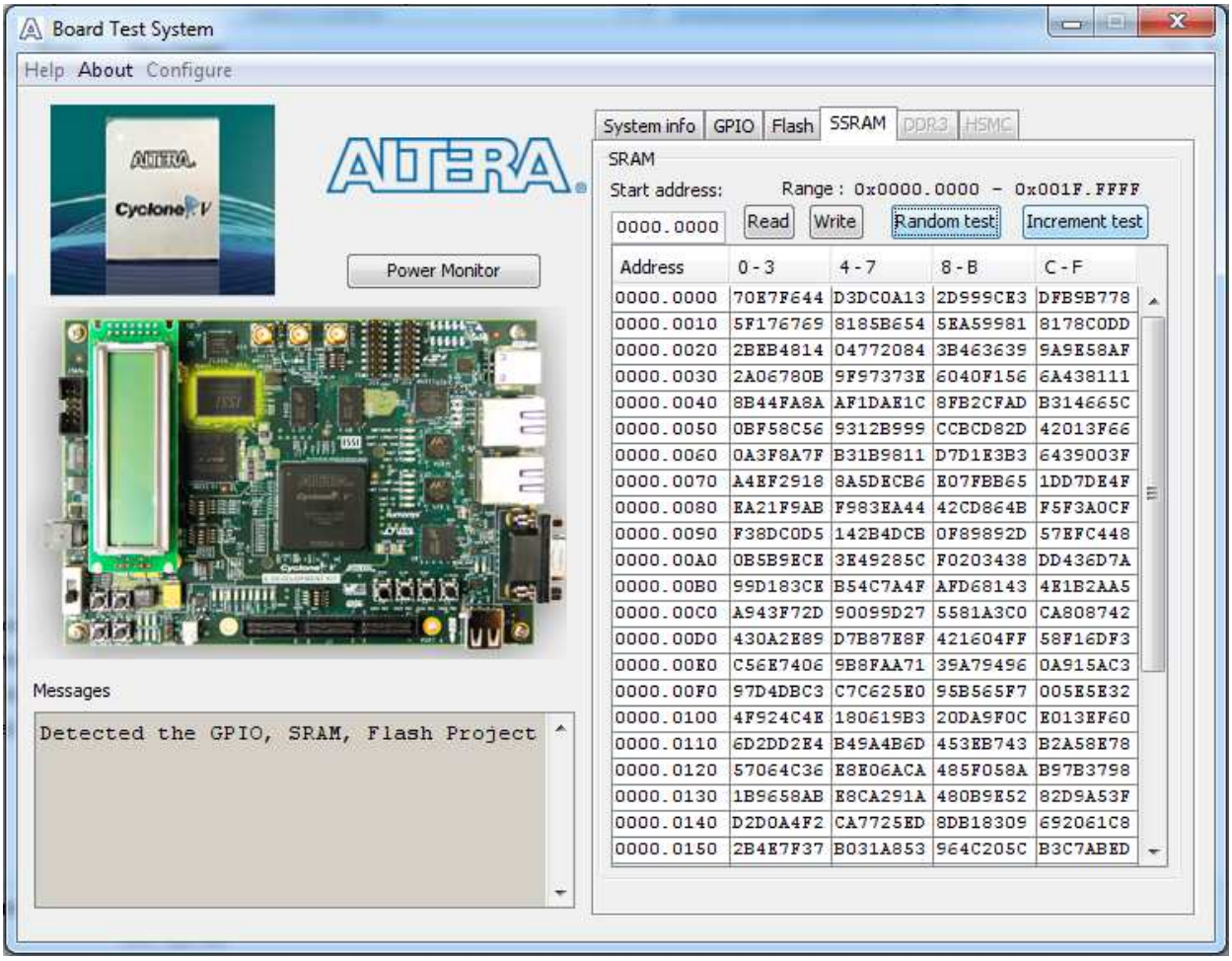
Flash Memory Map

Displays the flash memory map for the Cyclone V E FPGA Development Kit.

The SSRAM Tab

The **SSRAM** tab allows you to read and write SRAM and flash memory on your board. Figure 6–4 shows the **SSRAM** tab.

Figure 6–4. The SSRAM Tab



The following sections describe the controls on the **SSRAM** tab.

Read

The **Read** control reads the SRAM on your board. To see the SRAM contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table.

Write

The **Write** control writes the SRAM on your board. To update the SRAM contents, change values in the table and click **Write**. The application writes the new values to SRAM and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.