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Cyclone V SoC Development Kit

User Guide

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UG-01135-1.2

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Contents

Appendix A. Programming Flash Memory

Additional Information

1. About This Kit

The Altera® Cyclone® V system on a chip (SoC) Development Kit is a complete design environment that includes both the hardware and software you need to develop Cyclone V SoC designs.

Kit Features

This section briefly describes the kit contents.

For a complete list of this kit's contents and capabilities, refer to the Cyclone V SoC Development Kit page.

The Cyclone V SoC Development Kit includes the following hardware:

- Cyclone V development board—A development platform that allows you to develop and prototype hardware designs running on the Cyclone V SoC.

  For detailed information about the board components and interfaces, refer to the *Cyclone V SoC Development Board Reference Manual*.

- microSD flash memory card.
- Debug header breakout board high-speed mezzanine card (HSMC).
- Loopback daughtercard HSMC.
- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom.
  - USB cable.
  - Ethernet cable.
  - SMB cable.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the boards to verify that you received all of the items listed in *Quick Start Guide* printout in the box. If any of the items are missing, contact Altera before you proceed.

Inspect the Boards

To inspect each board, perform these steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components on the boards appear in place and intact.

In typical applications with the Cyclone V development board, a heat sink is not necessary. However, under extreme conditions or for engineering sample silicon, the board might require additional cooling to stay within operating temperature guidelines. The board has two holes near the FPGA that accommodate many different heat sinks, including the Dynatron V31G. You can perform power consumption and thermal modeling to determine whether your application requires additional cooling. For information about measuring board and FPGA power in real time, refer to "The Power Monitor" on page 5–15.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

References

Use the following links in Table 1–1 to check the Altera website for other related information:

Table 1–1. Related Links and Documents

Altera Website Link	Information
Cyclone V SoC Development Kit page	Latest board design files, reference designs, kit installation for Windows and Linux.
RocketBoards.org	Open-source community website supporting SoC development including Altera and Partner SoC development kit targets and related designs and documentation.
ARM Cortex-A (SoC)	On the dual-core ARM Cortex-A9 MPCore processor.
Getting Started for Software Developers	Developing software for the Cyclone V SoC.
Cyclone V SoC Development Kit Hardware Developer Resource Center	Developing SoC Hardware designs on the development kit.
Altera SoC Embedded Design Suite User Guide	Installing the SoC EDS and ARM DS-5. Preloader user guide. Hard Processor System (HPS) Flash programmer. Bare Metal and Linux Compiler. Yocto plugin. Debugging.
GSRD User Manual page	The Golden System Reference Design (GSRD) demonstrates the HPS features and the ability to communicate between HPS to the FPGA logic via the AXI Bridge interfaces.
Cyclone V SoC Development Board Reference Manual	Complete information about the development board.
Development Board Daughtercards	Additional daughter cards available for purchase.
Documentation: Cyclone V Devices	Cyclone V device documentation.
Devices	Purchase devices from the eStore.
Capture CIS Symbols	Cyclone V OrCAD symbols.
Embedded Processing	Nios II 32-bit embedded processor solutions.

2. Software Installation

This chapter explains how to install the following software:

- Quartus II Web Edition Software (optional)
- Altera SoC Embedded Development Suite (EDS)
- Cyclone V SoC Development Kit software
- On-Board USB-Blaster™ II driver

If you do not need to develop FPGA designs, you do not need to download the Quartus II software. For example, when you only want to write software for the SoC HPS. Installing the SoC EDS software, along with USB-II Blaster drivers, can provide your development kit JTAG programming environment.

Installing the Quartus II Web Edition Software

Perform these steps:

1. Download the Quartus II Web Edition Software from the Quartus II Subscription Edition Software page of the Altera website.

   Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.
2. Run the Quartus II Web Edition Software installer.
3. Follow the on-screen instructions to complete the installation process.

For a list of the Web Edition capabilities and features, refer to the Detailed Comparison sheet.

If you have difficulty installing the Quartus II software, refer to the *Altera Software Installation and Licensing Manual*.

Licensing Considerations

The Quartus II Web Edition Software is license-free and supports Cyclone V devices without any additional licensing requirement. This kit also works in conjunction with the Quartus II Subscription Edition Software, once you obtain the proper license file. To purchase a subscription, contact your Altera sales representative.

Installing the Altera SoC EDS

The Altera SoC EDS is a comprehensive tool suite for embedded software development on Altera SoC devices. The Altera SoC EDS contains the following:

- Development tools
- Utility programs
- Run-time software

- Application examples that enable firmware and application software development

The SoC EDS includes an exclusive offering of the ARM Development Studio™ 5 (DS-5™) Altera Edition Toolkit. The ARM DS-5 combines advanced multicore debugging capabilities with FPGA adaptivity. With Altera's SignalTap™ II Logic Analyzer, embedded software developers have full-chip visibility and control.

For the steps to install the SoC EDS Design Suite, refer to the *Altera SoC Embedded Design Suite User Guide*.

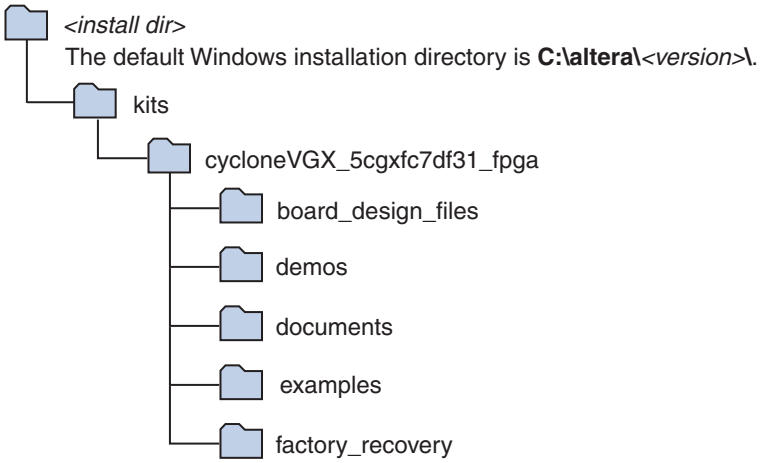
Installing the Development Kit

Perform these steps:

1. Download the Cyclone V SoC Development Kit installer from the Cyclone V SoC Development Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.
2. Start the Cyclone V SoC Development Kit installer.
3. Choose an installation directory that is relative to the Quartus II software installation directory. Follow the on-screen instructions to complete the installation process.
4. For the latest issues and release notes, Altera recommends that you review the **readme.txt** located in the root directory of the kit installation.

The installation program creates the Cyclone V SoC Development Kit directory structure shown in Figure 2–1.

Figure 2–1. Cyclone V SoC Development Kit Installed Directory Structure *(1)*



Note to Figure 2–1:

(1) Early-release versions might have slightly different directory names.

Table 2–1 lists the file directory names and a description of their contents.

Table 2–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications, if available.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Cyclone V SoC Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster II Driver

The Cyclone V development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the On-Board USB-Blaster II driver on the host computer.

Installation instructions for the On-Board USB-Blaster II driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

For USB-Blaster II configuration details, refer to the On-Board USB-Blaster II page.

3. Development Board Setup

This chapter explains how to set up the Cyclone V SoC development board and restore default settings.

Setting Up the Board

To prepare the board, perform these steps:

1. The development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch and Jumper Settings" on page 3–1 to return the board to its factory settings before proceeding.

   The development board ships with the Golden System Reference Design binaries stored in the microSD card.

   The microSD card also includes the following:

   - Hardware reference design FPGA image, Raw Binary File (**.rbf**) file
   - HPS image preloader U-Boot and Linux images
   - File system and software examples

2. Power up the development board by using the included laptop power supply plugged into J22 on the board.

   CAUTION: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage, and a lower-rated power supply may not be able to provide enough power for the board.

   Alternatively, you can use the an ATX power from a PC by plugging a 4-pin output from that supply to J20 on the development board.

   CAUTION: Make sure that the ATX supply is off when connecting to the board. Hot-swap is not supported and may damage the board's power supplies and other downstream devices.

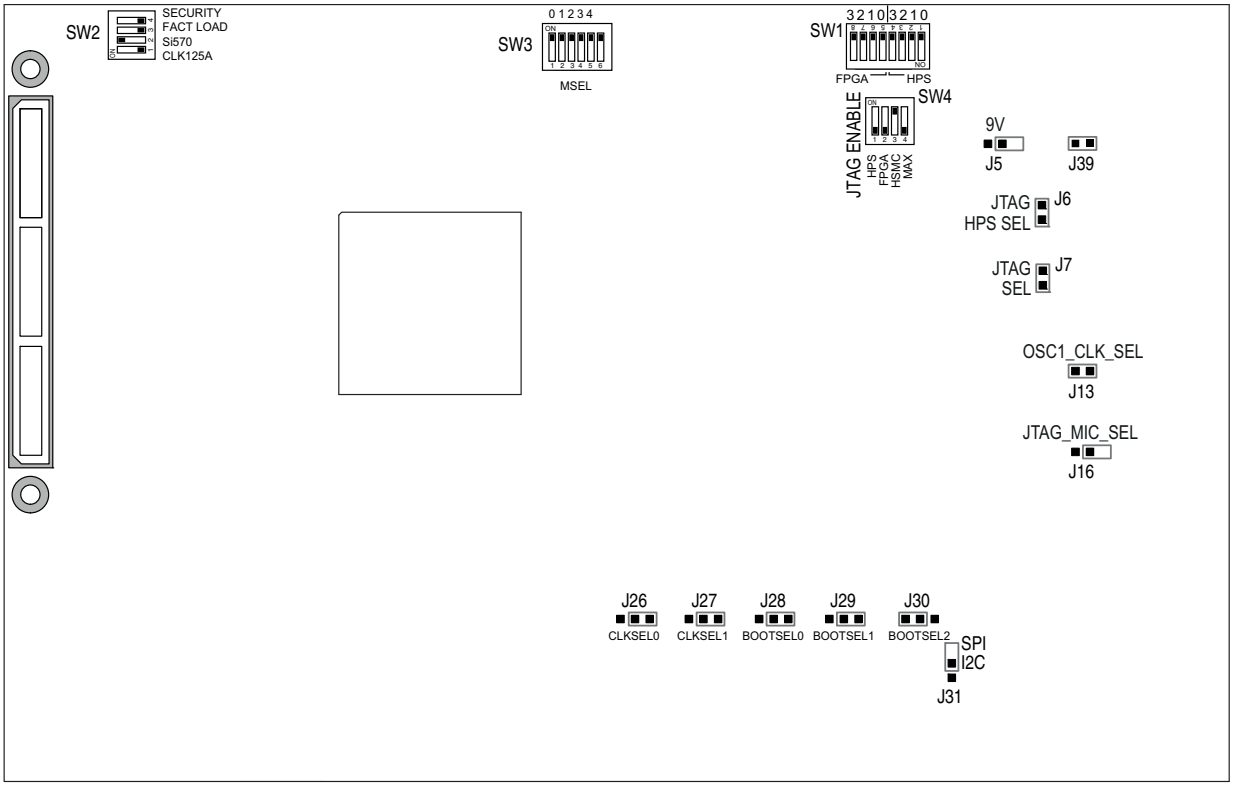
When configuration is complete, the Config Done LED (D38) illuminates, signaling that the Cyclone V device configured successfully.

Factory Default Switch and Jumper Settings

This section shows the factory settings (Figure 3–1) for the Cyclone V SoC development board. These settings ensure that the Board Update Portal and Golden System Reference design function properly.

The SD card, Max V system controller, and common flash interface (CFI) flash are already programmed with the factory default files. For more information, refer to Appendix A, Programming Flash Memory.

Figure 3–1. Switch Locations and Default Settings



To restore the switches to their factory default settings, perform these steps:

1. Set the DIP switch bank (SW2) to match Table 3–1 and Figure 3–1.

   In the following table, *ON* indicates the switch is to the left according to the board orientation as shown in Figure 3–1.

Table 3–1. SW2 DIP Switch Settings (Part 1 of 2)

Switch	Board Label	Function	Default Position
1	CLK125A	Switch 1 has the following options: ■ ON (0) = On-board oscillator is disabled. ■ OFF (1) = On-board oscillator is enabled.	OFF
2	Si570	Switch 2 has the following options: ■ ON (0) = On-board programmable oscillator is enabled. ■ OFF (1) = On-board programmable oscillator is disabled.	ON

Table 3–1. SW2 DIP Switch Settings (Part 2 of 2)

Switch	Board Label	Function	Default Position
3	FACT LOAD	Switch 3 has the following options: ■ ON (0) = Load the factory design starting at 0x20000 at power up. ■ OFF (1) = Parallel flash loader (PFL) disabled.	OFF
4	Security	Switch 4 has the following options: ■ ON (0) = On-Board USB Blaster II sends FACTORY command at power up ■ OFF (1) = On-Board USB Blaster II does not send FACTORY command at power up	OFF

2. Set the DIP switch bank (SW3) to match Table 3–2 and Figure 3–1.

   In the following table, *up* and *down* indicates the position of the switch with the board orientation as shown in Figure 3–1.

   Important: The default MSEL pin settings are set to all zeroes (ON) to select the fast passive parallel x16 mode. For power-up configuration from MAX V and CFI flash, ensure that the MAX V design uses this same mode as does in the design in the *<install dir>***kits\cycloneVSX_5csxfc6df31_soc\examples\max5** directory.

Table 3–2. SW3 DIP Switch Settings

Switch	Board Label	Function	Default Position
1	MSEL0	Switch 1 has the following options: ■ ON (up) = MSEL0 is 0. ■ OFF (down) = MSEL0 is 1.	ON
2	MSEL1	Switch 2 has the following options: ■ ON (up) = MSEL1 is 0. ■ OFF (down) = MSEL1 is 1.	ON
3	MSEL2	Switch 3 has the following options: ■ ON (up) = MSEL2 is 0. ■ OFF (down) = MSEL2 is 1.	ON
4	MSEL3	Switch 4 has the following options: ■ ON (up) = MSEL3 is 0. ■ OFF (down) = MSEL3 is 1.	ON
5	MSEL4	Switch 5 has the following options: ■ ON (up) = MSEL4 is 0. ■ OFF (down) = MSEL4 is 1.	ON

3. Set the DIP switch bank (SW4) to match Table 3–3 and Figure 3–1.

   In the following table, *up* and *down* indicates the position of the switch with the board orientation as shown in Figure 3–1.

Table 3–3. SW4 JTAG DIP Switch Settings

Switch	Board Label	Function	Default Position
1	HPS	■ ON (up) = Do not Include HPS in the JTAG chain. ■ OFF (down) = Include HPS in the JTAG chain	OFF
2	FPGA	■ ON (up) = Do not Include the FPGA in the JTAG chain. ■ OFF (down) = Include the FPGA in the JTAG chain.	OFF
3	HSMC	■ ON (up) = Do not include the HSMC connector in the JTAG chain. ■ OFF (down) = Include the HSMC connector in the JTAG chain.	ON
4	MAX	■ ON (up) = Do not include the MAX V system controller in the JTAG chain. ■ OFF (down) = Include the MAX V system controller in the JTAG chain.	OFF

4. Set the following jumper blocks to match Table 3–4 and Figure 3–1.

Table 3–4. Default Jumper Settings

Board Reference	Board Label	Description	Default Position
J5	9V	■ SHORT: Powers the CFI flash memory device using a 9 V supply for fast write in manufacturing. ■ OPEN: Powers CFI flash memory from the default 3 V supply.	OPEN
J6	JTAG HPS SEL	■ SHORT: Controls the HPS from On-Board USB Blaster II JTAG master. ■ OPEN: Controls the HPS from MICTOR-based JTAG master, such as DSTREAM or Lauterbach programming cables. Also, set SW4.1 to ON to remove the On-Board USB Blaster II from driving the HPS JTAG input port in this mode.	SHORT
J7	JTAG SEL	■ SHORT: The USB Blaster II is the source of the JTAG chain. ■ OPEN: The Mictor is the source of the JTAG chain.	SHORT
J13	OSC1_CLK_SEL	■ SHORT: Selects the on board 25MHz clock. ■ OPEN: Selects SMA.	SHORT

Table 3–4. Default Jumper Settings (Continued)

Board Reference	Board Label	Description	Default Position
J16	JTAG MIC SEL	■ SHORT: JTAG TRST input to HPS driven from the JTAG chain. ■ OPEN: JTAG TRST input to HPS driven from the MICTOR.	OPEN
J26	CLKSEL0	Selects the HPS clock settings.(1)	SHORT pins 2-3
J27	CLKSEL1	Selects the HPS clock settings.(1)	SHORT pins 2-3
J28	BOOTSEL0	Selects the boot mode and source for the HPS.(1)	SHORT pins 1-2
J29	BOOTSEL1	Selects the boot mode and source for the HPS.(1)	SHORT pins 2-3
J30	BOOTSEL2	Selects the boot mode and source for the HPS.(1)	SHORT pins 1-2
J31	SPI I2C	■ SHORT: Select SPI bus access from HPS to Linear Tech daughter card interface through J32. ■ OPEN: Select I^2C bus access from HPS to Linear Tech daughter card interface through J32.(2)	OPEN
J39	—	■ SHORT: External Mictor 38-pin connector's pin 14 is powered by 3.3V rail. ■ OPEN: External Mictor 38-pin connector's pin 14 is floating.	SHORT

Note to Table 3–4:

(1) For more information, refer to the Cyclone V Device Handbook.

(2) This connection can be software controlled from the HPS GPIO pin F16 on rev D and later boards.

For more information about the FPGA board settings, refer to the *Cyclone V SoC Development Board Reference Manual*.

Restoring the MAX V CPLD to the Factory Settings

This section describes how to restore the original factory contents to the MAX V CPLD on the development board. Make sure you have the Quartus II software installed, and then perform these steps:

1. Set the board switches to the factory default settings described in "Factory Default Switch and Jumper Settings" on page 3–1.

   DIP switch SW4.4 includes the MAX V device in the JTAG chain.

2. Launch the Quartus II Programmer.
3. Click **Auto Detect**.
4. Click **Add File** and select <*install dir*>**\kits\cycloneVSX_5csxfc6df31_soc\factory_recovery\max**<*no_ver*>**.pof**.

5. Turn on the **Program/Configure** option for the added file.
6. Click **Start** to download the selected configuration file to the MAX V CPLD. Configuration is complete when the progress bar reaches 100%.

To ensure that you have the most up-to-date factory restore files and product information, refer to the Cyclone V SoC Development Kit page of the Altera website.

Restoring the CFI Flash Device to the Factory Defaults

To program the factory image to the flash device in the Quartus II Programmer, do the following steps:

1. On the **Tools** menu in the Quartus II software, click **Programmer**.
2. In the Programmer window, click **Auto-Detect**.

   If you do not see USB Blaster or the board's embedded USB Blaster II listed next to **Hardware Setup**, refer to the "Installing the USB-Blaster II Driver" on page 2–3.

3. Click **Add File** and open <*install dir*>**\kits\cycloneVSX_5csxfc6df31_soc\factory_recovery\max2_PFL_writer.pof.**
4. Turn on the **Program/Configure** option for the **.pof** file.
5. Click **Start** to download the selected configuration file to the MAX V CPLD. Configuration is complete when the progress bar reaches 100%
6. Click **Auto Detect** and a flash device should show up attached to the MAX V in the main window.
7. Double-click the graphic of the flash device in the device chain pane to display the **Device's Properties** dialog box.
8. Select the flash image **.pof** file: <*install dir*>**\kits\cycloneVSX_5csxfc6df31_soc\factory_recovery\output_file.pof**.
9. Once the flash image **.pof** is attached in the Quartus II Programmer, turn on **Page_1** and **Option Bits**. (**Page_0** is reserved for the GSRD factory design.)
10. Click **Start**.
11. After the flash writing process has completed, power cycle the board and look for the MAX CONF DONE LED to turn ON if successful.
12. Altera recommends that you return to the Max V System Controller factory design after completing the flash writing. To do so, program the Max V with <*install dir*>**\kits\cycloneVSX_5csxfc6df31_soc\factory_recovery\max**<*version*>**.pof**. For more information, refer to "Restoring the MAX V CPLD to the Factory Settings" on page 3–5.

The flash writer version blinks the SEL 2, 1, and 0 LEDs and does not support the Power Monitor, Clock Control, or other logic functions. Use the flash writer only for flash programming.

To ensure that you have the most up-to-date factory restore files and information about this product, refer to the Cyclone V SoC Development Kit page of the Altera website.

4. Board Update Portal

The Board Update Portal web page provides links to useful information on the Altera website. You can use this web page to interact with your board:

- Blinking LEDs
- Writing text messages to the LCD
- Mouse over the board photo to view features

The Board Update Portal web page is served by the web server application running on the HPS on your board.

Connecting to the Board Update Portal Web Page

Ensure that you have the following setup or installed:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. Ensure that the CSEL and BSEL jumpers (Table 3–4 on page 3–4) and the DIP switch SW2.3 (Table 3–1 on page 3–2) are in the factory default positions.
2. Attach an Ethernet cable to the HPS Ethernet connector (J2) on the upper left of the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router and obtains an IP address and displays it to the LCD. If no IP address is obtained, the LCD displays *No IP obtained*. If the system booted, the LCD displays *Hello Tim*.

   If the LCD displays *No IP obtained*, your system partially booted, but without Ethernet access. If you receive the *No IP obtained* message, Altera recommends that you install the USB virtual COM port drivers to access the Linux system through a terminal window.

   For more information, refer to the *Configuring Serial Connection* section of the Linux Getting Started page on RocketBoards.org.

   There are several reasons why your board may fail to get and IP address in this step:

   - Your port is not active or the cable is not plugged in.
   - You do not have a DHCP server.
   - Your DHCP server ran out of addresses.
   - Your DHCP server was not allowed to respond to the board due to security filters, such as MAC address filtering.

4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

   ☞ You can click *Cyclone V SoC Development Kit* on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

You can also navigate directly to the Cyclone V SoC Development Kit page of the Altera website to determine if you have the latest kit software.

5. Board Test System

The development kit includes an application called the Board Test System (BTS) and related design examples. The BTS provides an easy-to-use interface to alter functional settings and observe the results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage. (While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.)

To install the BTS, follow the steps in "Installing the Development Kit" on page 2–2.

The Board Test System GUI communicates over the JTAG bus to a test design running in the Cyclone V device. Figure 5–1 shows the initial GUI for a board that is in the factory configuration.

Look for yellow highlights in the board picture around the corresponding components for each tab.

Figure 5–1. Board Test System Graphical User Interface

Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears that allows you to exercise the related board features.

The **Power Monitor** button starts the Power Monitor application that measures and reports current power information for the board. Because the application communicates over the JTAG bus to the MAX II device, you can measure the power of any design in the FPGA, including your own designs.

The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board for the Board Test System

With the power to the board off, follow these steps:

1. Plug the included USB cable from J37 (USB-Blaster II interface) to the host computer's USB port.
2. Ensure that the development board switches and jumpers are set to the default positions as shown in the "Factory Default Switch and Jumper Settings" section starting on page 3–1.

For more information about the board's DIP switch and jumper settings, refer to the *Cyclone V SoC Development Board Reference Manual*.

CAUTION

To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

Navigate to the <*install dir*>**\kits\cycloneVSX_5csxfc6df31_soc\examples\board_test_system** directory and run the **BoardTestSystem.exe** application.

To run the BTS in Windows, you can also click **Start** > **All Programs** > **Altera** > **Cyclone V SoC Development Kit** <*version*> > **Board Test System**.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. Typically the board will not be pre-programmed with a BTS design. One must be loaded using the Configure menu as described in the next section.

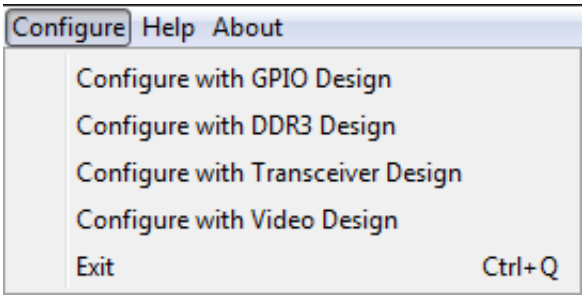
Using the Board Test System

This section describes each control in the BTS.

The Configure Menu

Use the Configure menu to select the design you want to use. Each design example on this menu tests different board features that corresponds to one or more application tabs. For example, if you select **Configure with GPIO Design**, the **System Info**, **GPIO**, and **I2C** tabs become active.

Figure 5–2. The Configure Menu



The System Info Tab

The **System Info** tab shows board's current configuration. Figure 5–1 on page 5–1 shows the **System Info** tab. The tab displays the contents of the MAX V registers, the JTAG chain, the board's MAC address, the flash memory map, and other details stored on the board.

The following sections describe the controls on the **System Info** tab.

Board Information

The **Board information** controls display static information about your board.

- **Board Name**—Indicates the official name of the board.
- **Part number**—Indicates the part number of the board.
- **Serial number**—Indicates the serial number of the board.
- **Factory test version**—Indicates the version of the Board Test System currently running on the board.
- **MAC1**—Indicates the MAC address of the board's ENET1 10/100 port.
- **MAC2**—Indicates the MAC address of the board's ENET2 10/100 port.
- **HPS MAC1**—Indicates the MAC address of the board's HPS 10/100/1000 Ethernet port.
- **MAX V ver**—Indicates the version of MAX V code currently running on the board. The MAX V code resides in the *<install dir>***kits\cycloneVSX_5csxfc6df31_soc\examples** directory. Newer revisions of this code might be available on the Cyclone V SoC Development Kit page of the Altera website.

JTAG Chain

The **JTAG chain** control shows all the devices currently in the JTAG chain. The Cyclone V device is always the first device in the chain. The JTAG chain is normally mastered by the On-board USB-Blaster II.

If you plug in an external USB-Blaster cable to the JTAG header (J23), the On-Board USB-Blaster II is disabled.

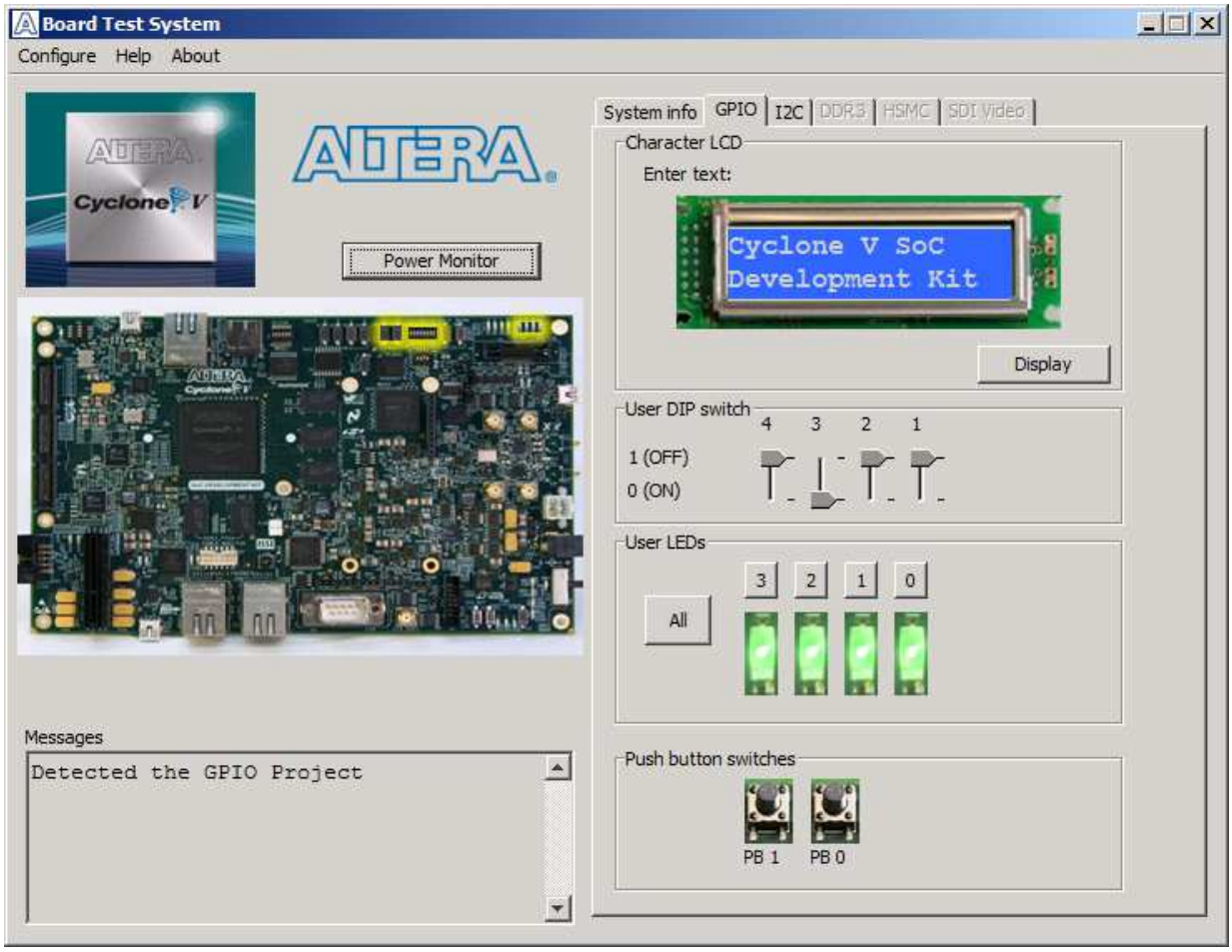
JTAG DIP switch bank (SW4) selects which interfaces are in the chain. Refer to Table 3–3 on page 3–4 for detailed settings.

For details on the JTAG chain, refer to the *Cyclone V SoC Development Board Reference Manual.* For USB-Blaster II configuration details, refer to the On-Board USB-Blaster II page.

The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. You can write to the character LCD, read DIP switch settings, turn LEDs on or off, and detect push button presses. Figure 5–3 shows the **GPIO** tab.

Figure 5–3. The GPIO Tab



The following sections describe the controls on the **GPIO** tab.

Character LCD

The **Character LCD** controls allow you to display text strings on the character LCD on your board. Type text in the text boxes and then click **Display**.

☞ If you exceed the 16 character display limit on either line, a warning message appears.

User DIP Switch

The read-only **User DIP switch** control displays the current positions of the switches in the user DIP switch bank. Change the switches on the board to see the graphical display change accordingly.