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Stratix V GX FPGA Development Kit

User Guide

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UG-01103-1.4

Contents

Appendix A. Programming the Flash Memory Device

Additional Information

1. About This Kit

The Altera® Stratix® V GX FPGA Development Kit is a complete design environment that includes both the hardware and software you need to develop Stratix V GX FPGA designs. The following list describes what you can accomplish with the kit:

- Test signal quality of the FPGA transceiver I/Os (10 Gbps+).
- Develop and test PCI Express® (PCIe) 3.0 designs.
- Develop and test memory subsystems consisting of SyncFlash, DDR3, and QDRII+.
- Develop and test SDI with the embedded 75-ohm 3G SDI transceivers.
- Develop embedded designs utilizing the Nios® II processor and external memory.
- Develop and test network designs utilizing Triple Speed Ethernet MegaCore® and external RJ-45 jack.
- Develop and test optical networking designs using
  - 10G and 40G Ethernet MAC MegaCores.
  - Quad small form factor pluggable (QSFP) optical interface.
- Take advantage of the modular and scalable design by using the high-speed mezzanine card (HSMC) connectors to interface to over 40 different HSMCs provided by Altera partners, supporting protocols such as Serial RapidIO®, 10 Gigabit Ethernet, SONET, Common Public Radio Interface (CPRI), Open Base Station Architecture Initiative (OBSAI) and others.
- Measure the FPGA's power consumption.
- Control twelve different programmable clock oscillators using the Clock Control GUI.

Kit Features

This section briefly describes the Stratix V GX FPGA Development Kit contents.

Hardware

The Stratix V GX FPGA Development Kit includes the following hardware:

- Stratix V GX FPGA development board—A development platform that allows you to develop and prototype hardware designs running on the Stratix V GX FPGA.

  For detailed information about the board components and interfaces, refer to the *Stratix V GX FPGA Development Board Reference Manual*.

- HSMC loopback board—A daughtercard that allows for loopback testing all signals on the HSMC interface using the Board Test System.

- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - Standard USB A to micro-USB cable
  - Ethernet cable
  - 75 Ω SMB video cable

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Software

Your kit includes a license for the Development Kit Edition (DKE) of the Quartus II software (Windows platform only). For one year, this license entitles you to most of the features of the Subscription Edition (excluding the IP Base Suite).

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software. For more information, refer to the Design Software page of the Altera website.

The Quartus II Development Kit Edition (DKE) software includes the following items:

- Quartus II Software—The Quartus II software, including the Qsys system integration tool, provides a comprehensive environment for network on a chip (NoC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system.
  - Verify the functionality of your design, and quickly and easily evaluate its size and speed.
  - Generate time-limited device programming files for designs that include MegaCore functions.
  - Program a device and verify your design in hardware.

  The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

  For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.

- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allows you to develop embedded software for the Nios II processor that you can include in your Altera FPGA designs.

Stratix V GX FPGA Development Kit Installer

The license-free Stratix V GX FPGA Development Kit installer includes all the documentation and design examples for the kit.

For information on installing the Development Kit Installer, refer to "Software Installation" on page 3–1.

The remaining chapters in this user guide lead you through the following Stratix V GX FPGA development board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the FPGA development board
- Configuring the Stratix V GX FPGA
- Running the Board Test System designs

For complete information about the FPGA development board, refer to the *Stratix V GX FPGA Development Board Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in "Kit Features" on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Board

To inspect the board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

   CAUTION Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.

In typical applications with the Stratix V GX FPGA development board, a heat sink is not necessary. However, under extreme conditions or for engineering sample silicon the board might require additional cooling to stay within operating temperature guidelines. The board has two holes near the FPGA that accommodate many different heat sinks, including the Dynatron CHR-152. You can perform power consumption and thermal modeling to determine whether your application requires additional cooling. For information about measuring board and FPGA temperature in real time, refer to "The Power Monitor" on page 6–21.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the Stratix V GX FPGA Development Kit page.
- For additional daughter cards available for purchase, refer to the Development Board Daughtercards page.
- For the Stratix V GX device documentation, refer to the Literature: Stratix V Devices page.
- To purchase devices from the eStore, refer to the Devices page.
- For Stratix V GX OrCAD symbols, refer to the Capture CIS Symbols page.
- For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

3. Software Installation

This chapter explains how to install the following software:

- Quartus II Subscription Edition Software
- Stratix V GX FPGA Development Kit
- USB-Blaster™ II driver

Installing the Quartus II Subscription Edition Software

Included in the Quartus II Subscription Edition Software are the Quartus II software (including Qsys), the Nios II EDS, and the MegaCore IP Library. To install the Altera development tools, perform the following steps:

1. Download the Quartus II Subscription Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.
2. Follow the on-screen instructions to complete the installation process.

If you have difficulty installing the Quartus II software, refer to *Altera Software Installation and Licensing Manual*.

Activating Your License

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus II software.

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web Edition or purchase a subscription to Quartus II software.

Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, follow these steps:

1. Log on at the myAltera Account Sign In web page, and click **Sign In**.
2. On the myAltera Home web page, click the *Self-Service Licensing Center* link.
3. Locate the serial number printed on the side of the development kit box below the bottom bar code.

   The number consists of alphanumeric characters and does not contain hyphens: for example, *5xxxSoCxxxxxxx*.
4. On the Self-Service Licensing Center web page, click the *Find it with your License Activation Code* link.

5. In the **Find/Activate Products** dialog box, enter your development kit serial number and click **Search**.
6. When your product appears, turn on the check box next to the product name.
7. Click **Activate Selected Products**, and click **Close**.
8. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus II software to enable the software.

   To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

For complete licensing details, refer to *Altera Software Installation and Licensing Manual*.

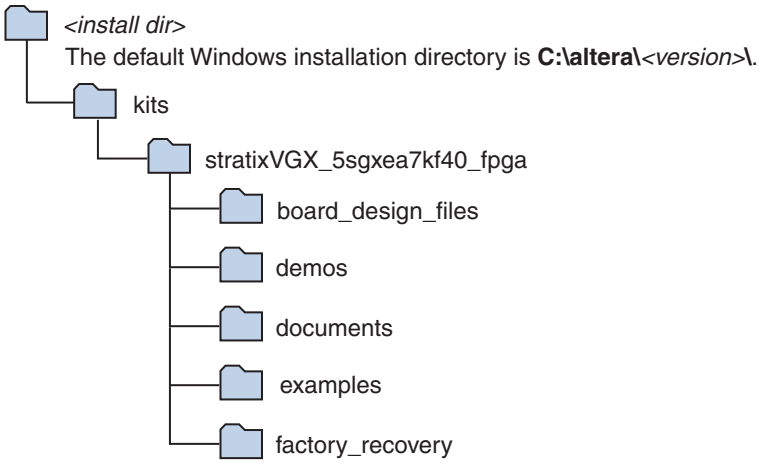
Installing the Stratix V GX FPGA Development Kit

Perform the following steps:

1. Download the Stratix V GX FPGA Development Kit installer from the Stratix V GX FPGA Development Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.
2. Start the Stratix V GX FPGA Development Kit installer **.exe**, or unzip the installation image for Linux.
3. Follow the on-screen instructions to complete the installation process. Choose an installation directory in the same relative location to the Quartus II software installation.

The installation program creates the Stratix V GX FPGA Development Kit directory structure shown in Figure 3–1.

Figure 3–1. Stratix V GX FPGA Development Kit Installed Directory Structure (1)



Note to Figure 3–1:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications when available.
documents	Contains the kit documentation.
examples	Contains the sample design files for the Stratix V GX FPGA Development Kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster II Driver

The Stratix V GX FPGA development board includes integrated On-Board USB-Blaster II circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster II driver on the host computer.

Installation instructions for the USB-Blaster II driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

4. Development Board Setup

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Stratix V GX FPGA development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch Settings" on page 4–1 to return the board to its factory settings before proceeding.
2. The FPGA development board ships with design examples stored in the flash memory device. Verify the DIP switch SW5.3 is set to the off position to load the design stored in the factory portion of flash memory. Figure 4–2 shows the DIP switch location on the back of the Stratix V GX FPGA development board.
3. Verify that the HSMC card is installed on port A (connector J1) of the board.
4. Verify that the HSMC card is installed on port B (connector J2) of the board.
5. Ensure that the power switch SW2 is in the off position.
6. Connect the Power Adpater +19 V, 6.32 A to the DC Power Jack (J4) on the FPGA board and plug the cord into a power outlet.

   CAUTION: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

7. Set the POWER switch (SW2) to the on position. When power is supplied to the board, Power blue LED (D24) illuminates, indicating that the board has power.

The MAX V device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. The DIP switch SW5.3 controls which design to load. When the switch is in the off position, the PFL loads the design from the factory portion of flash memory.

The kit includes a MAX V design which contains the MAX V PFL megafunction. The design resides in the *<install dir>*\kits\stratixVGX_5sgxea7kf40_fpga\examples\max5 directory.

When configuration is complete, the Config Done LED (D17) illuminates, signaling that the Stratix V GX device configured successfully.

For more information about the PFL megafunction, refer to *AN 386: Parallel Flash Loader Megafunction User Guide*.

Factory Default Switch Settings

This section shows the factory switch settings for the Stratix V GX FPGA development board.

Figure 4–1 shows the switch locations and the default position of each switch on the top side of the board.

Figure 4–1. Switch Locations and Default Settings on the Board Top

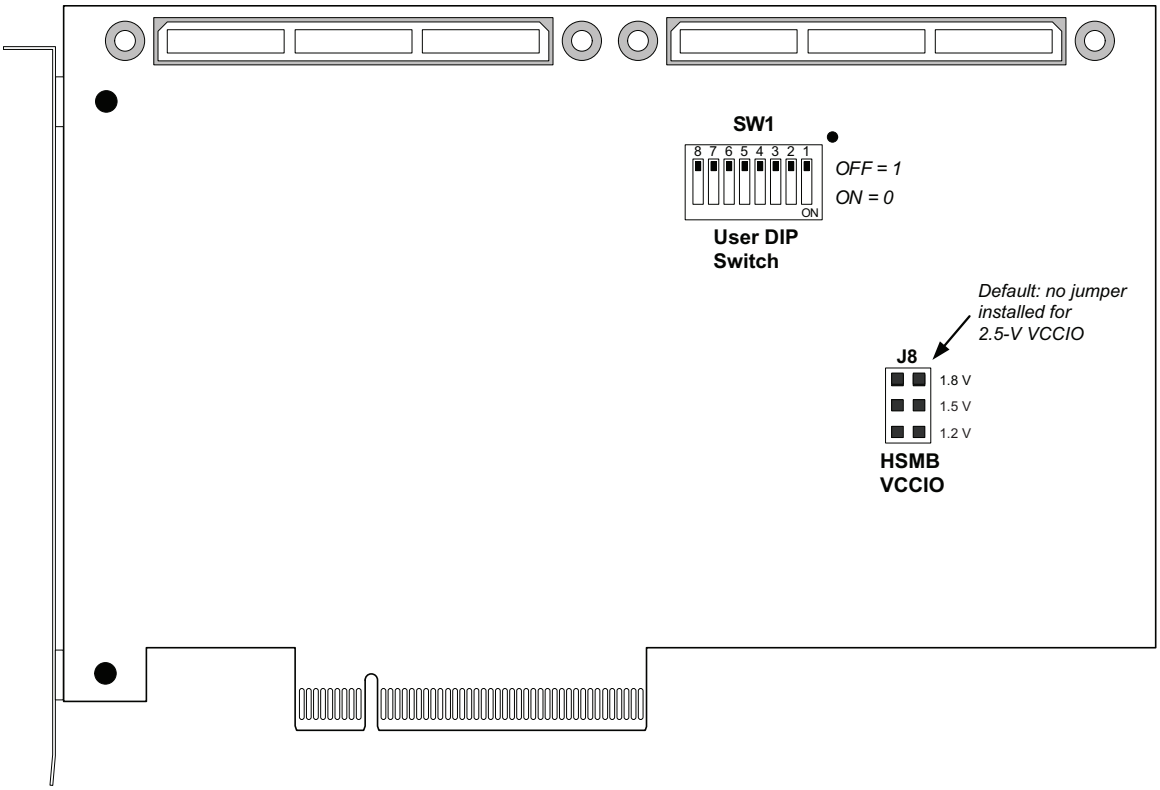
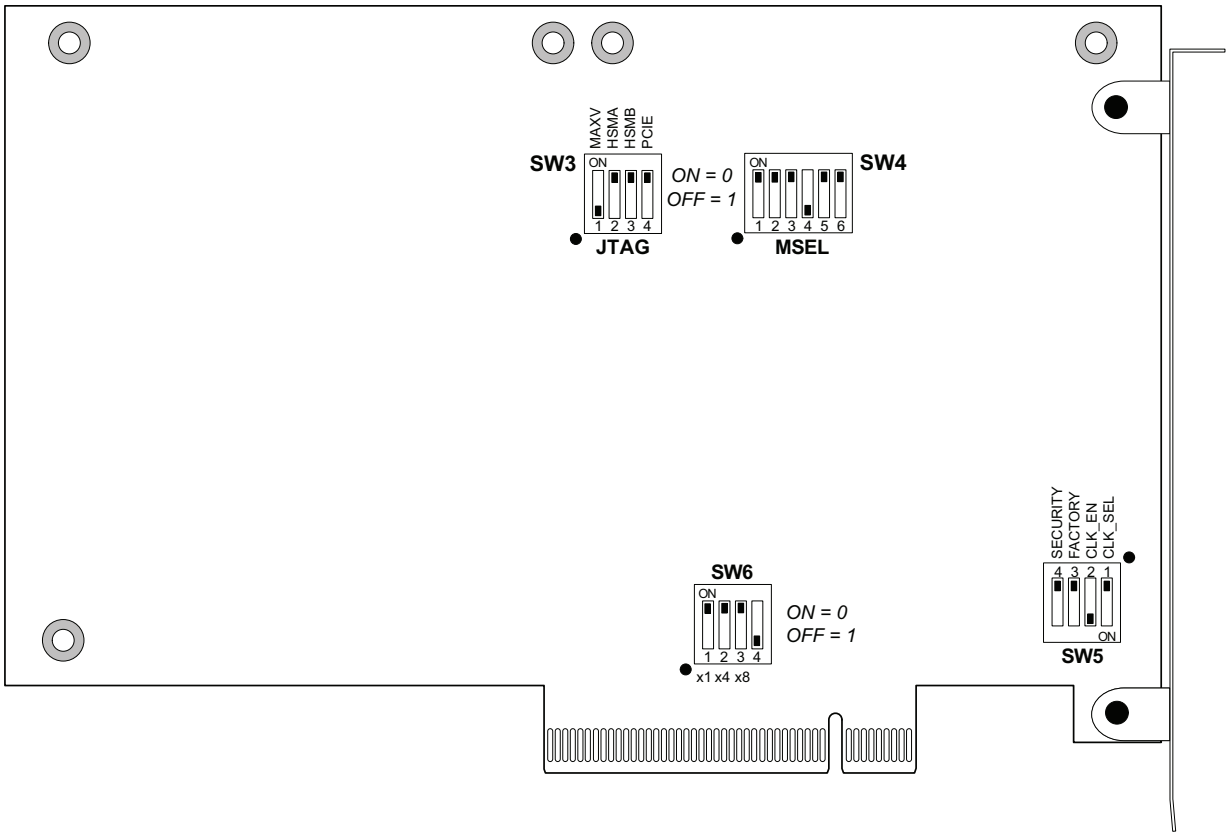


Figure 4–2 shows the switch locations and the default position of each switch on the bottom side of the board.

Figure 4–2. Switch Locations and Default Settings on the Board Bottom



To restore the switches to their factory default settings, perform the following steps:

1. Set jumper block (J8) to match Table 4–1 and Figure 4–1. Not installing any jumpers (default) = 2.5 V.

Table 4–1. J8 Jumper Block (1)

Jumper	HSMB VCCIO	Position
Pins 1-2	1.8 V	Not Installed
Pins 3-4	1.5 V	Not installed
Pins 5-6	1.2 V	Not installed

Note to Table 4–1:

(1) Adding a single jumper between the pins sets the voltage as described in the table. Install only one jumper location at a time.

2. Set the DIP switch bank (SW3) to match Table 4–2 and Figure 4–2.

Table 4–2. SW3 JTAG DIP Switch Settings (1)

Switch	Board Label	Function	Default Position
1	MAX_JTAG_EN	Switch 1 has the following options: ■ When on (0), removes the MAX V system controller in the JTAG chain. ■ When off (1), includes the MAX V system controller from the JTAG chain.	Off
2	HSMA_JTAG_EN	Switch 2 has the following options: ■ When on (0), removes the HSMC Port A in the JTAG chain. ■ When off (1), includes the HSMC Port A from the JTAG chain.	On
3	HSMB_JTAG_EN	Switch 3 has the following options: ■ When on (0), removes the HSMC Port B in the JTAG chain. ■ When off (1), includes the HSMC Port B from the JTAG chain.	On
4	PCIE_JTAG_EN	Switch 4 has the following options: ■ When on (0), removes the PCI Express Edge connector from the JTAG chain. ■ When off (1), includes the PCI Express Edge connector in the JTAG chain.	On

Note to Table 4–2:

(1) If you plug in an external USB-Blaster cable to the JTAG header (J10), the On Board USB-Blaster II is disabled. The JTAG chain is normally mastered by the on-board USB-Blaster II.

For details on the JTAG chain, refer to the *Stratix V GX FPGA Development Board Reference Manual*.

3. Set DIP switch bank (SW4) to match Table 4–3 and Figure 4–2.

Table 4–3. SW4 MSEL DIP Switch Settings (1)

Switch	Board Label	Function	Default Position
1	MSEL0	Configuration Setting 0	On (0)
2	MSEL1	Configuration Setting 1	On (0)
3	MSEL2	Configuration Setting 2	On (0)
4	MSEL3	Configuration Setting 3	Off (1)
5	MSEL4	Configuration Setting 4	On (0)
6	—	—	On (0)

Note to: Table 4–3

(1) Set MSEL[4:0] to valid configuration schemes as listed in the *Stratix V Device Handbook*.

4. Set DIP switch bank (SW5) to match Table 4–4 and Figure 4–2.

If you use an external USB Blaster, Altera recommends that you disable the power-up configuration of the FPGA by changing the MSEL(4:0) DIP switch (SW4) from 01000 to 11000. This will prevent power-up FPGA configuration from flash in the default FPPx32 mode. The On-Board USB-Blaster II is disabled when you plug in an external USB Blaster, which prevents the JTAG FACTORY command from being sent to disable the security mode JTAG lockout prior to configuring the Stratix V. The On-Board USB-Blaster II issues the JTAG FACTORY command when the SECURITY switch (SW5.4) is set to 1. For more information on the *Stratix V ES JTAG Port Access Limitation After Configuration*, refer to *Errata Sheet and Guidelines for Stratix V ES Devices*.

Table 4–4. SW5 DIP Switch Settings

Switch	Board Label	Function	Default Position
1	CLK_SEL	Switch 1 has the following options: ■ When on (0), the SMA input clock is selected. ■ When off (1), the programmable oscillator clock is selected.	Off
2	CLK_EN (1)	Switch 2 has the following options: ■ When on (0), the on-board oscillator is enabled. ■ When off (1), the on-board oscillator is disabled.	On
3	FACTORY (1)	Switch 3 has the following options: ■ When on (0), loads the user design from flash at power up. ■ When off (1), loads the factory design from flash at power up.	Off
4	SECURITY (1)	Switch 4 has the following options: ■ When on (0), does not send factory command at power up. ■ When off (1), sends factory command at power up.	Off

Note to Table 4–4:

(1) Functionality of the CLK_EN, FACTORY and SECURITY settings are dependent on the MAX V system controller CPLD. In order to function properly, the MAX V CPLD must be programmed with the required MAX V design.

5. Set DIP switch bank (SW6) to match Table 4–5 and Figure 4–2.

Table 4–5. SW6 DIP Switch Settings

Switch	Board Label	Function	Default Position
1	PCIE_PRSNT2n_x1	Switch 1 has the following options: ■ When on (0), x1 presence detect is enabled. ■ When off (1), x1 presence detect is disabled.	On
2	PCIE_PRSNT2n_x4	Switch 2 has the following options: ■ When on (0), x4 presence detect is enabled. ■ When off (1), x4 presence detect is disabled.	On
3	PCIE_PRSNT2n_x8	Switch 3 has the following options: ■ When on (0), x8 presence detect is enabled. ■ When off (1), x8 presence detect is disabled.	On
4	—	—	Off

For more information about the FPGA board settings, refer to the *Stratix V GX FPGA Development Board Reference Manual*.

5. Board Update Portal

The Stratix V GX FPGA Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the DIP switch SW5.3 in the off position, the Stratix V GX FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware 1 portion of flash memory and provides links to useful information on the Altera website, including kit-specific links and design resources.

After successfully updating the user hardware 1 flash memory, you can load the your design from flash memory into the FPGA. To do so, set the DIP switch SW5.3 to the on position and power cycle the board, which loads the user 1 design into flash.

The source code for the Board Update Portal design resides in the <*install dir*>**\kits\stratixVGX_5sgxea7kf40_fpga\examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page A–3.

Connecting to the Board Update Portal Web Page

Ensure that you have the following items setup and installed:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. With the board powered down, set the DIP switch SW5.3 to the off position, which loads the factory design into flash.
2. Attach the Ethernet cable from the board to your LAN.
3. Power up the board. The board connects to the LAN's gateway router, and obtains an IP address. The LCD on the board displays the IP address.
4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

   You can click **Stratix V GX FPGA Development Kit** on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

You can also navigate directly to the Stratix V GX FPGA Development Kit page of the Altera website to determine if you have the latest kit software.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user hardware 1 portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

Design files available from the Stratix V GX FPGA Development Kit page include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Preparing Design Files for Flash Programming" on page A–1 for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" to access the Board Update Portal web page.
2. In the **Hardware File Name** field, specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field. Otherwise, leave the **Software File Name** field blank.
3. Click **Upload**, and a progress bar indicates the percent complete.
4. To configure the FPGA with the new design after the flash memory upload process is complete, set the DIP switch SW5.3 to the on position and power cycle the board. Refer to Table 6–1 on page 6–4 for an alternative method of programming the FPGA using push-buttons.

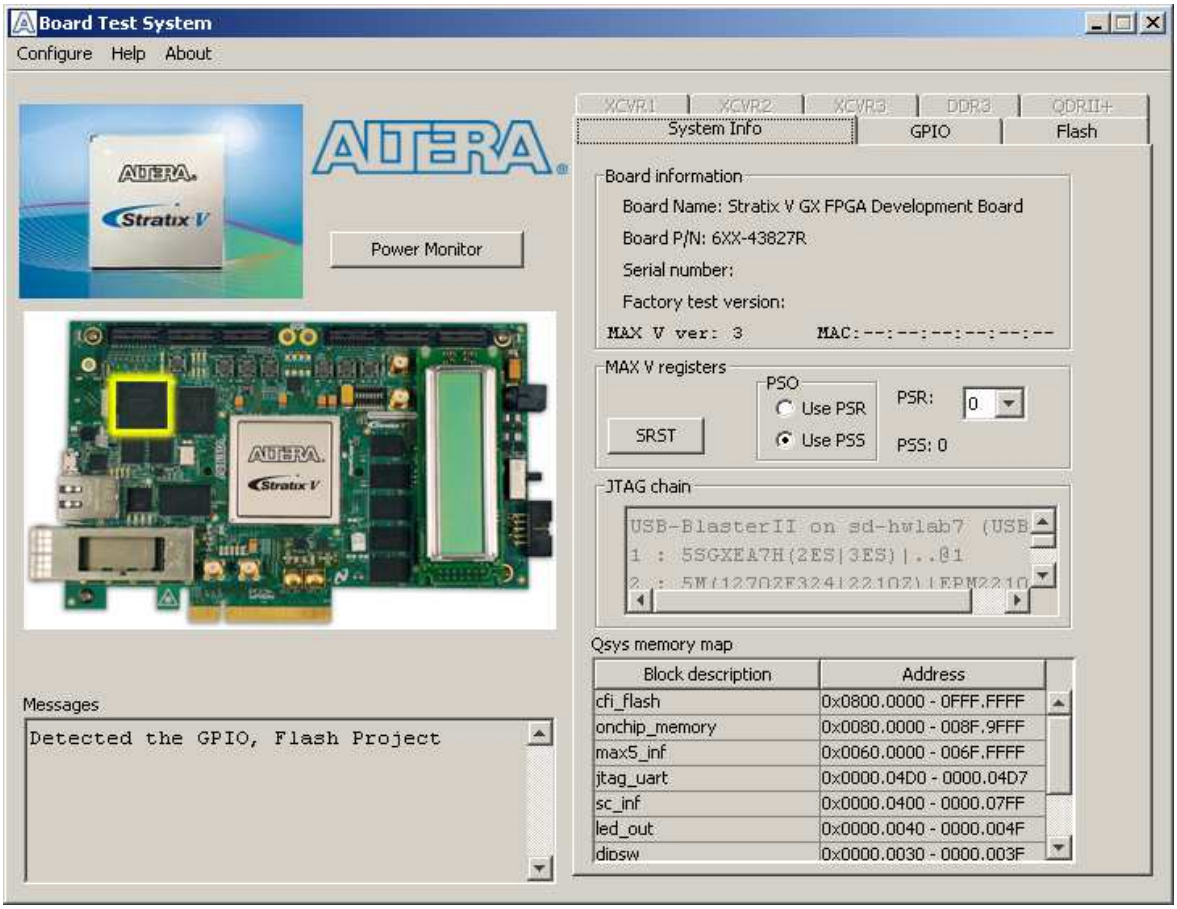
As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user hardware 1 portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "Restoring the Flash Device to the Factory Settings" on page A–3.

6. Board Test System

The kit includes design examples and an application called the Board Test System to test the functionality of the Stratix V GX FPGA development board. The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the application to test board components, modify functional parameters, observe performance, and measure power usage. (While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.) To install the Board Test System, follow the steps in "Installing the Stratix V GX FPGA Development Kit" on page 3–2.

The Board Test System communicates over the JTAG bus to a test designs running in the Stratix V GX device. Figure 6–1 shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.