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DSP Pro Development Board

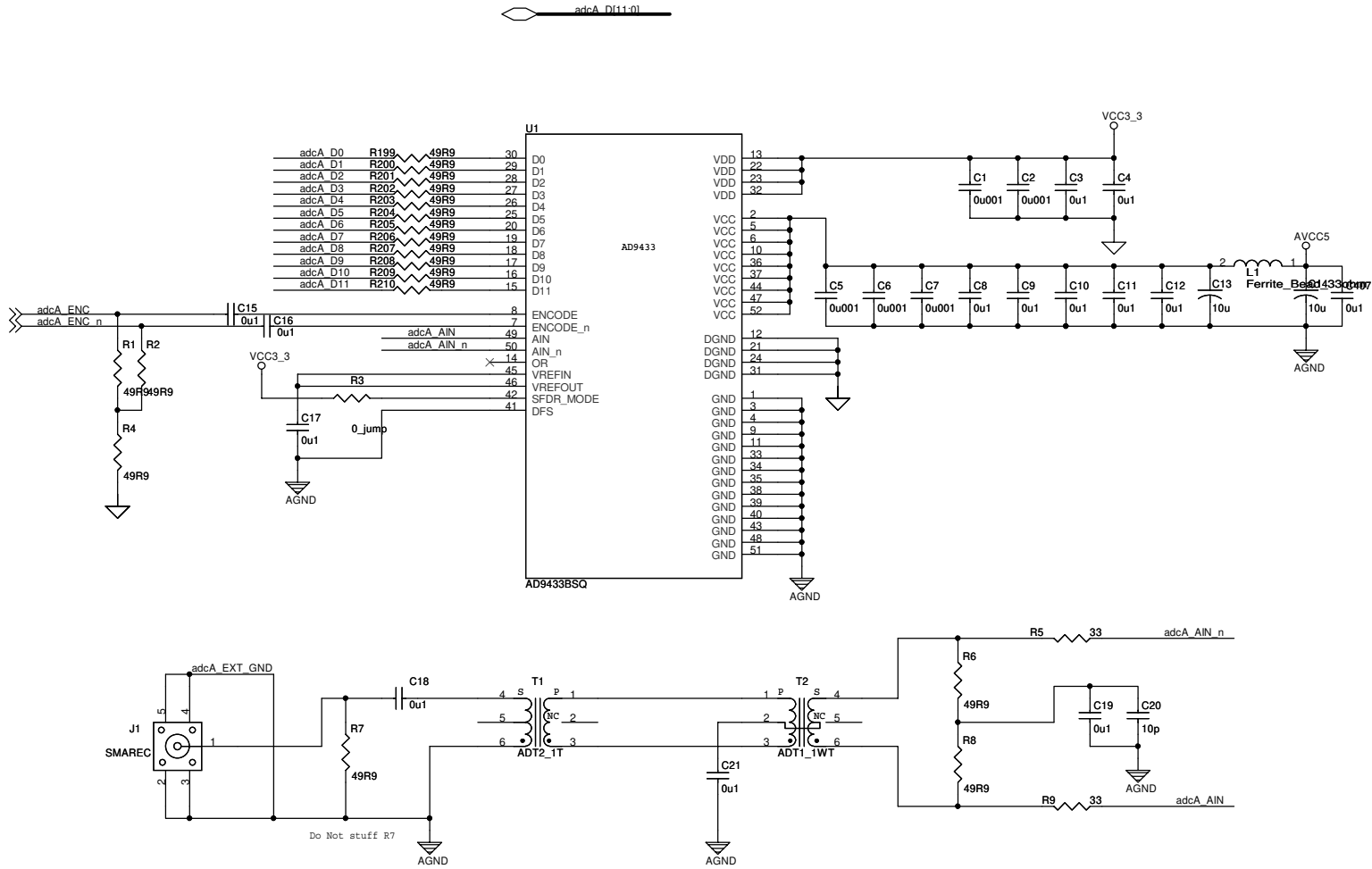
Stratix II 2S180 Edition

Rev 01

Revision History		
Date	Change Description	Rev
8/18/05	Created schematic and changed the component from the 2S60 on the DSP board to the 2S180 on this Pro version of the board	01

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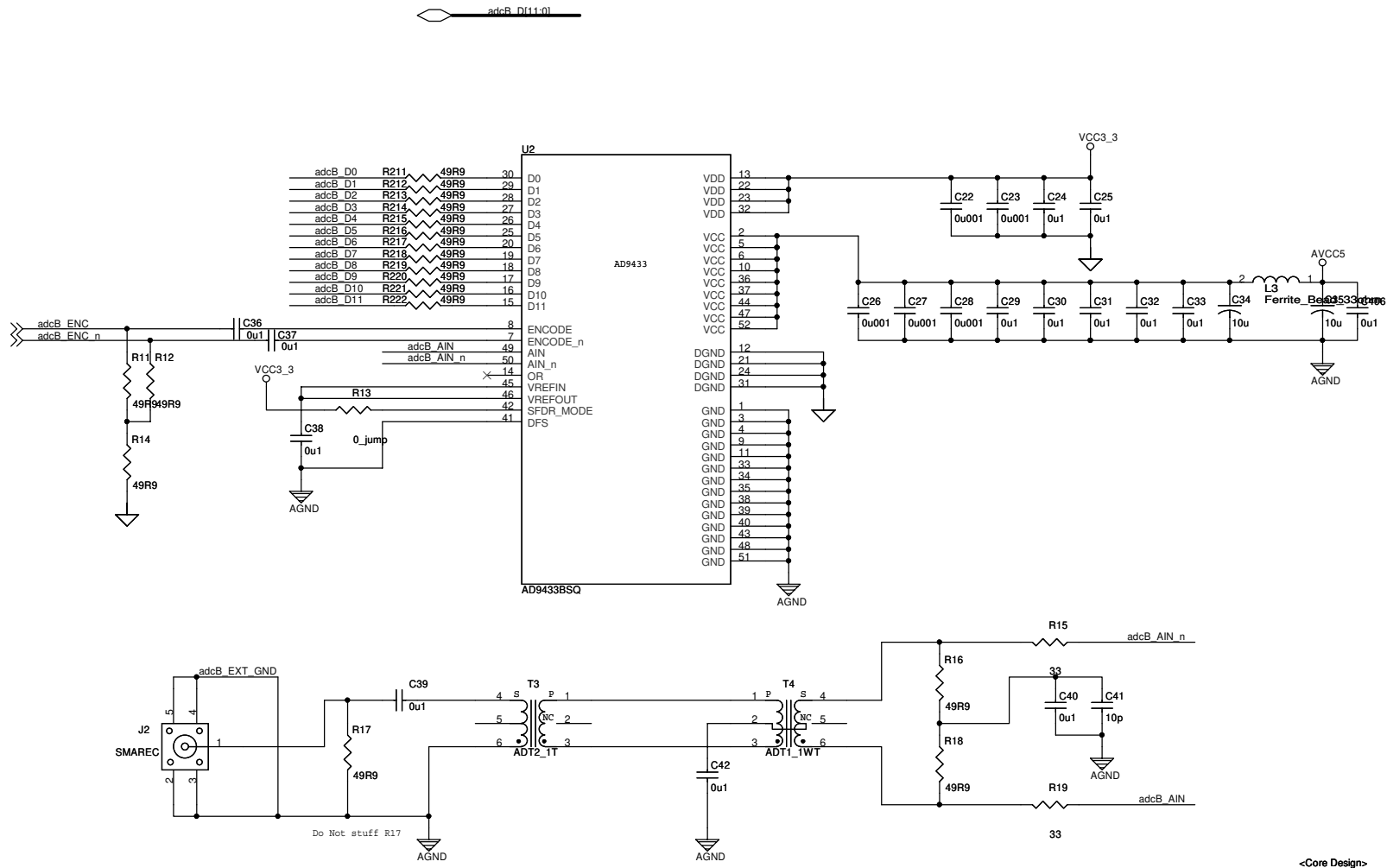
Altera Corp. 110 Cooper Street, Suite 201, Santa Cruz, CA, 95060		
Title DSP Pro Stratix II 2S180 (Maine Pro)		
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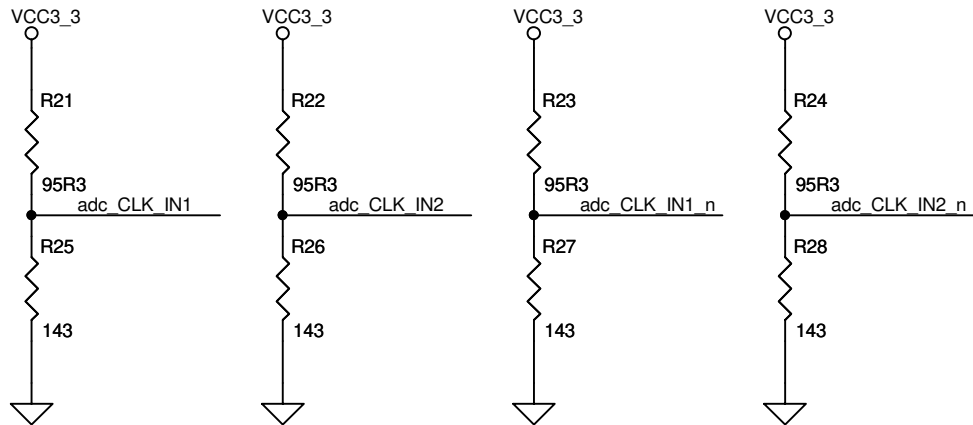
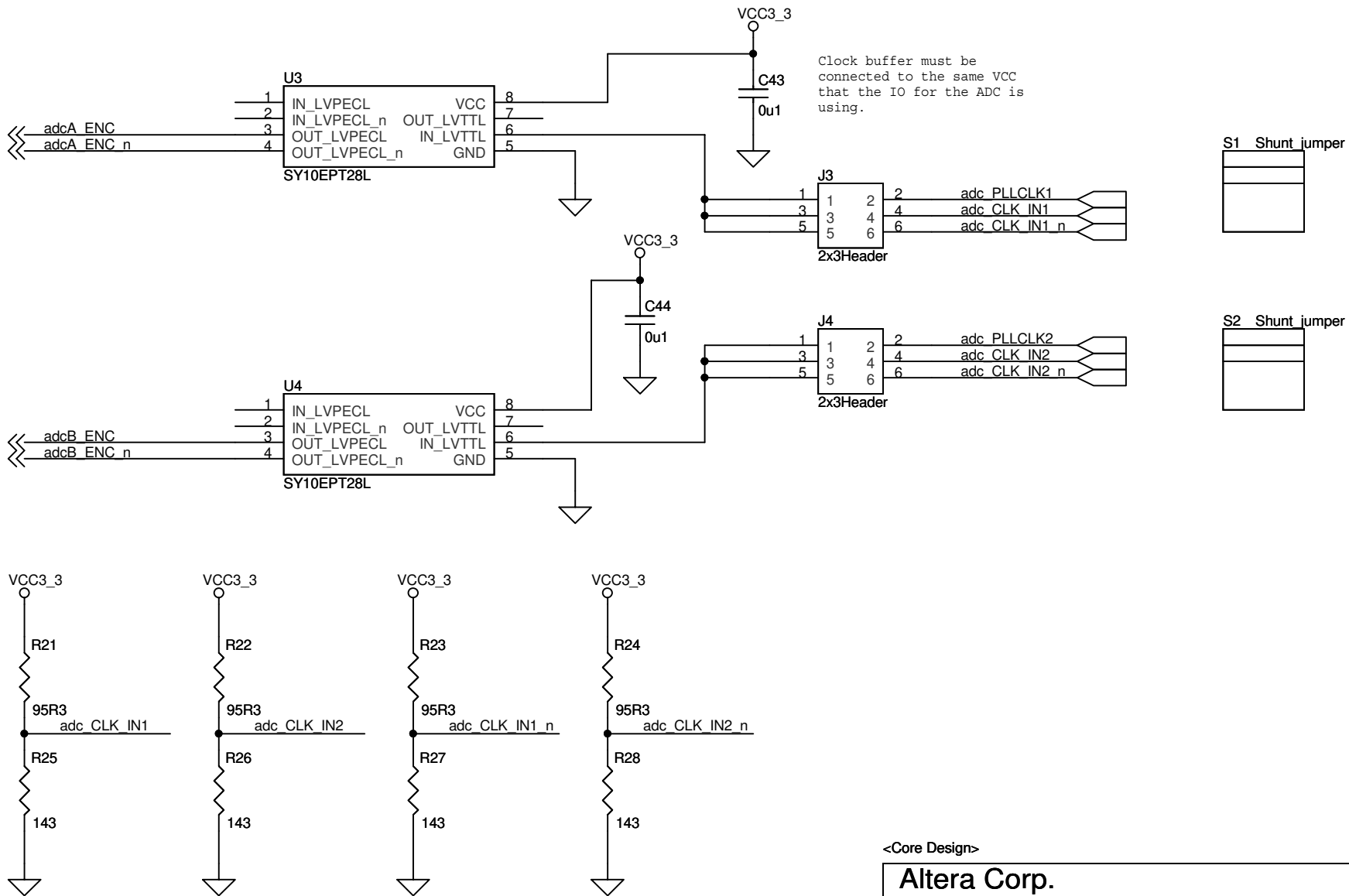


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ADC Clock Selection



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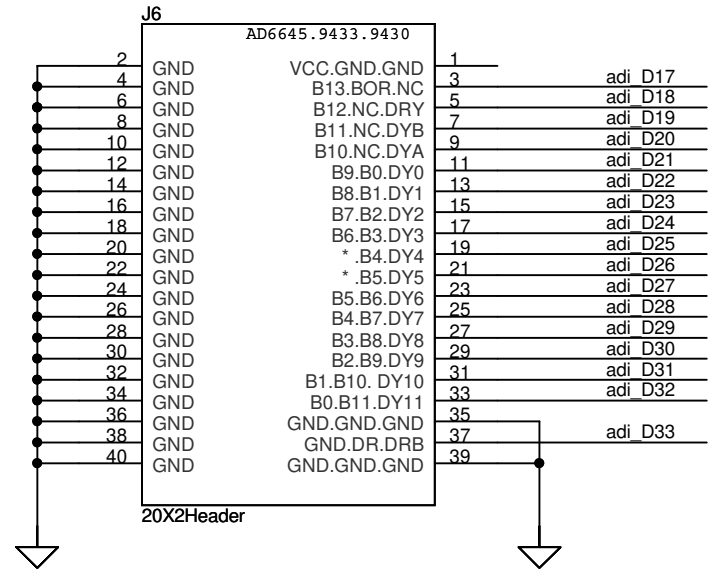
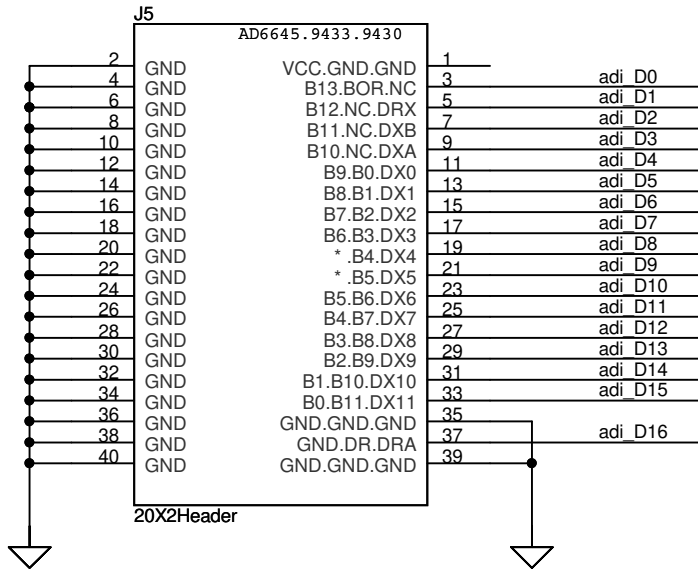
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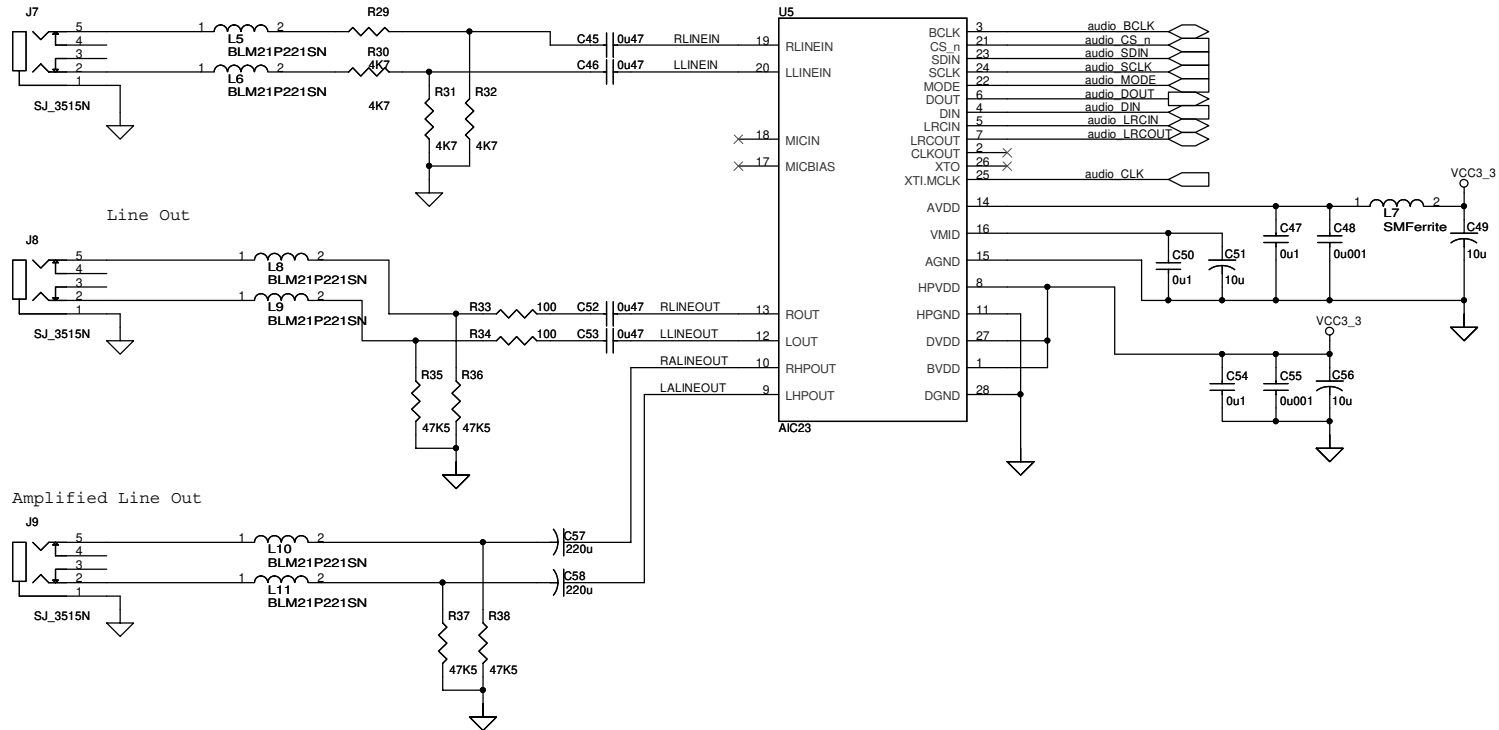
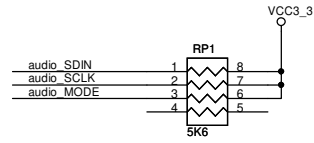
ADI Connector

adi_D[33:0]



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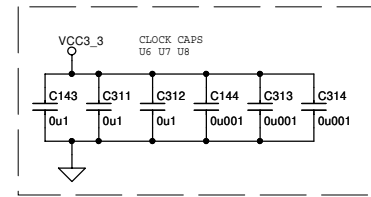
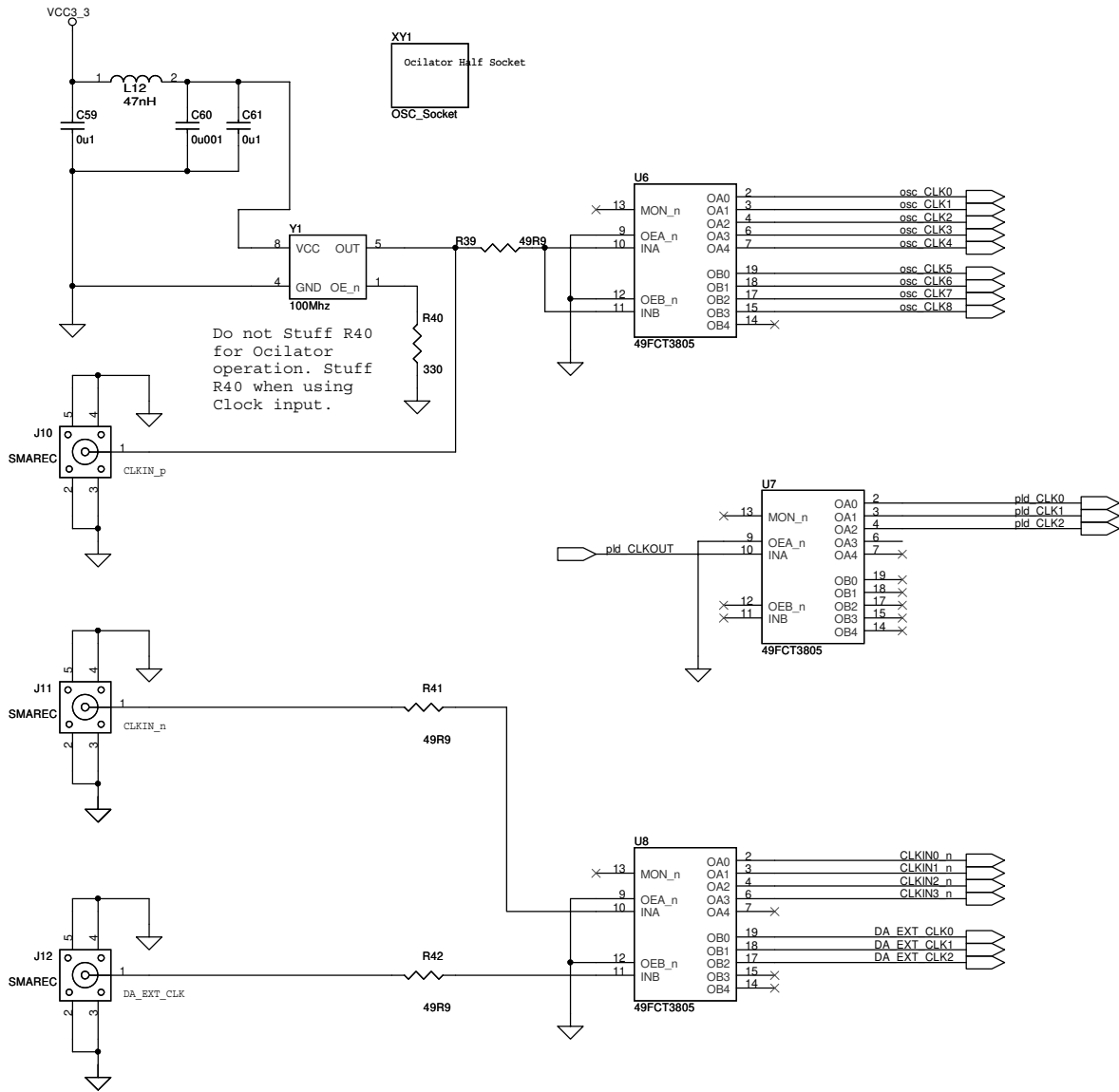
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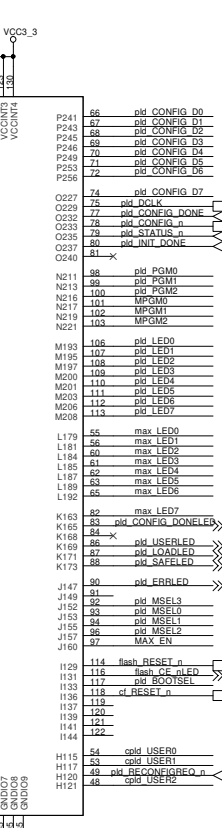
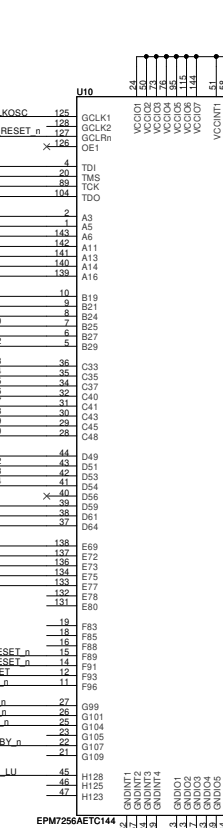
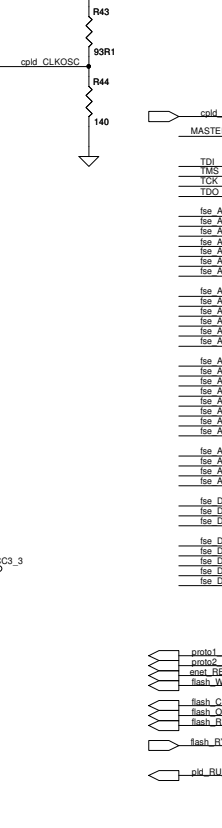
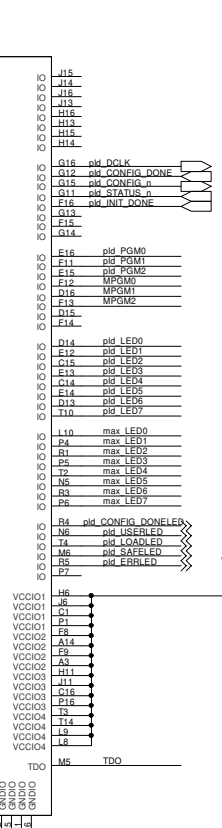
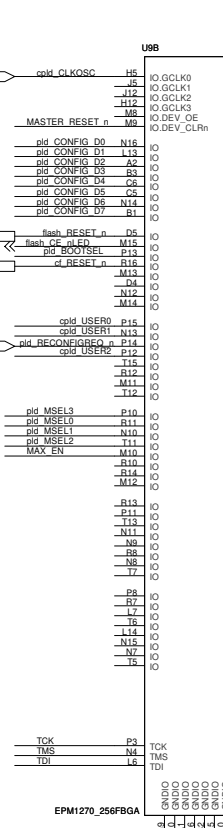
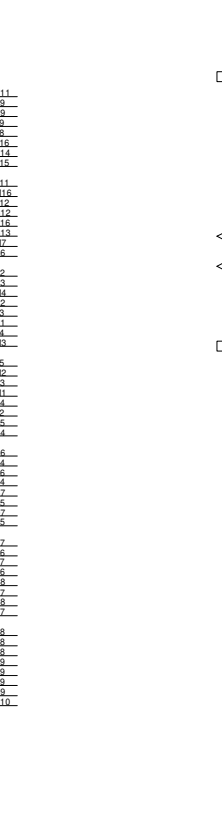
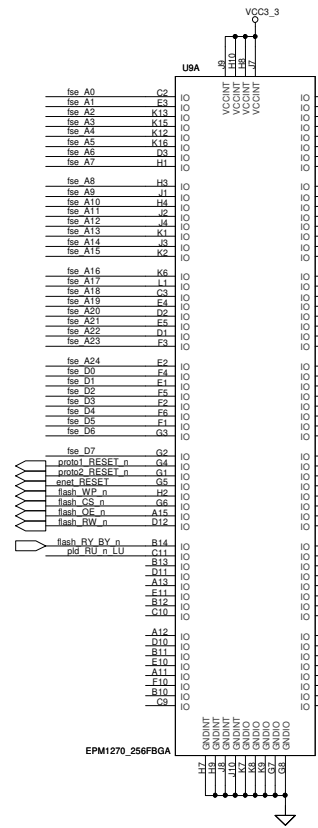
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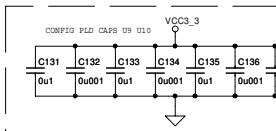
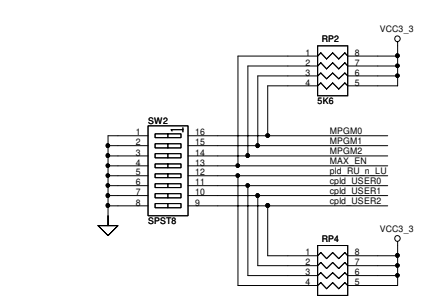
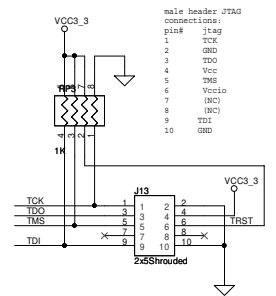
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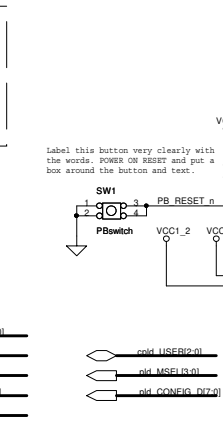
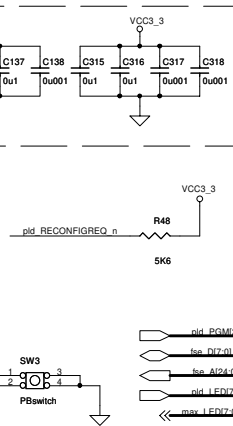
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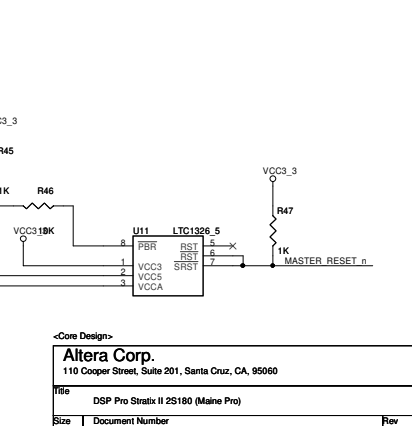
Configuration PLD



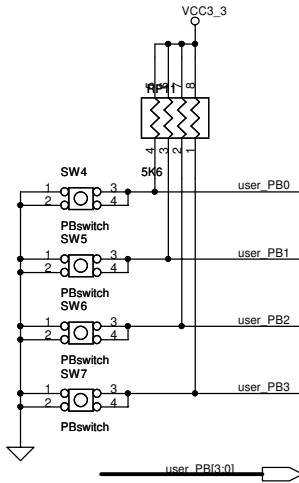
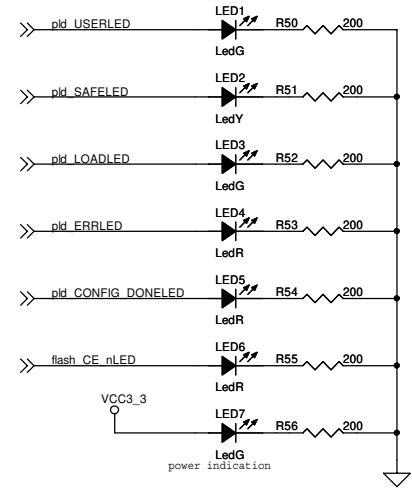
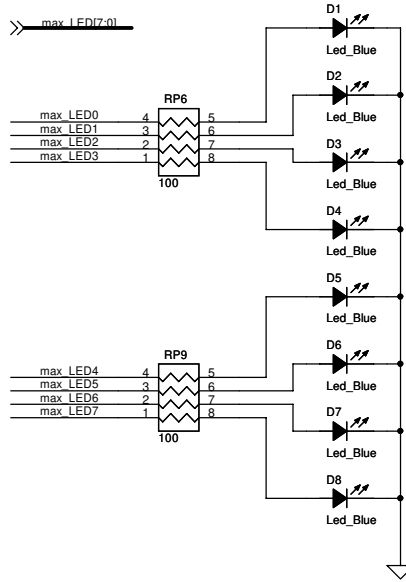
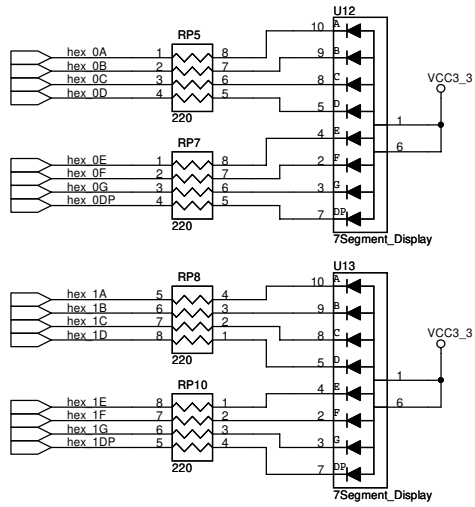
pld_BOOTSEL determines whether to force a boot from the default boot sector, or the user-programmed boot sector.



Label this button very clearly with the words, POWER ON RESET and put a box around the button and text.



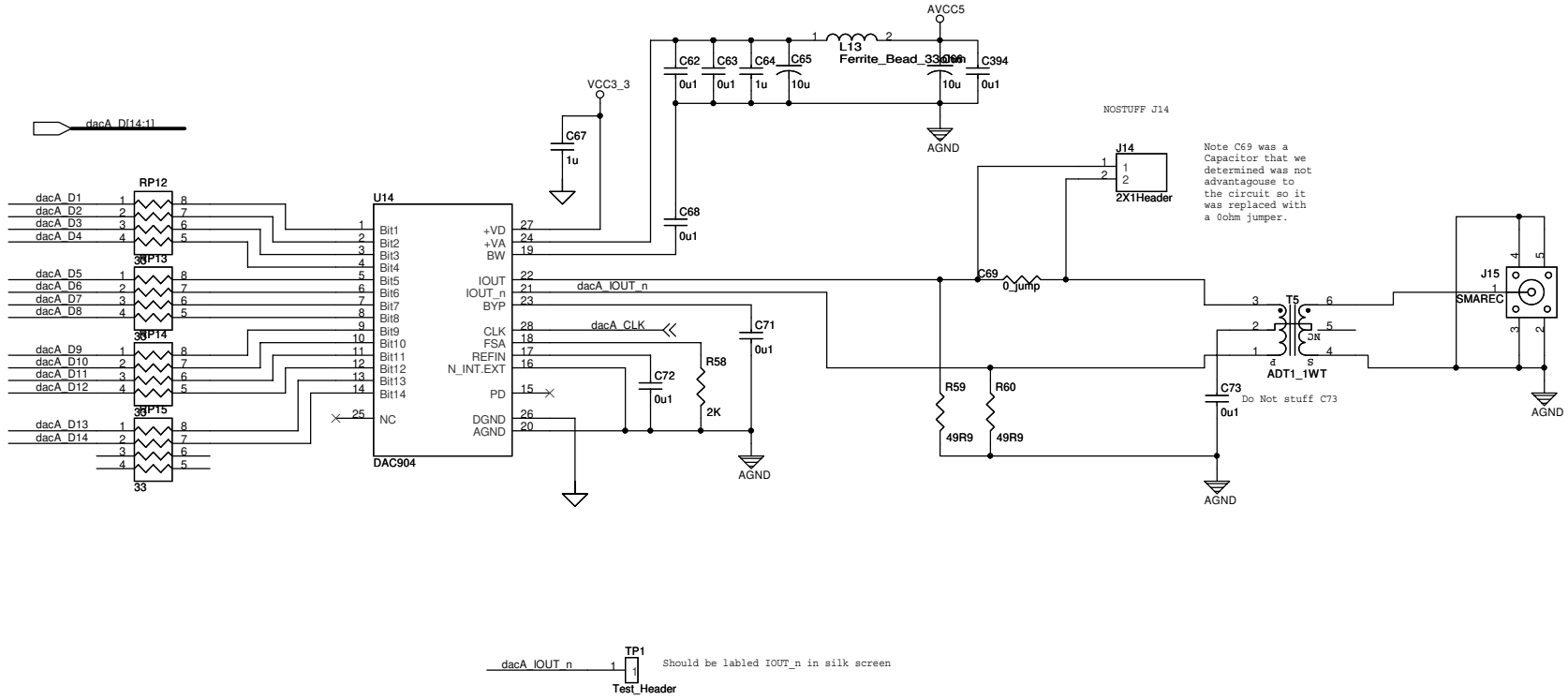
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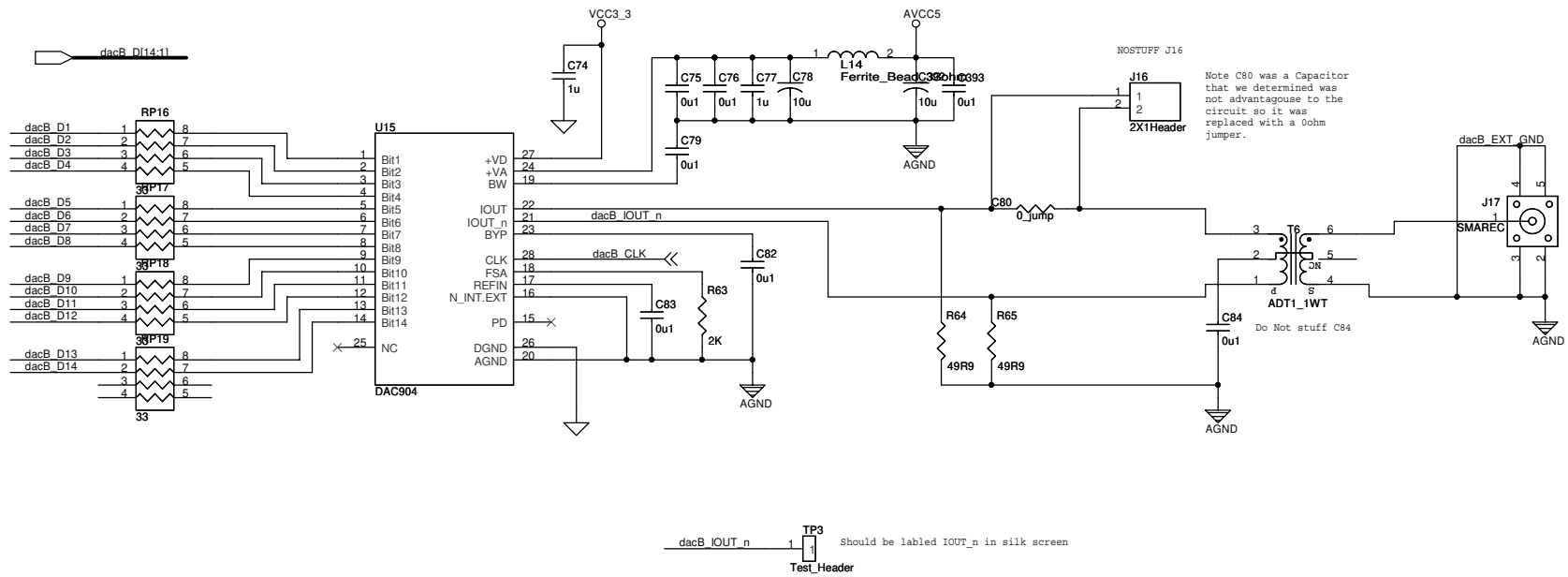
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Note C69 was a Capacitor that we determined was not advantageous to the circuit so it was replaced with a 0ohm jumper.

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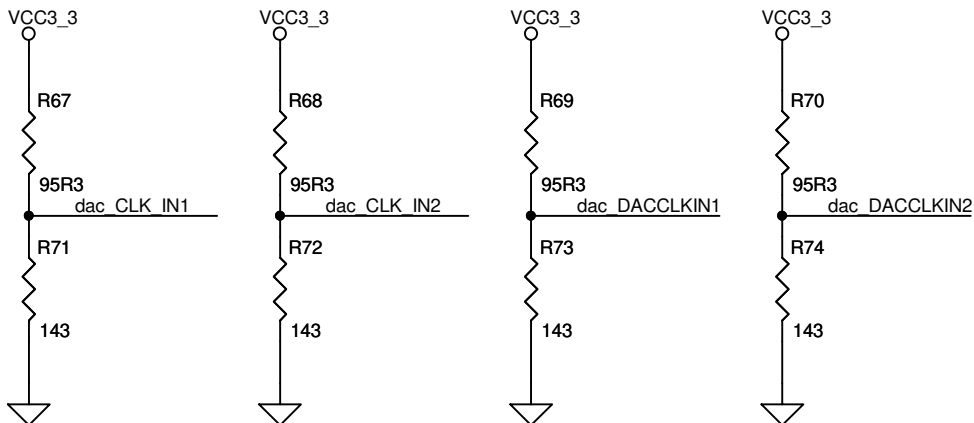
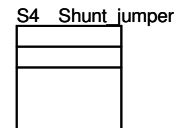
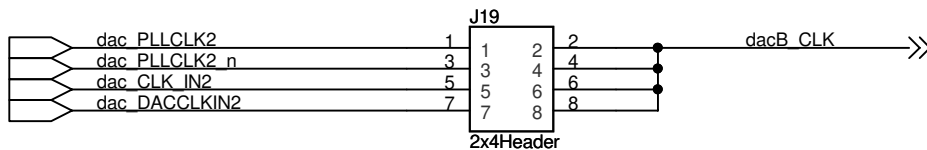
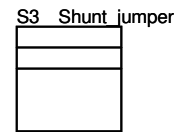
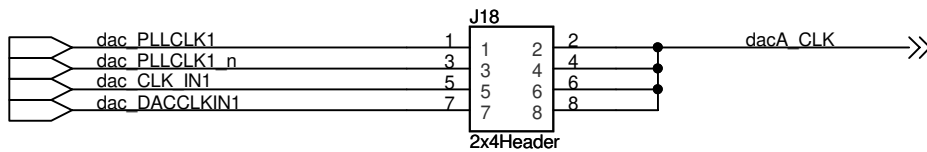
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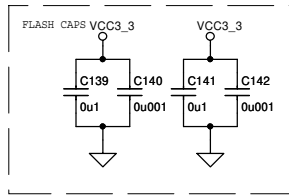
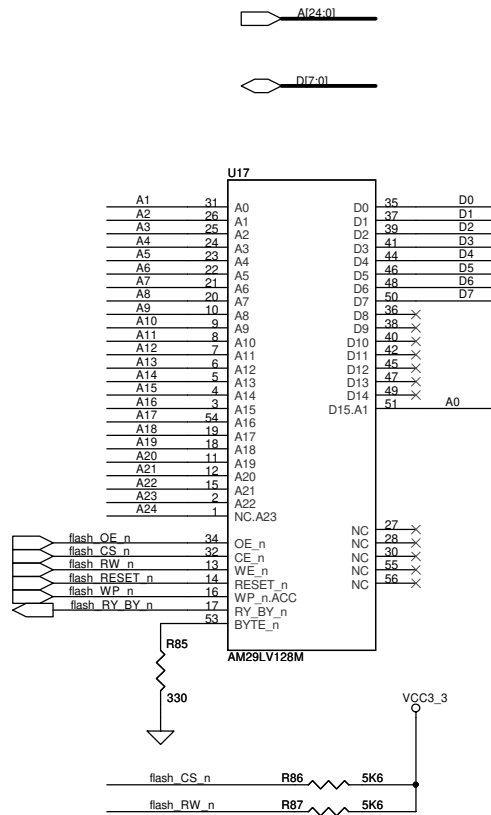
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DAC Clock Jumper



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Flash chip is 16M x 8 for 16Mbytes of flash

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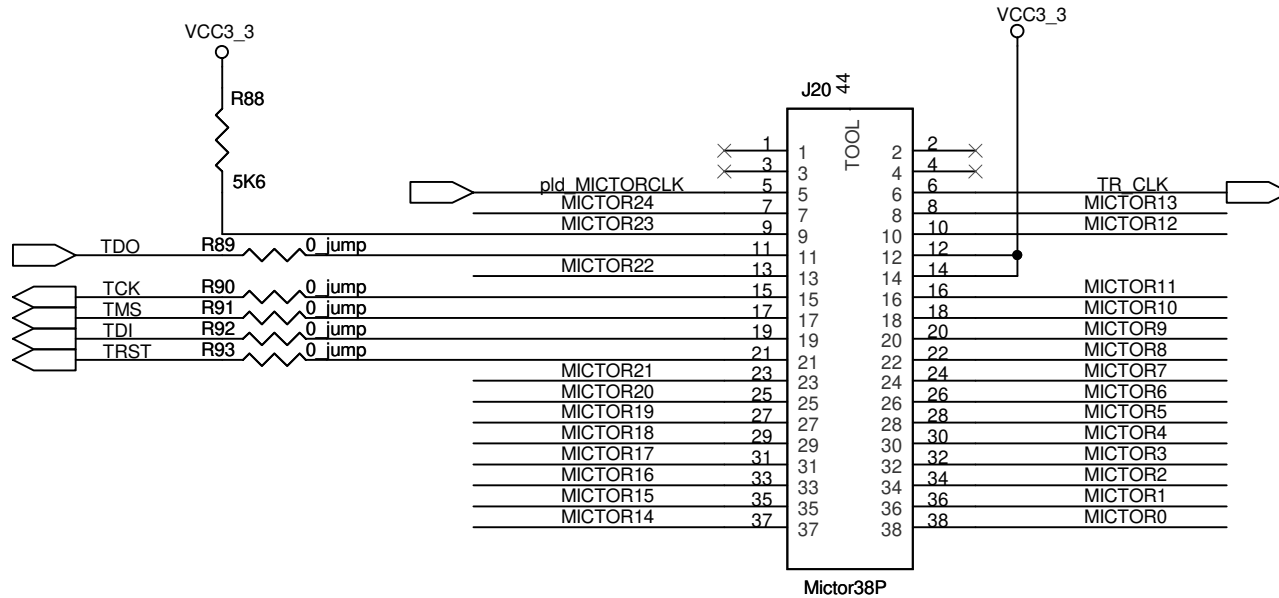
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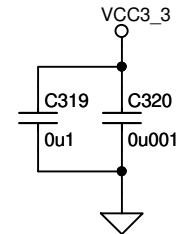
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Mictor Connector

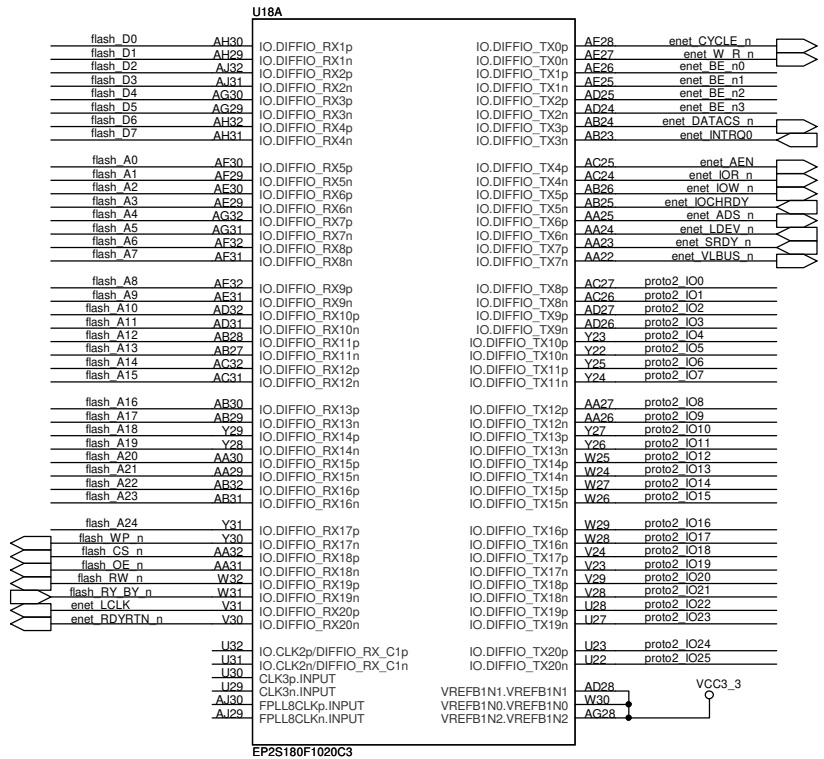


MICTOR124:01

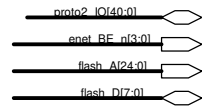


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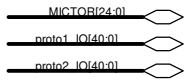
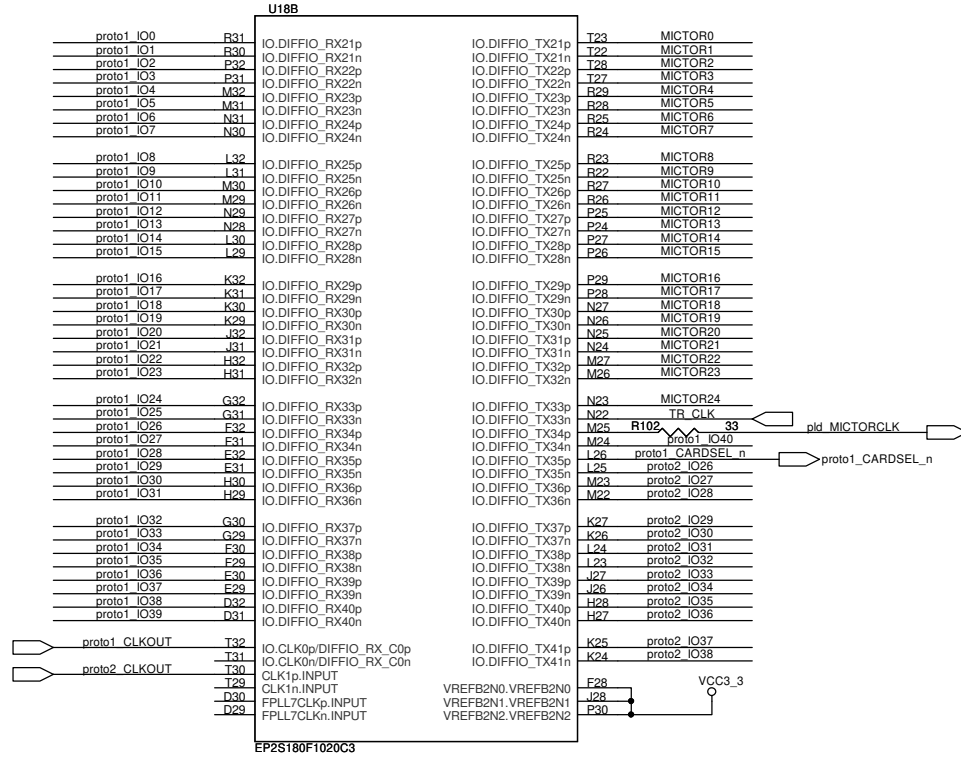
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PLD Bank 2

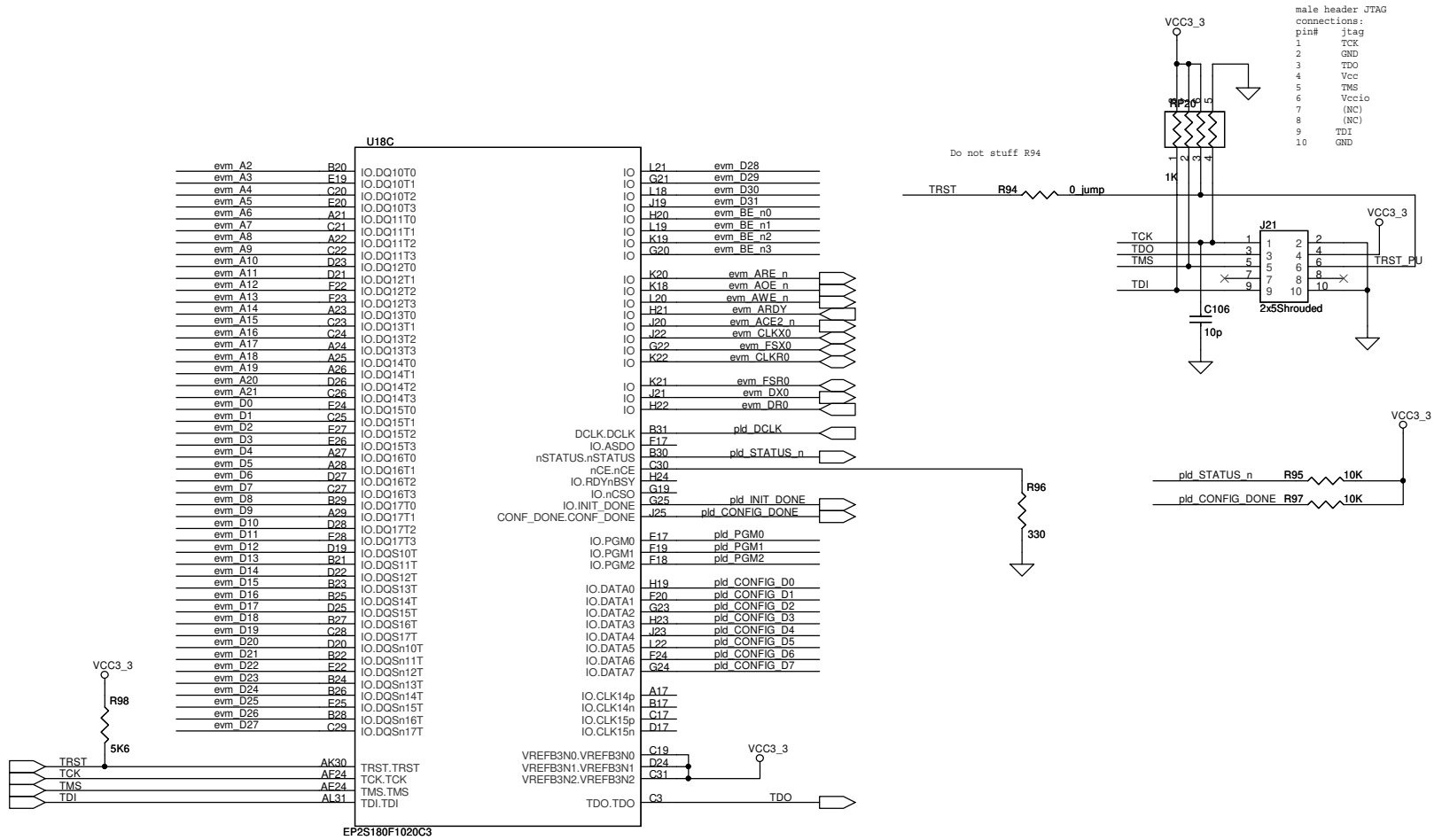


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PLD Bank 3



male header JTAG connections:

pin#	jtag
1	TCK
2	GND
3	TDO
4	Vcc
5	TMS
6	Vccio
7	(NC)
8	(NC)
9	TDI
10	GND

- evm_A[21:2]
- evm_D[31:0]
- evm_BE_n[3:0]
- pld_PGM[2:0]
- pld_CONFIG_D[7:0]

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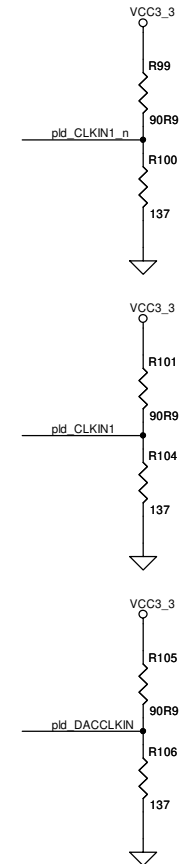
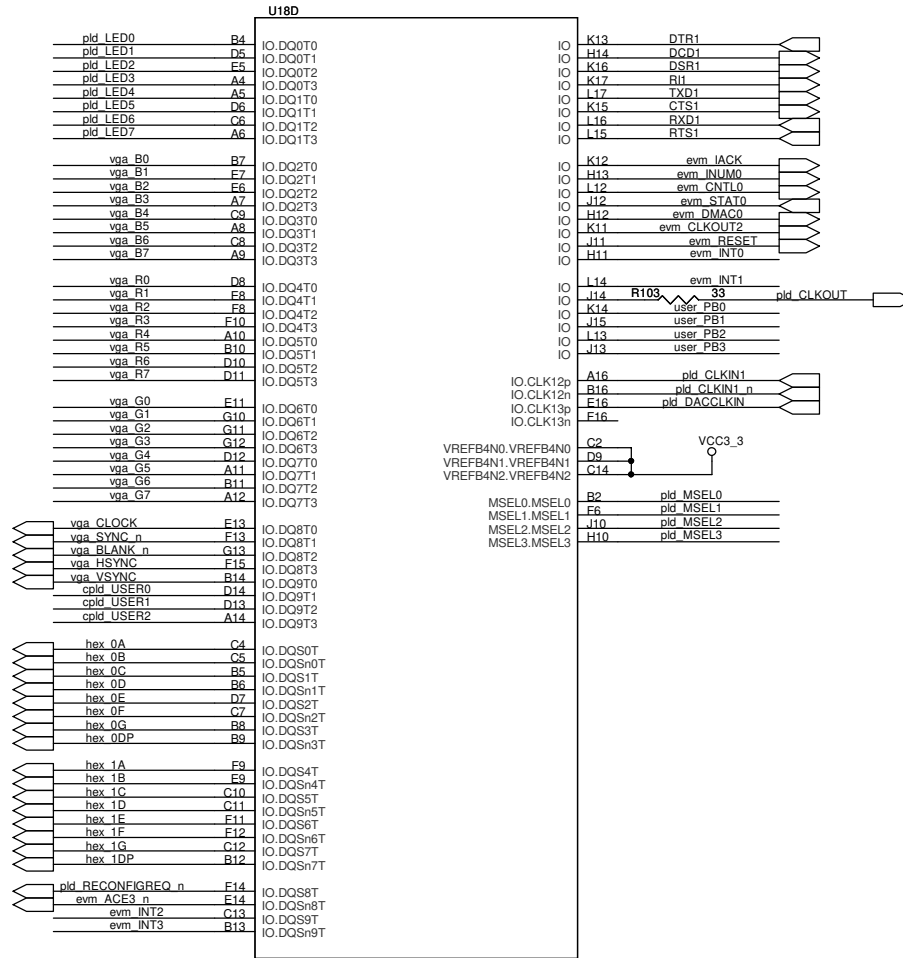
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PLD Bank 4



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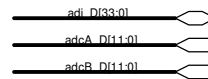
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U18E

adcA D0	D1			J6	adi D16
adcA D1	D2	IO.DIFFIO_RX43p	IO.DIFFIO_TX42p	J7	adi D17
adcA D2	E3	IO.DIFFIO_RX43n	IO.DIFFIO_TX42n	J8	adi D18
adcA D3	E4	IO.DIFFIO_RX44p	IO.DIFFIO_TX43p	J9	adi D19
adcA D4	F1	IO.DIFFIO_RX44n	IO.DIFFIO_TX43n	K8	adi D20
adcA D5	F2	IO.DIFFIO_RX45p	IO.DIFFIO_TX44p	K9	adi D21
adcA D6	F3	IO.DIFFIO_RX45n	IO.DIFFIO_TX44n	L9	adi D22
adcA D7	F4	IO.DIFFIO_RX46p	IO.DIFFIO_TX45p	L10	adi D23
		IO.DIFFIO_RX46n	IO.DIFFIO_TX45n		
adcA D8	F1	IO.DIFFIO_RX47p	IO.DIFFIO_TX46p	L7	adi D24
adcA D9	F2	IO.DIFFIO_RX47n	IO.DIFFIO_TX46n	L8	adi D25
adcA D10	G3	IO.DIFFIO_RX48p	IO.DIFFIO_TX47p	K6	adi D26
adcA D11	G4	IO.DIFFIO_RX48n	IO.DIFFIO_TX47n	K7	adi D27
adcB D0	G1	IO.DIFFIO_RX49p	IO.DIFFIO_TX48p	L6	adi D28
adcB D1	G2	IO.DIFFIO_RX49n	IO.DIFFIO_TX48n	L6	adi D29
adcB D2	J3	IO.DIFFIO_RX50p	IO.DIFFIO_TX49p	M10	adi D30
adcB D3	J4	IO.DIFFIO_RX50n	IO.DIFFIO_TX49n	M11	adi D31
adcB D4	H1	IO.DIFFIO_RX51p	IO.DIFFIO_TX50p	M8	adi D32
adcB D5	H2	IO.DIFFIO_RX51n	IO.DIFFIO_TX50n	M9	adi D33
adcB D6	J1	IO.DIFFIO_RX52p	IO.DIFFIO_TX51p	M6	
adcB D7	J2	IO.DIFFIO_RX52n	IO.DIFFIO_TX51n	M7	
adcB D8	K3	IO.DIFFIO_RX53p	IO.DIFFIO_TX52p	N6	
adcB D9	K4	IO.DIFFIO_RX53n	IO.DIFFIO_TX52n	N7	
adcB D10	K1	IO.DIFFIO_RX54p	IO.DIFFIO_TX53p	N8	
adcB D11	K2	IO.DIFFIO_RX54n	IO.DIFFIO_TX53n	N9	
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adi D1	L4	IO.DIFFIO_RX55n	IO.DIFFIO_TX54n	P9	
adi D2	N4	IO.DIFFIO_RX56p	IO.DIFFIO_TX55p	P6	
adi D3	N5	IO.DIFFIO_RX56n	IO.DIFFIO_TX55n	P7	
adi D4	M3	IO.DIFFIO_RX57p	IO.DIFFIO_TX56p	P4	
adi D5	M4	IO.DIFFIO_RX57n	IO.DIFFIO_TX56n	P5	
adi D6	L1	IO.DIFFIO_RX58p	IO.DIFFIO_TX57p	P10	
adi D7	L2	IO.DIFFIO_RX58n	IO.DIFFIO_TX57n	P11	
adi D8	N2	IO.DIFFIO_RX59p	IO.DIFFIO_TX58p	R6	
adi D9	N3	IO.DIFFIO_RX59n	IO.DIFFIO_TX58n	R7	
adi D10	M1	IO.DIFFIO_RX60p	IO.DIFFIO_TX59p	R4	
adi D11	M2	IO.DIFFIO_RX60n	IO.DIFFIO_TX59n	R5	
adi D12	R2	IO.DIFFIO_RX61p	IO.DIFFIO_TX60p	R10	
adi D13	R3	IO.DIFFIO_RX61n	IO.DIFFIO_TX60n	R11	
adi D14	P1	IO.DIFFIO_RX62p	IO.DIFFIO_TX61p	T5	
adi D15	P2	IO.DIFFIO_RX62n	IO.DIFFIO_TX61n	T6	
			IO.DIFFIO_TX62p	T10	fan_TACH
			IO.DIFFIO_TX62n	T11	fan_EN_n
T1		IO.CLK10p/DIFFIO_RX_C3p			
T2		IO.CLK10n/DIFFIO_RX_C3n			
T3		CLK11p.INPUT	VREFBSN0.VREFBSN0	P3	VCC3_3
T4		CLK11n.INPUT	VREFBSN1.VREFBSN1	J5	
D3		FPLL10CLKp.INPUT	VREFBSN2.VREFBSN2	F5	
D4		FPLL10CLKn.INPUT			

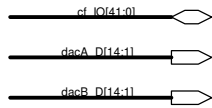
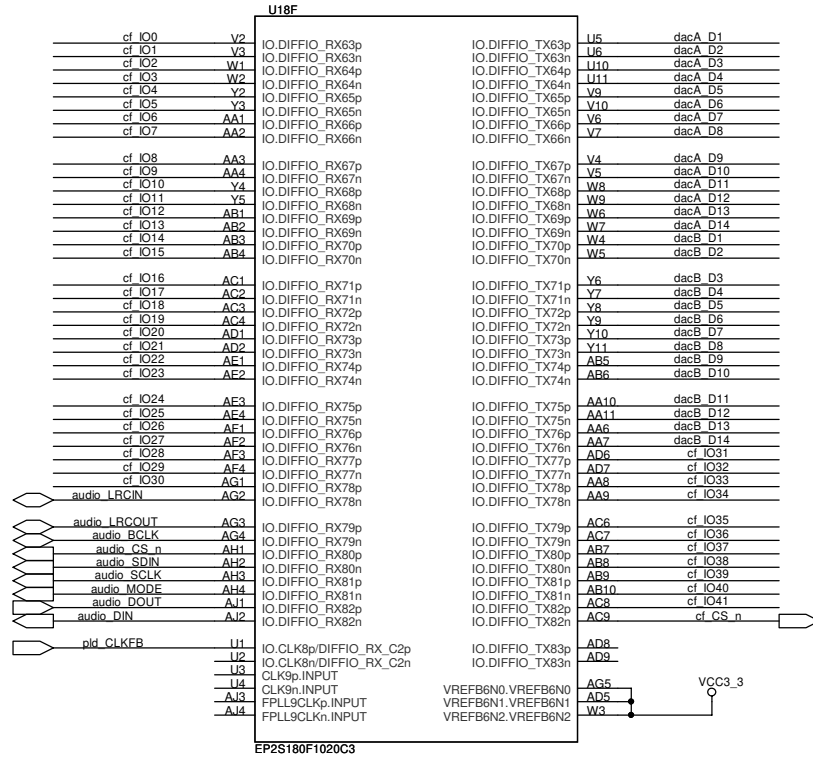
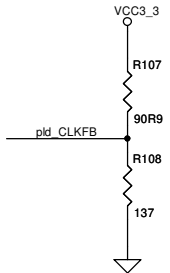
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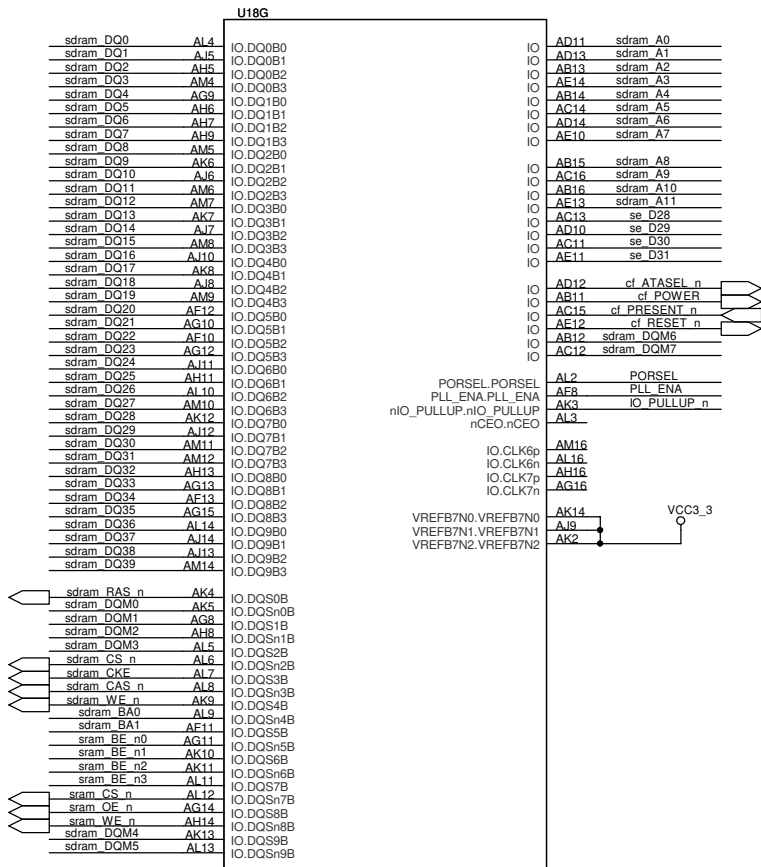
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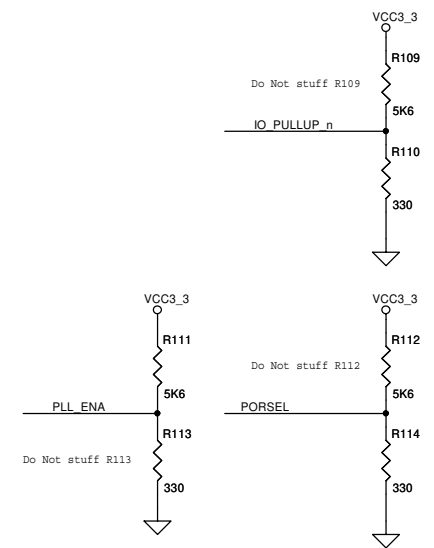
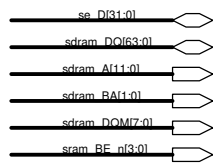
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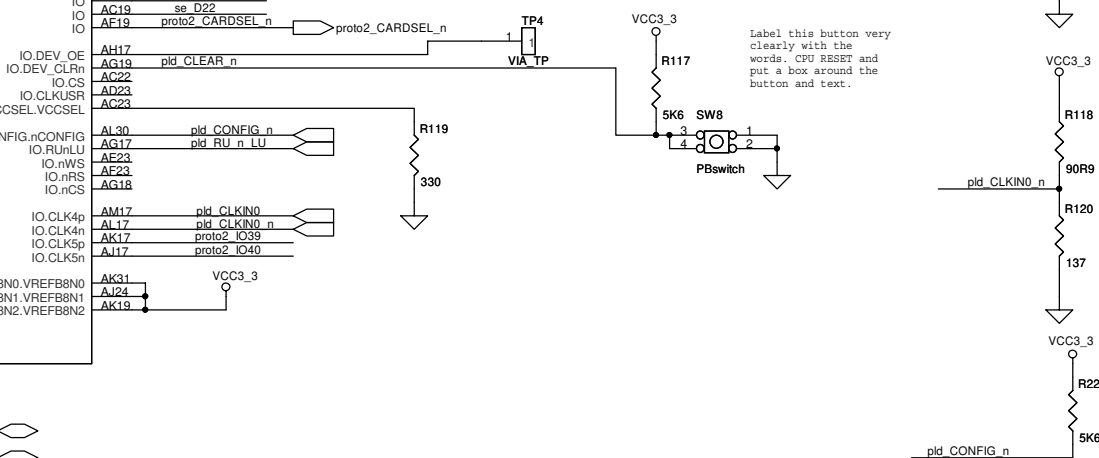
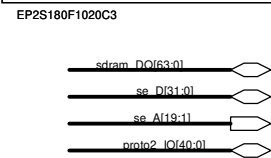
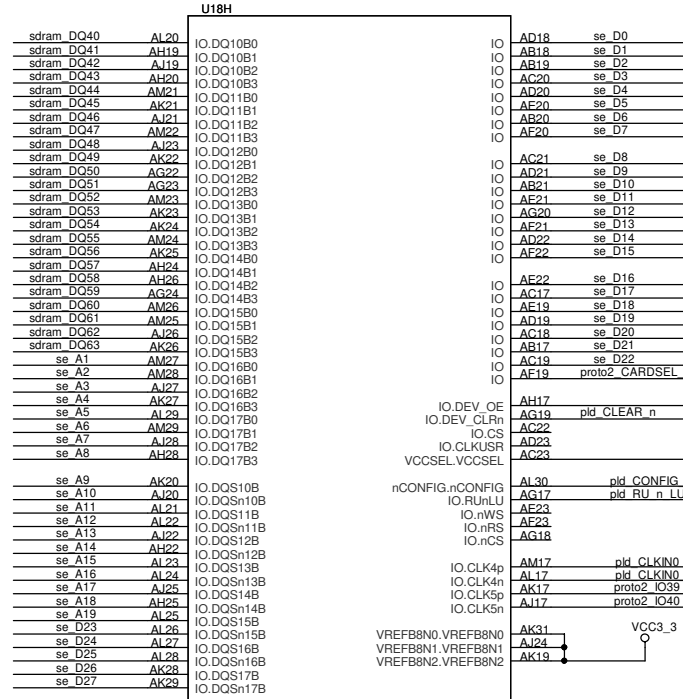
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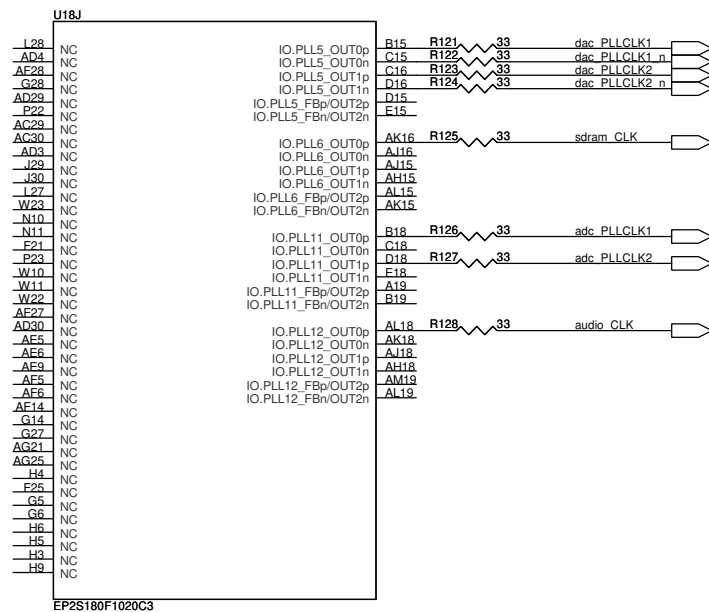
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