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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Cyclone III FPGA Starter Kit

User Guide



101 Innovation Drive San Jose, CA 95134 www.altera.com

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1. Getting Started

Introduction

Welcome to the Altera® Cyclone® III FPGA Starter Kit, which includes a full-featured field-programmable gate array (FPGA) development board, hardware and software development tools, documentation, and accessories needed to begin FPGA development.

The development board includes an Altera Cyclone III FPGA and comes preconfigured with a hardware reference design stored in flash memory. You can use the development board as a platform to prototype a variety of FPGA designs.

The starter kit provides an integrated control environment that includes a software controller in a control panel application, a USB command controller, a multi-port SRAM/DDR SDRAM/flash memory controller, and example designs specified in Verilog code. You can use this design as a starting point for test designs.

This user guide addresses the following topics:

- How to set up, power up, and verify correct operation of the development board.
- How to install the Cyclone III FPGA Starter Kit.
- How to install the Altera® Quartus II Web Edition software.
- How to set up and use the control panel, a graphical user interface (GUI), to manipulate components on the board, implement applications.
- How to configure the Cyclone III FPGA.
- How to set up and run example designs.



For complete details on the development board, refer to the *Cyclone III FPGA Starter Board Reference Manual*.

Before You Begin

Before proceeding, check the contents of the kit:

- Cyclone III FPGA Starter Development Board
- 12-V DC power supply
- USB cable



For the most up-to-date information on this product, visit the Altera website at www.altera.com/products/devkits/altera/kit-cyc3-starter.html.

Further Information

For other related information, refer to the following websites:

| For More Information About | Refer To |
|--|---|
| Additional daughter cards available for purchase | www.altera.com/products/devkits/ kit-daughter_boards.jsp |
| Cyclone III handbook | www.altera.com/literature/lit-cyc3.jsp |
| Cyclone III reference designs | http://www.altera.com/products/devkits/altera/kit-cyc3-starter.html |
| eStore if you want to purchase devices | www.altera.com/buy/devices/buy-devices.html |
| Cyclone III Orcad symbols | www.altera.com/support/software/download/pcb/pcbpcb_index.html |
| Nios® II 32-bit embedded processor solutions | www.altera.com/technology/embedded/ emb-index.html |

Software Installation

This section describes the following procedures:

- "Installing the Cyclone III FPGA Starter Kit"
- "Installing the Quartus II Web Edition Software" on page 1–4

Installing the Cyclone III FPGA Starter Kit

The license-free Cyclone III FPGA Starter Kit installer includes all the documentation and design examples for the kit.

To install the Cyclone III FPGA Starter Kit, follow these steps:

 Download the Cyclone III FPGA Starter Kit installer from the Cyclone III FPGA Starter Kit page of the Altera website. Alternatively, you can request a development kit DVD from the Development Kits, Daughter Cards & Programming Hardware page of the Altera website. 2. Follow the on-screen instructions to complete the installation process.

The installation program creates the Cyclone III FPGA Starter Kit directory structure shown in Figure 1–1.

Figure 1–1. Cyclone III FPGA Starter Kit Default Installed Directory Structure

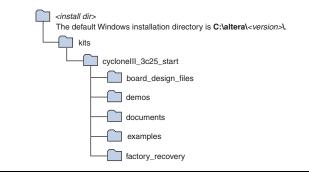


Table 1–1 lists the file directory names and a description of their contents.

| Table 1–1. Installed Directory Contents | | |
|---|--|--|
| Directory Name | Description of Contents | |
| board_design_files | Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design. | |
| demos | Contains demonstration projects that may or may not contain up-to-date source code. | |
| documents | Contains the development kit documentation. | |
| examples | Contains the example design files for the Cyclone III FPG Starter Kit | |
| factory_recovery | Contains programming files for returning board to factory default condition. | |

Installing the Quartus II Web Edition Software

The Quartus II Web Edition software provides the necessary tools for developing hardware and software for Altera FPGAs. Included in the Quartus II Web Edition software are the Quartus II software, the Nios II EDS, and the MegaCore® IP Library. The Quartus II software (including SOPC Builder) and the Nios II EDS are the primary FPGA development tools for creating the reference designs in this kit.

To install the Quartus II Web Edition software, follow these steps:

- Download the Quartus II Web Edition software from the Quartus II Web Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.
- 2. Follow the on-screen instructions to complete the installation process.
 - If you have difficulty installing the Quartus II software, refer to Quartus II Installation & Licensing for Windows and Linux Workstations.

The Quartus II Web Edition software includes the following items:

- Quartus II software—The Quartus II software, including the SOPC Builder system development tool, provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
 - To compare the Quartus II subscription and web editions, refer to *Altera Quartus II Software—Subscription Edition vs. Web Edition*. The kit also works with the subscription edition.
- MegaCore IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions with the OpenCore Plus feature to perform the following tasks:
 - Simulate behavior of a MegaCore function in your system
 - Verify functionality of your design, and quickly and easily evaluate its size and speed
 - Generate time-limited device programming files for designs that include MegaCore functions
 - Program a device and verify your design in hardware



The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

- For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.
- Nios® II Embedded Design Suite (EDS)—A full-featured tool set that allows you to develop embedded software for the Nios II processor which you can include in your Altera FPGA designs.

Licensing Considerations

The Quartus II Web Edition software is license-free and supports Cyclone III devices without any additional licensing requirement. This kit also works with the Quartus II Subscription Edition software, after you obtain the proper license file. To purchase a subscription, contact your Altera sales representative.



2. Development Board and Control Panel Setup

Development Board Setup

The development board is preloaded with an example design to demonstrate the Cyclone[®] III device and board features. At power-up, the preloaded design also enables you to quickly confirm that the board is operating correctly.

Figure 2–1 shows the Cyclone III development board layout and components.

Sense Resistor for FPGA Core Power Measurement (JP6) 1-Mbyte SSRAM (U5) DC Power Input (J2) Power Switch (SW1) Sense Resistor for Shared I/O Power (JP3) 16-Mbyte Parallel **HSMC** Flash (U6) Connector (J1) Connector (J3)Flash LED Cyclone III Device (U1) Configuration Done LED USB UART (U8) Reconfigure User Push Button Switches and Reset JTAG Header (J4) Push Buttons User LEDs 32-Mbyte DDR SDRAM (U4) 50-MHz System Clock

Figure 2-1. Cyclone III Development Board Layout and Components

Requirements

Before you proceed, ensure that the follwing items are installed:

- Altera[®] Quartus[®] II software on the host computer
- Cyclone III FPGA Starter Kit
- USB-BlasterTM driver software on the host computer. The Cyclone III FPGA starter development board includes an integrated USB-Blaster circuitry for FPGA programming.

Powering Up the Development Board

To power-up the development board, follow these steps:

- 1. Ensure that the ON/OFF switch (SW1) is in the OFF position (up).
- 2. Connect the USB-Blaster cable from the host computer to the USB-Blaster port on the development board.
- Connect the 12-V DC adapter to the development board and to a power source.



Only use the supplied 12-V power supply. Power regulation circuitry on the board could be damaged by supplies greater than 12 V.

- 4. Press the power switch (SW1).
- 5. Confirm that all four user LEDs are ON.

Installing the USB-Blaster Driver

The Cyclone III FPGA development board includes an integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster driver on the host computer.

Installation instructions for the USB-Blaster driver are available on the Altera website at www.altera.com/support/software/drivers/dri-index.html. On the "Altera Programming Cable Driver Information" page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

Control Panel Setup

Setting up the control panel involves the following:

- Configuring the FPGA
- Starting the control panel



Power up the board and ensure that is is operational.

For more information about using the control panel, refer to the "Using the Control Panel" chapter.

Configuring the FPGA Using the **Quartus II Programmer**

You can use the Quartus II Programmer to configure the FPGA with a specific .sof. Before configuring the FPGA, ensure that the Quartus II Programmer and the USB-Blaster driver are installed on the host computer, the USB cable is connected to the development board, power to the board is on, and no other applications that use the JTAG chain are running.

To configure the Cyclone III FPGA, follow these steps:

- 1. Start the Quartus II Programmer.
- 2. Click **Add File** and select the path to the desired **.sof**.
- 3. Turn on the **Program/Configure** option for the added file.
- 4. Click **Start** to configure the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.



3. Using the Control Panel

Overview

The control panel consists of the following:

- The graphical user interface (GUI) application on the host computer
- The standard Nios II hardware design running on the board's Cyclone III FPGA device

After installing the Cyclone III FPGA Starter Kit, you can locate the control panel for the hardware and software in the <*kit path*>\demos\control_panel directory.

The design downloaded to the Cyclone III device implements a command controller that processes board commands sent over the USB-Blaster from the control panel. To perform the appropriate actions, the command controller communicates with the controller of the targeted board I/O device.

You can perform the following actions with the control panel:

- Light up LEDs
- Detect push button presses
- Read from and write to the DDR SDRAM, SRAM, flash memory, and on-chip RAM

The following sections describe how to perform the above actions with the control panel already open on the host computer. If not already open, launch the control panel as described in "Control Panel Start".

Control Panel Start

The Cyclone III development board is shipped with an example design stored in the flash memory which configures the Cyclone III FPGA upon power-up with the standard Nios II design.



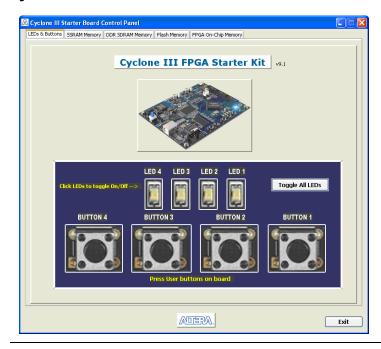
For an older version of the Cyclone III development board shipped with the Cyclone III FPGA Starter Kit v7.1.0, v7.2.0, or 8.0.0 application, you must manually configure the **cycloneIII_3c25_start_niosII_standard.sof** into the FPGA before launching the control panel application.

You can locate the source for the example design in the *<kit path>*\examples\cycloneIII_3c25_starter_board_standard directory.



To launch the control panel user interface, run the **control_panel.exe** program found in the *<kit path>***demos\control_panel** directory (Figure 3–1).

Figure 3-1. Control Panel Window



LEDs and Buttons

Illuminating LEDs

To illuminate an LED, follow these steps:

- 1. The **LED & Buttons** tab should be visible when the application runs. If it is not visible, click the **LED & Buttons** tab (Figure 3–2).
- 2. Click on LEDs to individually turn on the LEDs.

Exit

Buttons Indicators

1. Press the push-button switches on the board. Notice that buttons on the GUI change accordingly.

Cyclone III Starter Board Control Panel

LED & Buttons SSRAM Memory DOR SDRAM Memory Flash Memory FPGA On-Chip Memory

Cyclone III FPGA Starter Kit

V9.1

LED 4 LED 3 LED 2 LED 1

Click LEDs to toggle On/Off ->

BUTTON 4 BUTTON 3 BUTTON 2 BUTTON 1

Figure 3–2. Control Panel Window for LEDs and Buttons

DDR SDRAM/ SSRAM/On-Chip Controller

You can perform the following types of memory read/write operations with the control panel:

ANTERA

- Read from and write to the DDR SDRAM, SSRAM, or on-chip device
- Write entire contents of a file, to the DDR SDRAM, SSRAM, or on-chip device
- Read contents of the DDR SDRAM, SSRAM, or on-chip device, to a file

The following sections describe how to access the DDR SDRAM. You can use the same procedure to access the SSRAM.

Read/Write Data

To read from and write to the DDR SDRAM, follow these steps:

 Click the DDR SDRAM tab (Figure 3–3). The Address column indicates the hex address of the DDR SDRAM. The values inside the 0-3, 4-7, 8-B, and C-F columns are the DDR SDRAM contents in hex words format.

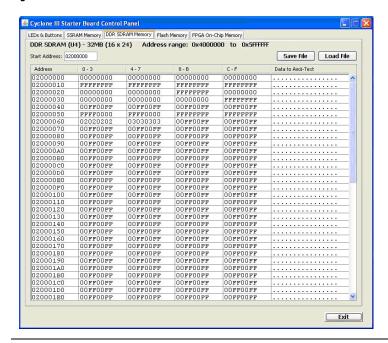


Figure 3-3. Control Panel DDR SDRAM Tab

2. To write a 32-bit word to the DDR SDRAM, click the desired location, enter the desired value in hex format, and press **Enter**.

Read from a File

To read the contents of a file and load it to the DDR SDRAM, follow these steps:

- 1. Click Load File.
- Browse to **sample.txt** located in the **control_panel** directory and click **Open**. This step instantiates the DDR SDRAM controller and loads the text contents into the DDR SDRAM. Notice that the Data to Ascii-text column shows the DDR SDRAM contents in Ascii value.

Write to a File

To write the contents of the DDR SDRAM to a file, follow these steps:

- Click Save File.
- 2. Enter the start and end addresses of the DDR SDRAM.
- 3. Choose a file name and click Save. This instantiates the controller to read the DDR SDRAM contents from the start address to the end address, and write the contents to a file.

Flash Memory **Programmer**

You can perform the following operations to read from and write to the board's flash memory with the control panel:

- Perform a CFI query of flash memory
- Erase select blocks of flash memory
- Write 32-bit hex word to flash memory
- Write a binary file to flash memory
- Load the contents of the flash memory into a file



Do not exit from the control panel while erasing the flash memory.

Flash Memory Tab

To use the flash memory functions, click the **Flash Memory** tab (Figure 3–4).

Cyclone III Starter Board Control Panel LEDs & Buttons SSRAM Memory DDR SDRAM Memory Flash Memory FPGA On-Chip Memory FLASH (U6) - 16MB (16 x 23) Address range: 0x00000000 to 0x0FFFF00 Start Address: 00000000 CFI Query Reset Erase Block Data to Ascii-Text This is a sample text file provi ded for the exam ple of writing a file to memory 20697320 00000000 54686973 61207361 6D706C65 20746578 64656420 706C6520 00000010 00000020 74206669 666F7220 6C652070 74686520 726F7669 6578616D 6F662077 6520746F 72697469 6B672061 6F727920 00000040 206D656D 30217261 20537461 74726F6C 63617469 20437963 72746572 2050616E using AlOlra Cyc 00000050 00000060 7573696E 6C6F6E65 6720416C 20494949 lone III Starter
Kit Control Pan
el application.
If the memory wr
itten to is Flas 20436F6E 70706C69 204B6974 00000080 656C2061 6F6E2E20 00000090 000000A0 49662074 6865206D 656D6F72 20697320 79207772 6E20746F 68652076 656E7473 74207570 6C696E67 h thne the volat ile contents wil 1 persist upon p ower cycling the 000000080 68207468 696C6520 6E652074 6F6C6174 2077696C 000000D0 6C207065 6F6E2070 20746865 72642C20 2066696C 73656420 74686520 000000F0 00000100 20626F61 74686973 486F7765 65206361 00000000 board, Howe.... this file can be 6E206265 00000110 00000120 20657261 696E6720 62792063 45726173 6C69636B 65206275 erased by click ing the Erase bu 6D656D6F 00000130 00000140 2E204F74 2020606C 68657220 74746F6E tton. Other memo tton. Other memo
'a' 'l e'ara
t'alc @dda a Ca
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d d' a bl'la He 20606160 74606160 64686420 20206560 00000150 00000160 63204064 20494140 64612061 20006061 00000170 00000180 20406068 20426164 20406F66 64224D64 206C2061 60706869 616E2020 00000190 000001A0 41202064 68642065 64206F62 61206170 44686163 6E646174 20656864 20602064 68206420 68206420 000001B0 000001C0 68642074 00000110 64206064 62206060 64206160 62622060 000001E0 20204865 20612062 64206460 6C606C61 ATTERA Exit

Figure 3-4. Control Panel Flash Memory Tab

CFI Query

The common flash interface (CFI) flash memory devices conform to basic flash commands. The most basic command is Query which switches the device into a ROM table mode so that features of the flash device are determined by reading values from the table.

To perform a CFI query using the host application, click **CFI Query**. Notice that the memory table displays contents that correlate with the table contents as described in the device datasheet.

To put the flash device back in user mode, press **Reset** on the control panel.

Read/Write Data

To read from and write to the flash memory, follow these steps:

Cyclone III Starter Board Control Panel LEDs & Buttons | SSRAM Memory | DDR SDRAM Memory | Flash Memory | FPGA On-Chip Memory FLASH (U6) - 16MB (16 x 23) Address range: 0x0000000 to 0x0FFFF00 Start Address: 00000000 CFI Query Reset Erase Block Address Data to Ascii-Text 54686973 6D706C65 726F7669 6578616D 00000000 20697320 74206669 61207361 This is a sample text file provi ded for the exam ple of writing a file to memory using Al0!ra Cyc 20746578 64656420 706C6520 000000010 666F7220 6F662077 74686520 72697469 00000030 6B672061 2066696C 7573696E 6520746F 6720416C 206D656D 30217261 6F727920 20437963 lone III Starter
Kit Control Pan
el application.
If the memory wr
itten to is Flas
h thme the volat 20494949 20436F6E 70706C69 6865206D 20537461 74726F60 72746572 2050616E 00000060 6C6F6E65 204B6974 00000080 63617469 656D6F72 6F6E2E20 79207772 nnnnnnan 69747465 6E20746E 20697320 46606173 6F6C6174 ile contents wil l persist upon p ower cycling the board, Howe.... this file can be 000000000 0000000000 696C6520 6C207065 6F776572 636F6E74 72736973 20637963 656E7473 2077696C 6F6E2070 6C696B67 20746865 20626F61 20666960 73656420 74686520 00000100 74686973 65206361 6E206265 20657261 696E6720 74746F6E 6C69636B erased by click ing the Erase bu tton. Other memo 65206275 2E204F74 6D656D6F 00000140 20606160 2020606C 63204064 20206560 61726120 t`alc @dda a Ca 74606160 dhd IA@ .`a per
Bad @ofd"Md @ h
l a`phi.. aan
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ide `bddlp ehd 20494140 20406F66 60706869 68642065 00000160 00000170 00000180 64686420 20426164 20006061 64224D64 20706572 206C2061 41202064 00002061 616E2020 61206170 000001A0 20602064 68206420 20692020 44686163 ide `bddlp ehd d `db ``d a`bb ` d d` a bl`la He 60206264 62206060 20656864 62622060 69646520 000001D0 64206460 20612062 6C606C61 20204865 ANTERVA Exit

Figure 3-5. Control Panel Flash Memory Tab

- Click Erase Block to perform a block erase of the flash memory. The Address column indicates the hex address of the flash memory. The values inside the 0-3, 4-7, 8-B, and C-F columns are the flash memory contents in hex words format.
- 2. To write a 32-bit word to the flash memory, click the desired location, enter the desired value in hex format, and press **Enter**.



4. Measuring Power on the Cyclone III Starter Board

Introduction

One of the main features of the Cyclone[®] III device is its low power consumption. You can measure the power of the 3C25 device on the Cyclone III starter board under various conditions with an example design provided with the kit.

The power example design allows you to control the amount of logic utilized in the FPGA, the clock frequency, the number of I/Os being used, and measure the effect on the power to the Cyclone III device. Because the Cyclone III starter board has only four buttons and four LEDs, interaction with the board is minimal as defined below.

Table 4–1 describes the functionality of the four input buttons that control the power example design.

| Table 4–1. Four Input Button Functionality | | | |
|--|----------|----------------|---|
| Button | FPGA Pin | Туре | Description |
| 1 | F1 | Reset | Resets the demo to the beginning, node i_nrst. |
| 2 | F2 | Toggle | Advances the example design to the next higher frequency, node i_nfreq_next . |
| 3 | A10 | Toggle | Advances the example design to the next higher resource utilization, node_i_nperc_next. |
| 4 | B10 | Press and Hold | Enables the outputs to toggle, node i_noutput_ena. |

Tables 4–2 and 4–3 describe how the LEDs indicate the example design's current power state.

| Table 4–2. LEDs Power State (Frequency) | | | | |
|---|------|------|-------|-----------------|
| Displays | LEDs | | State | Clock Frequency |
| | MSB | LSB | (MHz) | State |
| Frequency | LED2 | LED1 | 00 | 0 |
| | | | 01 | 33 |
| | | | 10 | 67 |
| | | | 11 | 100 |

| Table 4–3. LEDs Power State (Resources) | | | | | |
|---|------|------|------------------------|-------------------|------------------|
| Dianlova | LEDs | | State | 0/ of Dooign Hood | |
| Displays - | MSB | LSB | State % of Design Used | State | % of Design Oseu |
| Resources | LED4 | LED3 | 00 | 25% | |
| | | | 01 | 50% | |
| | | | 10 | 75% | |
| | | | 11 | 100% | |

The design used for power measurement is a replicated set of randomly filled ROMs that feed a multiplier block and a shift register that is fed by a signal that changes every clock cycle. Tables 4–2 and 4–3 show the power state which represent the percent of the full design used. As compiled, this full design uses:

- Logic elements: 22,493/24,624 (91%)
- Combinational functions: 1,961/24,624 (8%)
- Dedicated logic registers: 21,133/24,624 (86%)
- Total registers: 21,133
- Total pins: 73/216 (34%)
- Total memory bits: 524,288/608,256 (86%)
- Embedded Multiplier 9-bit elements: 128/132 (97 %)
- Total PLLs: 1/4 (25%)

Measuring Power

The example design is located in <*kit install*>\examples\cycloneIII_3c25_start_power_demo. Configure

the FPGA with the **.sof** found in the directory.



The input clock (i_clk PIN_B9) is the 50-MHz oscillator on the board, which generates the input clock for the reference design through a PLL



For more information on configuring the FPGA, refer to "Configuring the FPGA Using the Quartus II Programmer" on page 2–3.

Current sense resistors (0.010 Ω ± 1%) are installed at locations JP6 (FPGA core power) and JP3 (FPGA I/O power + other device I/O power). With a digital multimeter set to mV measurement range, the resistor at location JP6 measures the core power. The resistor at location JP3 measures the I/O power. To measure the current being used in various configurations, use the following steps:



To obtain the power (P) in milliwatts, measure *<Measured Voltage>* (the voltage across the sense resistors at JP6 or JP3) in mV and calculate the nominal power using the equation:

P = 100 x < Measured Voltage > x < Supply Voltage >

where *Supply Voltage*> is 1.2 V for JP6 and 2.5 V for JP3.

You can use the four input buttons to advance through the various power state as outlined in Table 4–2. Notice how current increases as frequency and resource usage increase.

You can also measure the I/O power consumed by measuring the voltage across sense-resistor JP3 when Button 4 is pressed and held. Because this 2.5-V power rail is shared with other devices, there is a nominal 100 mW that must be subtracted from the calculated I/O power to obtain the FPGA I/O power.

The number of I/O pins used is controlled by the resource state (shown in Tables 4–2 and 4–3). For each increment in resources, 16 additional I/O pins are added (refer to Table 4–4).

| Table 4–4. I/O Pin & Resource State | | |
|-------------------------------------|--------------------|--|
| LED4/LED3 | Number of I/O Pins | |
| 00 | 16 | |
| 01 | 32 | |
| 10 | 48 | |
| 11 | 64 | |

Similarly, the toggle-frequency of these I/O pins is set by the overall design frequency (refer to Table 4–1).

Changing the Example Design

The source code for the Cyclone III power example design is also provided so you can use it as a starting point for your own measurements. You can adjust the number of outputs by changing parameter NUM_OUTPUTS_PER_STAMP. The default is 16, which for four resource percentage steps equates to $16 \times 4 = 64$.

The appropriate pins to be used as outputs are pre-assigned to the HSMC connector (J1). If you would like to look at more than the 76 I/Os available on J1, you need to make the appropriate pin assignments.