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Nios Development Board

Cyclone II Edition Reference Manual

101 Innovation Drive
San Jose, CA 95134
www.altera.com

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Contents

Appendix A. Restoring the Factory Configuration

Appendix B. Connecting to the Board via Ethernet

About this Manual

This manual provides details about the Nios® development board, Cyclone™ II Edition.Nios Development Board Cyclone II Edition

The table shows this document's revision history.

Date & Revision	Description
May 2007, 1.3	• Corrected Figure 1-1 and Figure 2-21. • Revised "How to Contact Altera". • Updated headers and footers.
October 2006, 1.2	• Corrected statement: LEDs D0 - D7 turn on when driven to 0, not 1. • Updated headers and footers.
June 2006, 1.1	• Updated part numbers to RoHS compliant parts • Corrected D7 pin information in LED pin table • Removed pin labels from J19 figure • Added J19 pin table • Changed PROTO1 and PROTO2 figures to use board net names • Added PROTO1 and PROTO2 pin tables • Corrected FPGA pin label for CON3 pin 9 in PMC Connector pin table • Added new pin AE15 to PMC Connector pin table • Added U69 pin table • Corrected factory config button figure • Added pin and device information and corrected net name for U3 Starting Configuration step 3 • Improved clock circuitry figure • Added clock signal pin tables
May 2005, 1.0	First publication.

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com

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Product literature	Website	www.altera.com/literature
Altera literature services	Email	literature@altera.com
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to table:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.

Visual Cue	Meaning
	The hand points to information that requires special attention.
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
W	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

1. Overview

Features Overview

The Nios Development Board, Cyclone II Edition, provides a hardware platform for developing embedded systems based on Altera® Cyclone II devices. The Nios Development Board, Cyclone II Edition provides the following features:

- Nios Development Board Cyclone II EditionA Cyclone II EP2C35F672C5 or EP2C35F672C5N FPGA with 33,216 logic elements (LE) and 483,840 bits of on-chip memory
- 16 MBytes of flash memory
- 2 MBytes of synchronous SRAM
- 32 MBytes of double data rate (DDR) SDRAM
- On-board logic for configuring the FPGA from flash memory
- On-board Ethernet MAC/PHY device and RJ45 connector
- Two 5.0 V-tolerant expansion/prototype headers each with access to 41 FPGA user I/O pins
- CompactFlash connector for Type I CompactFlash cards
- 32-bit PMC Connector capable of 33 MHz and 66 MHz operation
- Mictor connector for hardware and software debug
- RS-232 DB9 serial port
- Four push-button switches connected to FPGA user I/O pins
- Eight LEDs connected to FPGA user I/O pins
- Dual 7-segment LED display
- JTAG connectors to Altera devices via Altera download cables
- 50 MHz oscillator and zero-skew clock distribution circuitry
- Power-on reset circuitry

General Description

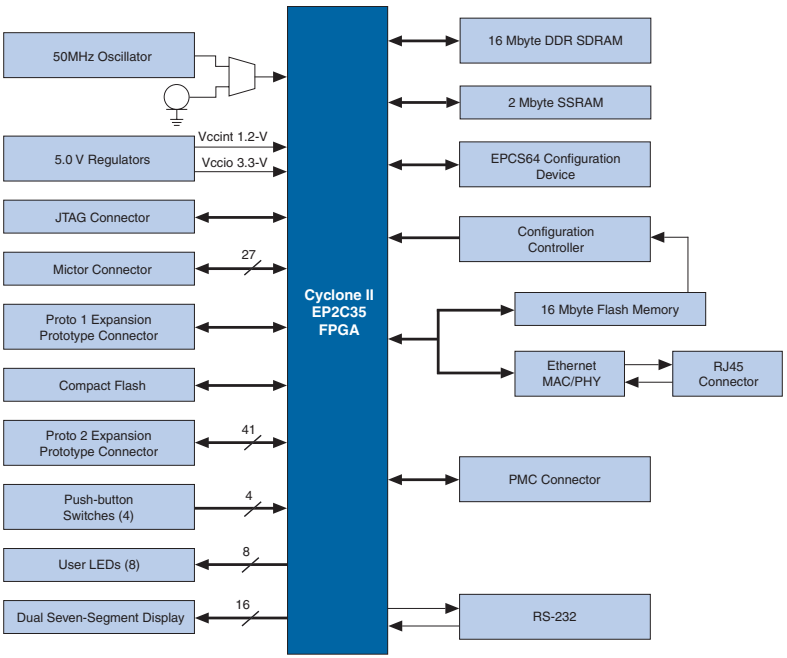
The Nios development board comes pre-programmed with a Nios II processor reference design. Hardware designers can use the reference design as an example of how to build systems using the Nios II processor and to gain familiarity with the features included. Software designers can use the pre-programmed Nios II processor design on the board to begin prototyping software immediately.

This document describes the hardware features of the Nios development board, including detailed pin-out information, to enable designers to create custom FPGA designs that interface with all components on the board. A complete set of schematics, a physical layout database, and GERBER files for the development board are installed with the Nios II development tools in the <*Nios II EDS install path*>**/documents** directory.

See the *Nios II Development Kit, Getting Started User Guide* for instructions on setting up the Nios development board and installing Nios II development tools.

Figure 1–1shows a block diagram of the Nios development board.

Figure 1–1. Nios Development Board, Cyclone II Edition Block Diagram



Factory-Programmed Reference Design

When power is applied to the board, on-board logic configures the FPGA using hardware configuration data stored in flash memory. After successful configuration, the Nios II processor design in the FPGA wakes up and begins executing boot code from flash memory.

The board is factory-programmed with a default reference design. This reference design is a web server that delivers web pages via the Ethernet port. For further information on the default reference design, refer to *Appendix B: Connecting to the Board via Ethernet*.

In the course of development, you might overwrite or erase the flash memory space containing the default reference design. Altera provides the flash image for the default reference design so you can return the board to its default state. Refer to *Appendix A: Restoring the Factory Configuration* for more information.

2. Board Components

Component List

This section introduces all the important components on the Nios development board. See Figure 2–1 and Table 2–1 for component locations and brief descriptions of all board features.

Figure 2–1. Nios Development Board

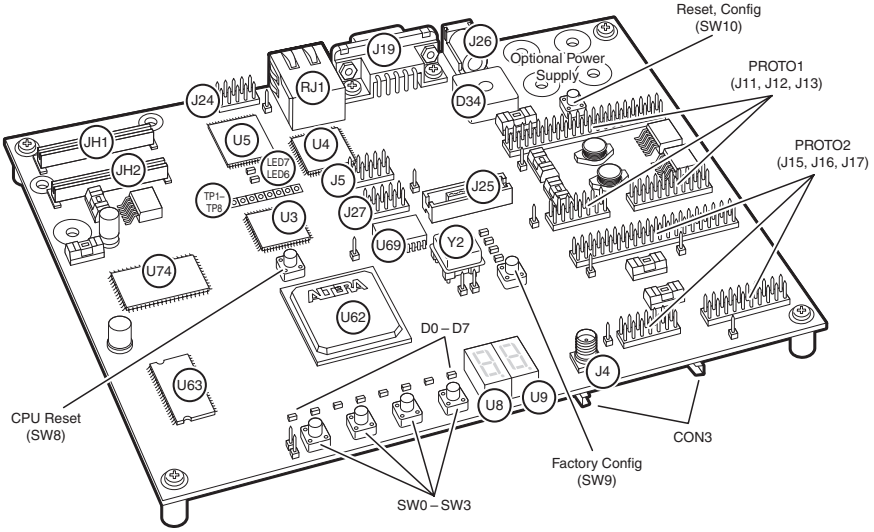


Table 2–1. Nios Development Board, Cyclone II Edition Components & Interfaces		
Board Designation	**Name**	**Description**
U62	Cyclone II FPGA	EP2C35F672C5 or EP2C35F672C5N device.
User Interface		
SW0 – SW3	Push-button switches	Four momentary contact switches for user input to the FPGA.
D0 – D7	Individual LEDs	Eight individual LEDs driven by the FPGA.
U8, U9	Seven-segment LEDs	Two seven-segment LEDs that display numeric output from the FPGA.

Table 2–1. Nios Development Board, Cyclone II Edition Components & Interfaces (Continued)

Board Designation	Name	Description
Memory		
U74	SSRAM memory	2 Mbytes of synchronous SRAM.
U5, LED7	Flash memory	16 Mbytes of nonvolatile memory for use by both the FPGA and the configuration controller. LED7 lights whenever the flash chip-enable is asserted.
U63	DDR SDRAM memory	32 Mbytes of DDR SDRAM.
Connections & Interfaces		
U4, RJ1	Ethernet MAC/PHY	10/100 Ethernet MAC/PHY chip connected to an RJ-45 Ethernet connector.
J19	Serial connector	RS-232 serial connector with 5 V-tolerant buffers. Supports all RS-232 signals.
PROTO1 (J11, J12, J13)	Expansion prototype connector	Expansion headers connecting to 41 I/O pins on the FPGA. Supplies 3.3V and 5.0V for use by a daughter card.
PROTO2 (J15, J16, J17)	Expansion prototype connector	Expansion headers connecting to 41 I/O pins on the FPGA. Supplies 3.3V and 5.0V for use by a daughter card.
CON3	CompactFlash connector	CompactFlash connector for memory expansion.
JH1, JH2	PMC connector	Expansion connector for a PCI mezzanine card.
J25	Mictor connector	Mictor connector providing access to 27 I/O pins on the FPGA. Allows debugging Nios II systems using a First Silicon Solutions (FS2) debug probe.
TP1 – TP8	Test Points	Test points providing access to eight FPGA I/O pins.
J24	JTAG connector	JTAG connection to the FPGA allowing hardware configuration using the Quartus® II software and software debug using the Nios II IDE.
J5	JTAG connector	JTAG connection to the MAX® configuration controller.
J27	EPCS configuration header	Connects to the EPCS serial configuration device for in-system programming.
Configuration & Reset		
U3	MAX Configuration controller	Altera MAX EPM7256AE device used to configure the FPGA from flash memory.
U69	Serial configuration device	Altera EPCS64 low-cost serial configuration device to configure the FPGA.
SW8	CPU Reset button	Push-button switch to reboot the Nios II processor configured in the FPGA.

Table 2–1. Nios Development Board, Cyclone II Edition Components & Interfaces (Continued)		
Board Designation	**Name**	**Description**
SW9	Factory Config button	Push-button switch to reconfigure the FPGA with the factory-programmed reference design.
SW10	Reset, Config	Push-button switch to reset the board.
LED0 – LED3, LED6	Configuration status LEDs	LEDs that display the current configuration status of the FPGA.
Clock Circuitry		
Y2	Oscillator	50 MHz clock signal driven to FPGA.
J4	External clock input	Connector to FPGA clock pin.
Power Supply		
J26	DC power jack	16V DC unregulated power source.
D34	Bridge rectifier	Power rectifier allows for center-negative or center-positive power supplies.
J28, J29, J30, J33 (and more)	Optional Power Supply	External power supply can be connected for high-current applications.

The sections that follow describe each component in detail.

Cyclone II EP2C35 Device (U62)

U62 is a Cyclone II FPGA in a 672-pin FineLine BGA® package. Depending on the board revision, the part number is EP2C35F672C5 or EP2C35F672C5N. Table 2–2 lists the device features.

Table 2–2. Cyclone II EP2C35 Device Features	
LEs	33,216
M4K Memory Blocks	105
Total RAM Bits	483,840
Embedded 18x18 Multiplier Blocks	35
PLLs	4
User I/O Pins	475

Preproduction builds of the Nios Development Board, Cyclone II Editon have an EP2C35F6728ES device.

The development board provides two separate methods for configuring the FPGA:

1. Using the Quartus® II software running on a host computer, a designer configures the device directly via an Altera download cable connected to the FPGA JTAG header (J24).

2. When power is applied to the board, a configuration controller device (U3) attempts to configure the FPGA with hardware configuration data stored in flash memory. For more information on the configuration controller, refer to "Configuration Controller Device (U3)" on page 2–33.

For Cyclone II-related documentation including pin out data for the EP2C35 device, see the Altera Cyclone II literature page at **www.altera.com/literature/lit-cyc2.jsp**.

Push-Button Switches (SW0 - SW3)

SW0 – SW3 are momentary-contact push-button switches to provide stimulus to designs in the FPGA. Refer to Figure 2–2. Each switch is connected to an FPGA general-purpose I/O pin with a pull-up resistor as shown in Table 2–3. Each I/O pin perceives a logic 0 when its corresponding switch is pressed.

Figure 2–2. Push-Button Switches (SW0 – SW3)

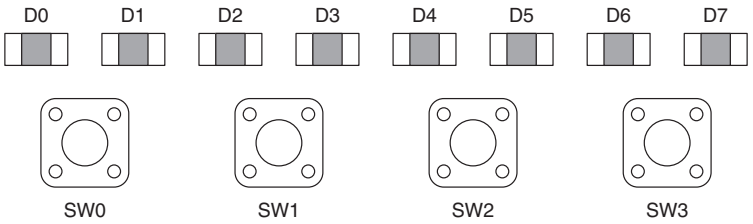


Table 2–3. Push Button Switches Pin Table

Button	FPGA Pin	Board Net Name
SW0	Y11	user_pb0
SW1	AA10	user_pb1
SW2	AB10	user_pb2
SW3	AE6	user_pb3

Individual LEDs (D0 - D7)

This Nios development board provides eight individual LEDs connected to the FPGA. Refer to "Push-Button Switches (SW0 - SW3)" on page 2–4. D0 – D7 are connected to general purpose I/O pins on the FPGA as shown in Table 2–4. When a pin drives logic 0, the corresponding LED turns on.

Table 2–4. LED Pin Table

LED	FPGA Pin	Board Net Name
D0	AC10	pld_led0
D1	W11	pld_led1
D2	W12	pld_led2
D3	AE8	pld_led3
D4	AF8	pld_led4
D5	AE7	pld_led5
D6	AF7	pld_led6
D7	AA11	pld_led7

Seven-Segment LEDs (U8 & U9)

U8 and U9 connect to the FPGA, and each segment is individually controlled by a general-purpose I/O pin. Refer to Figure 2–3. When a pin drives logic 0, the corresponding U8 and U9 LED turns on. See Table 2–5 for pin-out details.

Figure 2–3. Dual Seven-Segment Display

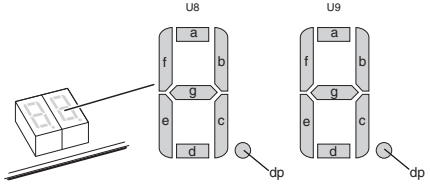


Table 2–5. Dual Seven-Segment Display

FPGA Pin	U8 & U9 Pin	Pin Function	Board Net Name
U8			
AE13	10	a	hex_0A
AF13	9	b	hex_0B
AD12	8	c	hex_0C
AE12	5	d	hex_0D
AA12	4	e	hex_0E
Y12	2	f	hex_0F
V11	3	g	hex_0G
U12	7	dp	hex_0DP
U9			
V14	10	a	hex_1A
V13	9	b	hex_1B
AD11	8	c	hex_1C
AE11	5	d	hex_1D
AE10	4	e	hex_1E
AF10	2	f	hex_1F
AD10	3	g	hex_1G
AC11	7	dp	hex_1DP

SSRAM Chip (U74)

U74 is a 32-bit, 2 Mbyte Cypress SSRAM chip. Depending on the board revision, the part number is CY7C1380C-167AC or CY7C1380D-167AXC. The chip is rated for synchronous accesses up to 167 MHz. U74 connects to the FPGA so it can be used by a Nios II embedded processor as general-purpose memory. The factory-programmed Nios II reference design identifies the SSRAM devices in its address space as a contiguous 2 Mbyte, 32-bit-wide, zero-wait-state main memory.

Table 2–6 shows all connections between the FPGA and the SSRAM chip.

Table 2–6. SSRAM Pin Table

FPGA Pin	U74 Pin	Pin Function	Board Net Name
AB3	37	A0	ssram_a0
AB4	36	A1	ssram_a1
G5	35	A2	ssram_a2
G6	34	A3	ssram_a3
B2	33	A4	ssram_a4
B3	32	A5	ssram_a5
C2	38	NC/A19	ssram_a6
C3	39	NC/A20	ssram_a7
L9	42	A6	ssram_a8
F7	43	A7	ssram_a9
L10	44	A8	ssram_a10
J5	45	A9	ssram_a11
L4	46	A10	ssram_a12
C6	47	A11	ssram_a13
A4	48	A12	ssram_a14
B4	49	A13	ssram_a15
A5	50	A14	ssram_a16
B5	81	A15	ssram_a17
B6	82	A16	ssram_a18
A6	99	A17	ssram_a19
C4	100	A18	ssram_a20
G9	85	ADSC_N	ssram_adsc_n
M3	93	BE_n0	ssram_be_n0
M2	94	BE_n1	ssram_be_n1
M4	95	BE_n2	ssram_be_n2
M5	96	BE_n3	ssram_be_n3
C7	98	CE1_n	ssram_ce1_n
L2	52	D0	ssram_d0
L3	53	D1	ssram_d1
L7	56	D2	ssram_d2
L6	57	D3	ssram_d3
N9	58	D4	ssram_d4

Table 2–6. SSRAM Pin Table (Continued)

FPGA Pin	U74 Pin	Pin Function	Board Net Name
P9	59	D5	ssram_d5
K1	62	D6	ssram_d6
K2	63	D7	ssram_d7
K4	68	D8	ssram_d8
K3	69	D9	ssram_d9
J2	72	D10	ssram_d10
J1	73	D11	ssram_d11
H2	74	D12	ssram_d12
H1	75	D13	ssram_d13
J3	78	D14	ssram_d14
J4	79	D15	ssram_d15
H3	18	D24	ssram_d16
H4	19	D25	ssram_d17
G1	22	D26	ssram_d18
G2	23	D27	ssram_d19
F2	24	D28	ssram_d20
F1	25	D29	ssram_d21
K8	28	D30	ssram_d22
K7	29	D31	ssram_d23
G4	2	D16	ssram_d24
G3	3	D17	ssram_d25
K6	6	D18	ssram_d26
K5	7	D19	ssram_d27
E2	8	D20	ssram_d28
E1	9	D21	ssram_d29
J8	12	D22	ssram_d30
J7	13	D23	ssram_d31
D5	86	OE_n	ssram_oe_n
J9	87	WE_n	ssram_we_n
D7	84	ADSP_n	ssram_adsp_n
H10	83	ADV_n	ssram_adv_n
B7	97	CE2	ssram_ce2
A7	92	CE3_n	ssram_ce3_n

Table 2–6. SSRAM Pin Table (Continued)			
FPGA Pin	**U74 Pin**	**Pin Function**	**Board Net Name**
K9	88	GW_n	ssram_gw_n
E5	89	CLK	sram_clk

The following pins on U74 have fixed connections, which restricts the usable modes of operation:

- MODE is pulled low to enable Linear Burst
- ZZ is pulled low to leave the chip enabled
- GLOBALW_n is pulled high to disable the global write
- CE2 and CE3_n are wired high and low respectively to be enabled and to make CE1_n the master chip enable

See **www.cypress.com** for detailed information about the SSRAM chip.

DDR SDRAM Chip (U63)

U63 is a Micron DDR SDRAM chip. Depending on the board revision, the part number is MT46V16M16TG or MT46V16M16P-6T. The DDR SDRAM pins are connected to the FPGA as shown in Table 2–7. Altera provides a DDR SDRAM controller that allows a Nios II processor to access the DDR SDRAM device as a large, linearly-addressable memory.

Table 2–7. DDR SDRAM Pin Table		
FPGA Pin	**U63 Pin**	**Board Net Name**
R2	2	sdram_dq0
R3	4	sdram_dq1
R4	5	sdram_dq2
P7	7	sdram_dq3
P6	8	sdram_dq4
T2	10	sdram_dq5
T3	11	sdram_dq6
R6	13	sdram_dq7
W2	54	sdram_dq8
W1	56	sdram_dq9
U6	57	sdram_dq10
U7	59	sdram_dq11
U5	60	sdram_dq12
Y1	62	sdram_dq13

Table 2–7. DDR SDRAM Pin Table (Continued)

FPGA Pin	U63 Pin	Board Net Name
V5	63	sdram_dq14
V6	65	sdram_dq15
P3	16	sdram_dqs0
W4	51	sdram_dqs1
U2	20	sdram_dm0
AA1	47	sdram_dm1
T6	29	sdram_a0
V2	30	sdram_a1
R8	31	sdram_a2
W3	32	sdram_a3
R5	35	sdram_a4
U10	36	sdram_a5
P4	37	sdram_a6
V1	38	sdram_a7
T9	39	sdram_a8
T8	40	sdram_a9
AA2	28	sdram_a10
T10	41	sdram_a11
U3	42	sdram_a12
U9	26	sdram_ba0
Y4	27	sdram_ba1
U1	22	sdram_cas_n
R7	44	sdram_cke
Y3	24	sdram_cs_n
V4	23	sdram_ras_n
U4	21	sdram_we_n
AA6	46	sdram_clk_n
AA7	45	sdram_clk_p

See **www.micron.com** for detailed information.

Flash Memory (U5)

U5 is an 8-bit, 16 Mbyte AMD flash memory device connected to the FPGA. Depending on the board revision, the part number is AM29LV128M or S29GL128M10TFIR1. Refer to Table 2–8 for connections between the FPGA and the flash memory chip. U5 can be used for two purposes:

1. A Nios II embedded processor implemented on the FPGA can use the flash memory as general-purpose memory and non-volatile storage.

2. The flash memory can hold FPGA configuration data that is used by the configuration controller to load the FPGA at power-up. Refer to "Configuration Controller Device (U3)" on page 2–33 for related information.

A Nios II processor design in the FPGA can identify the 16 Mbyte flash memory in its address space, and can program new data (either new FPGA configuration data, Nios II software, or both) into flash memory. The Nios II development software includes subroutines for writing and erasing flash memory.

The flash memory device shares address and data connections with the Ethernet MAC/PHY device.

Table 2–8. Flash Memory Pin Table

FPGA Pin	U5 Pin	Board Net Name
F9	51	fe_a0
H8	31	fe_a1
D11	26	fe_a2
E8	25	fe_a3
B14	24	fe_a4
A14	23	fe_a5
F14	22	fe_a6
G14	21	fe_a7
F13	20	fe_a8
G13	10	fe_a9
C15	9	fe_a10
B15	8	fe_a11
B16	7	fe_a12
C16	6	fe_a13
D15	5	fe_a14

Table 2–8. Flash Memory Pin Table (Continued)

FPGA Pin	U5 Pin	Board Net Name
E15	4	fe_a15
H15	3	fe_a16
H16	54	fe_a17
A17	19	fe_a18
B17	18	fe_a19
G15	11	fe_a20
F15	12	fe_a21
F16	15	fe_a22
G16	2	fe_a23
D8	35	fe_d0
C8	37	fe_d1
F10	39	fe_d2
G10	41	fe_d3
D9	44	fe_d4
C9	46	fe_d5
B8	48	fe_d6
A8	50	fe_d7
H17	32	flash_cs_n
F17	34	flash_oe_n
G17	13	flash_rw_n
B18	16	flash_wp_n
C17	53	flash_byte_n (1)
D17	17	flash_ry_by_n

Note to Table 2–8:
(1) BYTE_n on U5 is pulled low to keep the flash memory in byte mode which restricts the usable modes of operation.

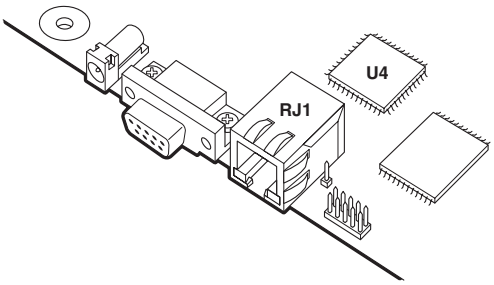
The on-board configuration controller makes assumptions about what-resides-where in flash memory. For details refer to "SW10 – Reset, Config" on page 2–35.

See **www.amd.com** for detailed information about the flash memory device.

Ethernet MAC/PHY (U4) & RJ45 Connector (RJ1)

The LAN91C111 chip (U4) is a 10/100 Ethernet media access control and physical interface (MAC/PHY) chip. The control pins of U4 are connected to the FPGA so that Nios II systems can access Ethernet networks via the RJ-45 connector (RJ1) as shown in Figure 2–4. The Nios II development tools include hardware and software components that allow Nios II processor systems to communicate with the LAN91C111 Ethernet device.

Figure 2–4. Ethernet RJ-45 Connector



Refer to Table 2–9 for connections between the FPGA and the MAC/PHY device.

The Ethernet MAC/PHY device shares both address and data connections with the flash memory.

Table 2–9. Ethernet MAC/PHY Pin Table

FPGA Pin	U4 Pin	Pin Function	Board Net Name (1)
E26	41	Address Enable	enet_aen
J17	43	Synchronous Ready	enet_srdy_n
F18	40	VL Bus Access	enet_vlbus_n
G18	45	Local Device	enet_ldev_n
D18	38	IO Char Ready	enet_iochrdy
E18	37	Address Strobe	enet_ads_n
A19	42	Local Bus Clock	enet_lclk
B19	46	Ready/Return	enet_rdyrtn_n
D20	35	Bus Cycle	enet_cycle_n
D14	36	Write/Read	enet_w_r_n
Y15	34	Bus Chip Select	enet_datacs_n
AA15	29	Interrupt	enet_intr0