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Nios® II

Nios Development Board

Reference Manual, Stratix II Edition

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Contents

About this Manual

This manual provides component details about the Nios® development board, Stratix™ II Edition.

The following table shows the reference manual's revision history.

Date	Description
July 2005	Updated for the EP2S30 device.
October 2004	Updated the heat sink illustrations.
September 2004	First publication of Nios Development Board Reference Manual, Stratix II Edition

How to Find Information

- The Adobe Acrobat Find feature allows you to search the contents of a PDF file. Click the binoculars toolbar icon to open the Find dialog box.
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This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
⚠	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
👣	The feet direct you to more information on a particular topic.

Introduction

Features Overview

The Nios development board, Stratix II Edition, provides a hardware platform for developing embedded systems based on Altera Stratix II devices. The Nios development board, Stratix II Edition provides the following features:

- A Stratix II FPGA with more than 13,500 adaptive logic modules (ALM) and 1.3 million bits of on-chip memory
- 16 Mbytes of flash memory
- 1 Mbyte of static RAM
- 16 Mbytes of SDRAM
- On board logic for configuring the Stratix II device from flash memory
- On-board Ethernet MAC/PHY device
- Two 5V-tolerant expansion/prototype headers each with access to 41 Stratix II user I/O pins
- CompactFlash™ connector for Type I CompactFlash cards
- Mictor connector for hardware and software debug
- Two RS-232 DB9 serial ports
- Four push-button switches connected to Stratix II user I/O pins
- Eight LEDs connected to Stratix II user I/O pins
- Dual 7-segment LED display
- JTAG connectors to Altera® devices via Altera download cables
- 50 MHz oscillator and zero-skew clock distribution circuitry
- Power-on reset circuitry

General Description

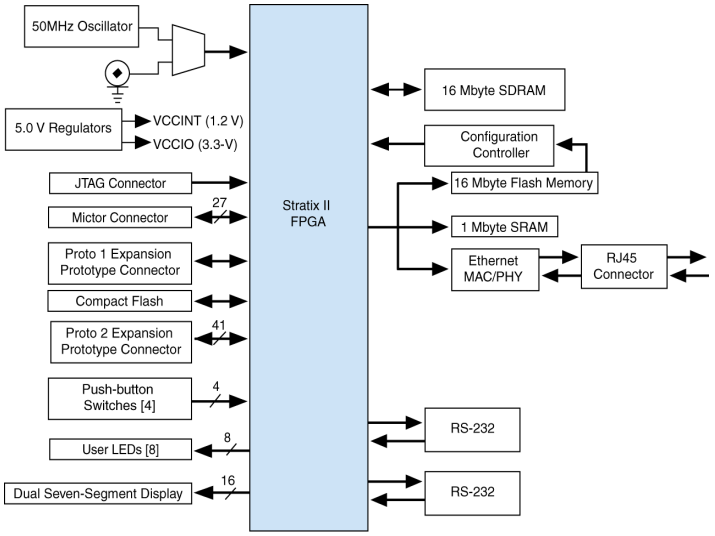
The Nios development board comes pre-programmed with a Nios II processor reference design. Hardware designers can use the reference design as an example of how to use the features of the Nios development board. Software designers can use the pre-programmed Nios II processor design on the board to begin prototyping software immediately.

This document describes the hardware features of the Nios development board, including detailed pin-out information, to enable designers to create custom FPGA designs that interface with all components on the board.

Refer to the Nios II Development Kit, Getting Started User Guide for instructions on setting up the Nios development board and installing Nios II development tools.

Figure 1–1 shows a block diagram of the Nios development board.

Figure 1–1. Nios Development Board, Stratix II Edition Block Diagram



Early shipments of the Nios development board, Stratix II edition use an EP2S60F672C5ES device. This is a fully tested engineering sample (ES) device. However, it has a known issue affecting the M-RAM blocks. The issue can be worked around easily, but some consideration is required when migrating designs based on this device to a non-ES device. There is a label near the FPGA; if the letters "ES" appear on the label, the device is an engineering sample.

For details, refer to the Stratix II FPGA Family Errata Sheet and the documented example designs included in the Nios II Development Kit.

Factory-Programmed Reference Design

When power is applied to the board, on-board logic configures the Stratix II FPGA using hardware configuration data stored in flash memory. When the device is configured, the Nios II processor design in the FPGA wakes up and begins executing boot code from flash memory.

The board is factory-programmed with a default reference design. This reference design is a web server that delivers web pages via the Ethernet port. For further information on the default reference design, see Appendix C, Connecting to the Board via Ethernet.

In the course of development, you may overwrite or erase the flash memory space containing the default reference design. Altera provides the flash image for the default reference design so you can return the board to its default state. See Appendix B, Restoring the Factory Configuration for more information.

Component List

This section introduces all the important components on the Nios development board (see Figure 2–1). A complete set of schematics, a physical layout database, and GERBER files for the development board are installed in the Nios II development kit **documents** directory.

See Figure 2–1 and Table 2–1 on page 2–6 for locations and brief descriptions of all features of the board.

Figure 2–1. Nios Development Board

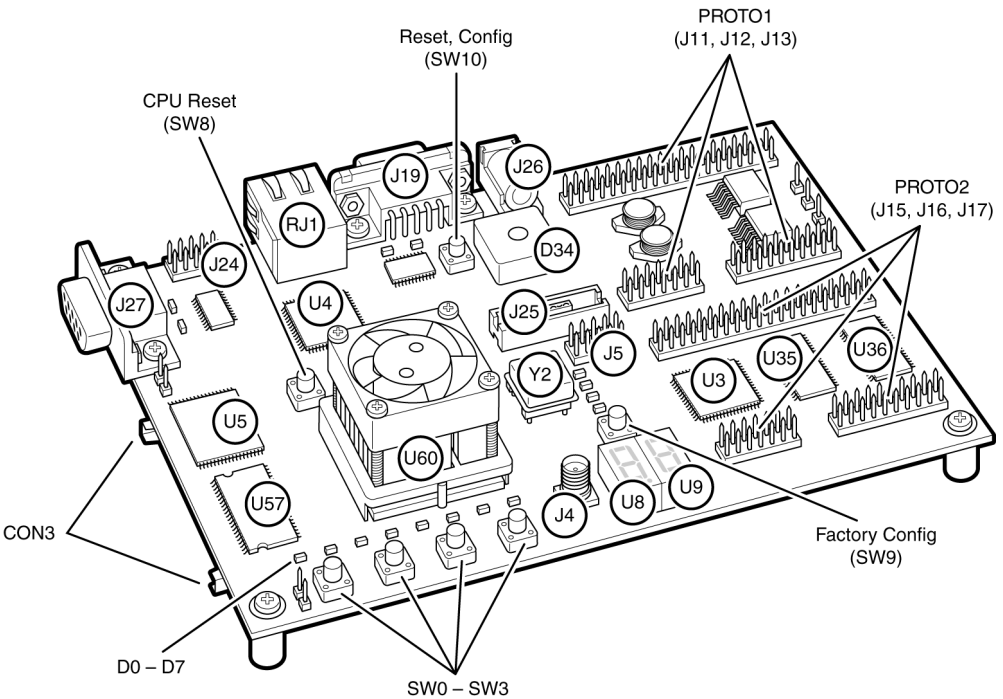


Table 2–1. Nios Development Board, Stratix Edition Components & Interfaces (Part 1 of 2)

Board Designation	Name	Description
Featured Device		
U60	Stratix II FPGA	EP2S60F672C5 or EP2S30F672C5 device with mounted heat sink
User Interface		
SW0 – SW3	Push-button switches	Four momentary contact switches for user input to the FPGA
D0 – D7	Individual LEDs	Eight individual LEDs driven by the FPGA
U8, U9	Seven-segment LEDs	Two seven-segment LEDs to display numeric output from the FPGA
Memory		
U35, U36	SRAM memory	Two SRAM chips combined to form 1 Mbyte of fast, static RAM
U5	Flash memory	16 Mbytes of nonvolatile memory for use by both the FPGA and the configuration controller
U57	SDRAM memory	16 Mbytes of SDRAM
Connectors & Interfaces		
U4, RJ1	Ethernet MAC/PHY	10/100 Ethernet MAC/PHY chip connected to an RJ-45 Ethernet connector
J19, J27	Serial connectors	Two serial connectors with 5 V-tolerant buffers. Supports all RS-232 signals.
PROTO1 (J11, J12, J13)	Expansion prototype connector	Expansion headers connecting to 41 I/O pins on the FPGA. Supplies 3.3V and 5.0V for use by a daughter card.
PROTO2 (J15, J16, J17)	Expansion prototype connector	Expansion headers connecting to 41 I/O pins on the FPGA. Supplies 3.3V and 5.0V for use by a daughter card.
CON3	CompactFlash connector	CompactFlash connector for memory expansion
J25	Mictor connector	Mictor connector for debugging Nios II systems using a First Silicon Solutions (FS2) debug probe.
J24	JTAG connector	Connects to the FPGA allowing hardware configuration from Quartus II software and software debug from the Nios II IDE.
J5	JTAG connector	Connects to the configuration controller
Configuration & Reset		
U3	Configuration controller	Altera EPM7128AE device used to configure the FPGA from flash memory

Table 2–1. Nios Development Board, Stratix Edition Components & Interfaces (Part 2 of 2)		
Board Designation	**Name**	**Description**
SW8	CPU Reset button	Push-button switch to reboot the Nios II processor configured in the FPGA
SW9	Factory Config button	Push-button switch to reconfigure the FPGA with the factory-programmed reference design
SW10	Reset, Config	Push-button switch to reset the board
LED0 – LED3	Configuration status LEDs	LEDs that display the current configuration status of the FPGA
Clock Circuitry		
Y2	Oscillator	50 MHz clock signal driven to FPGA
J4	External clock input	Connector to FPGA clock pin
Power Supply		
J26	DC power jack	17 V DC unregulated power source
D34	Bridge rectifier	Power rectifier allows for center-negative or center-positive power supplies

The sections that follow describe each component in detail.

Stratix II Device (U60)

U60 is a Stratix II FPGA in a 672-pin FineLine BGA® package. Early shipments of the Nios Development Board, Stratix II Edition included an EP2S60F672C5 device. Some early boards used engineering sample parts, indicated by "ES" after the part number. Later shipments of the board use an EP2S30F672C5 device. Table 2–2 lists the device features.

Table 2–2. Stratix II Device Features (Part 1 of 2)		
Feature	**EP2S30**	**EP2S60**
ALMs	13,552	24,176
Adaptive look-up tables (ALUTs)	27,104	48,352
Equivalent LEs	33,880	60,440
M512 RAM blocks	202	329
M4K RAM blocks	144	255
M-RAM blocks	1	2
Total RAM bits	1,369,728	2,544,192
DSP blocks	16	36

Table 2–2. Stratix II Device Features (Part 2 of 2)

Feature	EP2S30	EP2S60
18-bit x 18-bit multipliers	64	144
Enhanced PLLS	2	4
Fast PLLs	4	8
User I/O pins	500	492

The development board provides two separate methods for configuring the Stratix II device:

1. Using the Quartus II software running on a host computer, a designer configures the device directly via an Altera® download cable connected to the Stratix II JTAG header (J24).

2. When power is applied to the board, a configuration controller device (U3) attempts to configure the Stratix II device with hardware configuration data stored in flash memory. For more information on the configuration controller, see "Configuration Controller Device (U3)" on page 2–25.

For Stratix II-related documentation including Stratix II pinout data refer to the Altera Stratix II literature page at **www.altera.com/ literature/lit-stx2.html**.

Early shipments of the board had a heat sink mounted on the Stratix II FPGA. Boards shipped later than May 2005 do not include the heat sink, because thermal management is unnecessary for the majority of FPGA designs for this board. A heat sink maintains the FPGA within its specified thermal operating range, independent of the resource utilization, clock frequency, and operating conditions of the FPGA. The heat sink used on early shipments of the board is produced by Intricast Inc., part number CS1995V01. See **www.intricast.com** for details.

Refer to Altera's *AN185: Thermal Management Using Heat Sinks* for information on using heat sinks with Altera devices.

Push-Button Switches (SW0 - SW3)

SW0 – SW3 are momentary-contact push-button switches and are used to provide stimulus to designs in the Stratix II device. See Figure 2–2. Each switch is connected to a Stratix II general-purpose I/O pin with a pull-up resistor as shown in Table 2–3. Each Stratix II device pin will see a logic 0 when its corresponding switch is pressed.

Table 2–3. Push Button Switches Pin Out Table

Button	Stratix II Pin
SW0	W24
SW1	W23
SW2	Y24
SW3	Y23

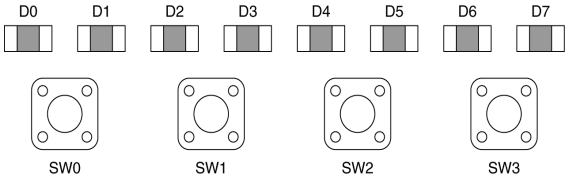
Individual LEDs (D0 - D7)

This Nios development board provides eight individual LEDs connected to the Stratix II device. See Figure 2–2. D0 – D7 are connected to general purpose I/O pins on the Stratix II device as shown in Table 2–4. When the Stratix II pin drives logic 1, the corresponding LED turns on.

Table 2–4. LED Pin Out Table

LED	Stratix II Pin
D0	AD26
D1	AD25
D2	AC25
D3	AC24
D4	AB24
D5	AB23
D6	AB26
D7	AB25

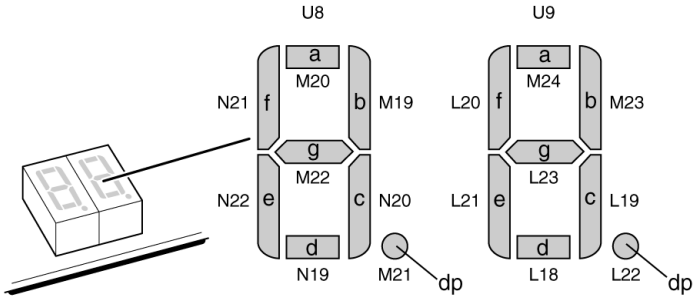
Figure 2–2. Push Button Switches & Individual LEDs



Seven-Segment LEDs (U8 & U9)

U8 and U9 are connected to the Stratix II device so that each segment is individually controlled by a general-purpose I/O pin. When the Stratix II pin drives logic 0, the corresponding LED turns on. See Figure 2–3 for Stratix II pin-out details.

Figure 2–3. Seven-Segment LEDs



SRAM Memory (U35 & U36)

U35 and U36 are IDT IDT71V416S, 512 Kbyte x 16-bit asynchronous SRAM devices. They are connected to the Stratix II device so they can be used by a Nios II embedded processor as general-purpose memory. The two 16-bit devices can be used in parallel to implement a 32-bit wide memory subsystem. The factory programmed Nios II reference design identifies these SRAM devices in its address space as a contiguous 1Mbyte, 32-bit-wide, zero-wait-state main memory.

The SRAM devices share address and data connections with the flash memory and the Ethernet MAC/PHY device. For shared bus information, see Appendix A, Shared Bus Table.

Refer to **www.idt.com** for detailed information about the SRAM devices.

Flash Memory (U5)

U5 is a 16 Mbyte AMD AM29LV128M flash memory device connected to the Stratix II device and can be used for two purposes:

1. A Nios II embedded processor implemented on the Stratix II device can use the flash as general-purpose readable memory and non-volatile storage.

2. The flash memory can hold Stratix II device configuration data that is used by the configuration controller to load the Stratix II device at power-up. See "Configuration Controller Device (U3)" on page 2–25 for related information.

A Nios II processor design in the FPGA can identify the 16 Mbyte flash memory in its address space, and can program new data (either new Stratix II configuration data, Nios II embedded processor software, or both) into flash memory. The Nios II embedded processor software includes subroutines for writing and erasing flash memory.

The flash memory device shares address and data connections with the SRAM chips and the Ethernet MAC/PHY chip. For shared bus information, see Appendix A, Shared Bus Table.

The on-board configuration controller makes assumptions about what-resides-where in flash memory. For details see section "Flash Memory Partitions" on page 2–27.

See **www.amd.com** for detailed information about the flash memory device.

SDRAM Memory (U57)

The SDRAM device (U57) is a Micron MT48LC4M32B2 with PC100 functionality and self refresh mode. The SDRAM is fully synchronous with all signals registered on the positive edge of the system clock.

The SDRAM device pins are connected to the Stratix II device (see Table 2–5). An SDRAM controller peripheral is included with the Nios II development kit, allowing a Nios II processor to view the SDRAM device as a large, linearly-addressable memory.

Table 2–5. SDRAM (U57) Pin Table (Part 1 of 2)

Pin Name	Pin Number	Connects to Stratix II Pin
A0	25	AD4
A1	26	AD3
A2	27	AD5
A3	60	W9
A4	61	W10
A5	62	AB10
A6	63	AF5
A7	64	AE5
A8	65	AC6
A9	66	AF6
A10	24	AA10
A11	21	Y9
BA0	22	AE23
BA1	23	AD23
DQ0	2	W15
DQ1	4	V14
DQ2	5	AA16
DQ3	7	AD16
DQ4	8	AF17
DQ5	10	AD17
DQ6	11	AF18
DQ7	13	AA17
DQ8	74	V16
DQ9	76	AB17
DQ10	77	AF19
DQ11	79	AD18
DQ12	80	AD19

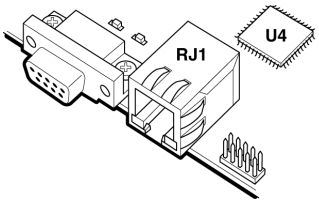
Table 2–5. SDRAM (U57) Pin Table (Part 2 of 2)		
Pin Name	**Pin Number**	**Connects to Stratix II Pin**
DQ13	82	AF20
DQ14	83	AC17
DQ15	85	V17
DQ16	31	AB18
DQ17	33	AF21
DQ18	34	AD20
DQ19	36	AD21
DQ20	37	AF22
DQ21	39	AC18
DQ22	40	W18
DQ23	42	AB19
DQ24	45	AD22
DQ25	47	AE22
DQ26	48	AF24
DQ27	50	AE24
DQ28	51	AB7
DQ29	53	V10
DQ30	54	AA8
DQ31	56	AF3
DQM0	16	AF7
DQM1	71	AD7
DQM2	28	AC7
DQM3	59	AF8
RAS_N	19	AE17
CAS_N	18	AE16
CKE	67	AE20
CS_N	20	AE19
WE_N	17	AE18
CLK	68	AF12

Refer to **www.micron.com** for detailed information.

Ethernet MAC/PHY (U4)

The LAN91C111 (U4) is a mixed signal analog/digital device that implements protocols at 10 Mbps and 100 Mbps. The control pins of U4 are connected to the Stratix II device so that Nios II systems can access Ethernet via the RJ-45 connector (RJ1).See Figure 2–4 on page 2–14. The Nios II development kit includes hardware and software components that allow Nios II processor systems to communicate with the LAN91C111 Ethernet device.

Figure 2–4. Ethernet RJ-45 Connector



The Ethernet MAC/PHY device shares address and data connections with the flash memory and the SRAM chips. For shared bus information, see Appendix A, Shared Bus Table

Refer to **www.smsc.com** for detailed information about the LAN91C111 device.

Serial Port Connectors (J19 & J27)

J19 and J27 are standard DB-9 serial connectors. These connectors are typically used for communication with a host computer using a standard, 9-pin serial cable connected to (for example) a COM port. Level-shifting buffers (U52 and U58) are used between J19 & J27 and the Stratix II device, because the Stratix II device cannot interface to RS-232 voltage levels directly.

J19 and J27 are able to transmit all RS-232 signals. Alternately, the Stratix II design may use only the signals it needs, such as J19's `RXD` and `TXD`. LEDs are connected to the `RXD` and `TXD` signals, giving a visual indication when data is being transmitted or received. Figure 2–5 and Figure 2–6 show the pin connections between the serial connectors and the Stratix II device.

Figure 2–5. Serial Connector J19

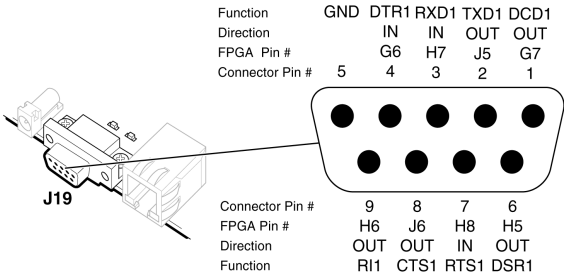
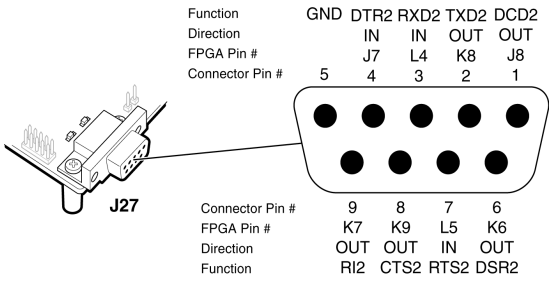


Figure 2–6. Serial Connector J27



Expansion Prototype Connectors (PROTO1 & PROTO2)

PROTO1 and PROTO2 are standard-footprint, mechanically-stable connections that can be used (for example) as an interface to a special-function daughter card. Headers J11, J12, and J13 collectively form PROTO1, and J15, J16 and J17 collectively form PROTO2.

The expansion prototype connector interface includes:

- 41 I/O pins for prototyping. All 41 I/O pins connect to user I/O pins on the Stratix II device. Each signal passes through analog switches to protect the Stratix II device from 5V logic levels. These analog switches are permanently enabled. The output logic-level on the expansion prototype connector pins is 3.3V.
  - PROTO1 switches: U19, U20, U21, U22 and U25
  - PROTO2 switches: U27, U28, U29, U30 and U31
- A buffered, zero-skew copy of the on-board oscillator output from U2.
- A buffered, zero-skew copy of the Stratix II phase-locked loop (PLL) output from U60.

- A logic-negative power-on reset signal.
- Five regulated 3.3V power-supply pins (2A total max load for both PROTO1 & PROTO2).
- One regulated 5V power-supply pin (1A total max load for both PROTO1 & PROTO2).
- Numerous ground connections.

The PROTO1 expansion prototype connector shares Stratix II I/O pins with the CompactFlash connector (CON3). Designs may use either the PROTO1 connector or the CompactFlash connector.

Refer to the Altera web site for a list of available expansion daughter cards that can be used with the Nios development board at **www.altera.com/devkits.**

Figure 2–7, and Figure 2–8 on page 2–17 show connections from the PROTO1 expansion headers to the Stratix II device. Unless otherwise noted, labels indicate Stratix II device pin numbers.

Figure 2–7. PROTO1 Expansion Prototype Connector - J11, J12 & J13

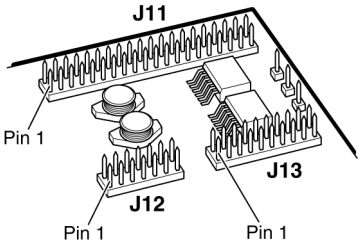
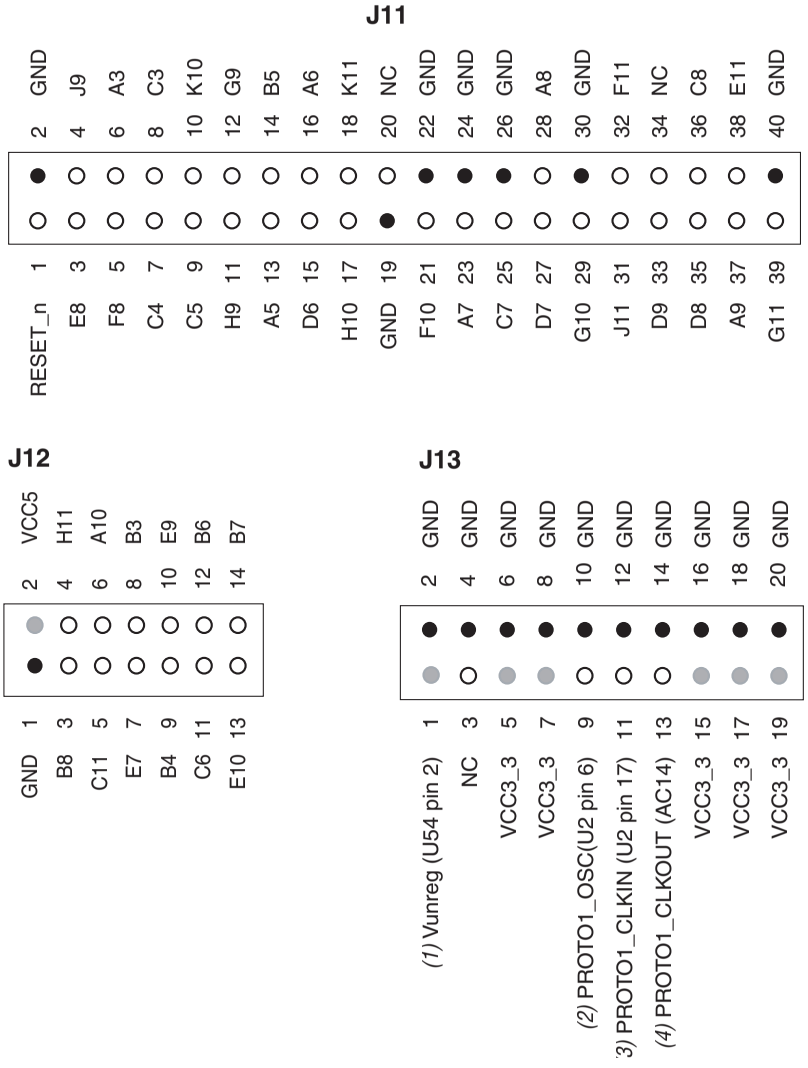


Figure 2–8. PROTO1 Pin Information - J11, J12 & J13



Note to Figure 2–8

(1) Unregulated voltage from DC power supply
(2) Clk from board oscillator
(3) Clk from FPGA via buffer
(4) Clk output from protocard to FPGA